

PHP/PHB/PHD63NQ03LT

TrenchMOS™ logic level FET

Rev. 01 — 14 June 2002

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHP63NQ03LT in SOT78 (TO-220AB)

PHB63NQ03LT in SOT404 (D²-PAK)

PHD63NQ03LT in SOT428 (D-PAK).

1.2 Features

- Logic level compatible
- Low gate charge

1.3 Applications

- DC to DC converters
- Switched mode power supplies

1.4 Quick reference data

- $V_{DS} = 30\text{ V}$
- $I_D = 68.9\text{ A}$
- $P_{tot} = 111\text{ W}$
- $R_{DSon} \leq 13\text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT428 simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)	<p style="text-align: center;"> SOT78 (TO-220) SOT404 (D²-PAK) SOT428 (D-PAK) </p>	

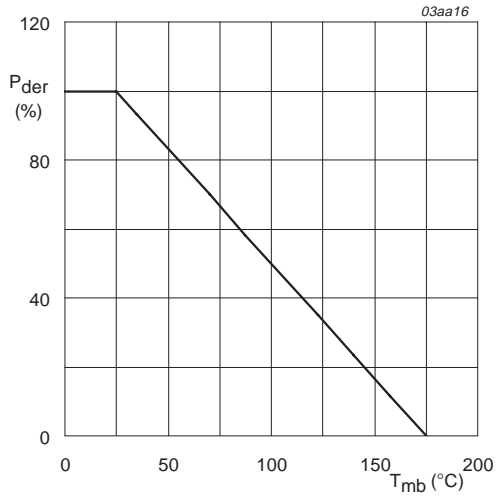
[1] It is not possible to make connection to pin 2 of the SOT404 or SOT428 packages.

3. Limiting values

Table 2: Limiting values

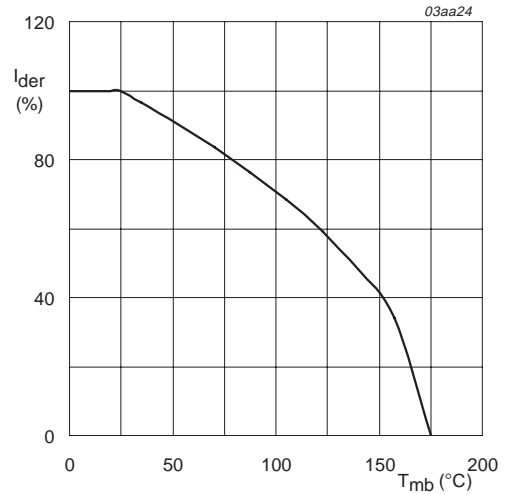
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
V_{GSM}	peak gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$; pulsed; duty cycle = 25 %	-	± 25	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	68.9	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	48.7	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	111	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	68.9	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	48.7	A



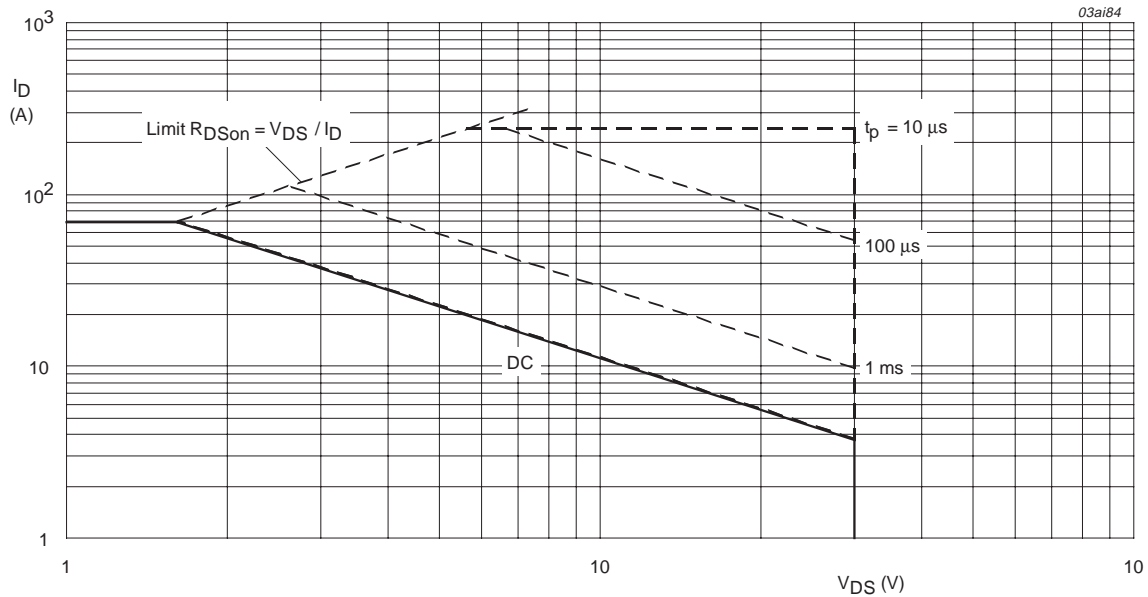
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10V.

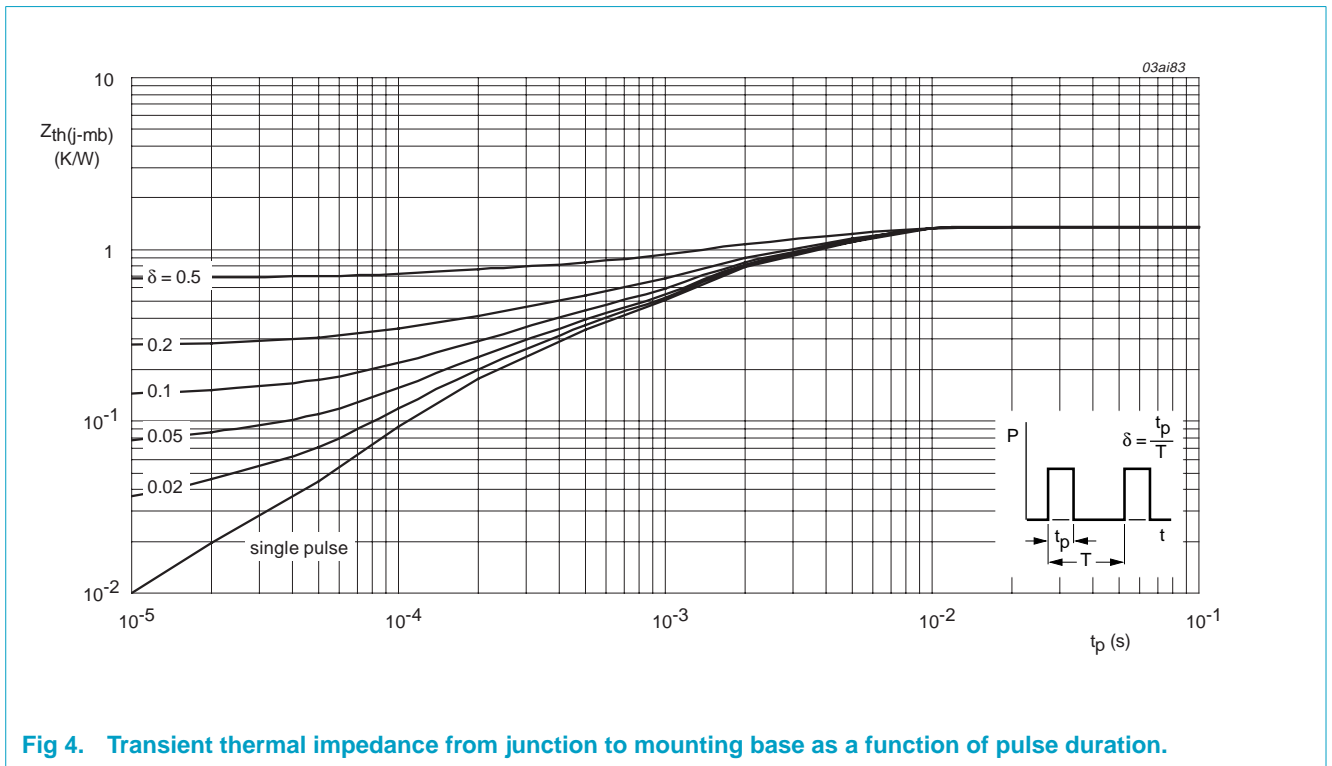
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.35	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT428	SOT428 minimum footprint; mounted on a PCB	-	75	-	K/W
	SOT404 and SOT428	SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

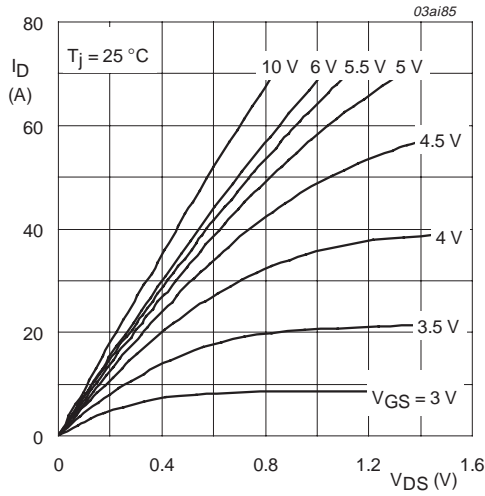
4.1 Transient thermal impedance



5. Characteristics

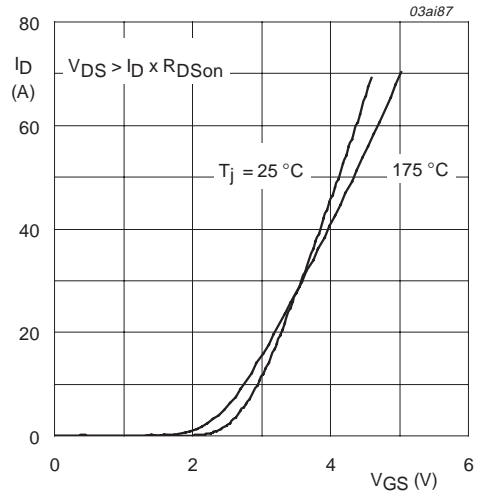
Table 4: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	30	-	-	V
		$T_j = -55\text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9				V
		$T_j = 25\text{ °C}$	1	1.9	2.5	V
		$T_j = 175\text{ °C}$	0.6	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.9	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	0.05	1	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\ \text{V}$; $I_D = 25\ \text{A}$; Figure 7 and 8 $T_j = 25\text{ °C}$	-	15	17.7	m Ω
		$T_j = 175\text{ °C}$	-	24	28.3	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 25\ \text{A}$; Figure 7 and 8	-	11	13	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 50\ \text{A}$; $V_{DD} = 15\ \text{V}$; $V_{GS} = 5\ \text{V}$; Figure 13	-	9.6	-	nC
Q_{gs}	gate-source charge		-	4	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.2	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	920	-	pF
C_{oss}	output capacitance		-	275	-	pF
C_{rss}	reverse transfer capacitance		-	110	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\ \text{V}$; $I_D = 25\ \text{A}$; $V_{GS} = 4.5\ \text{V}$; $R_G = 5.6\ \Omega$	-	12	-	ns
t_r	rise time		-	140	-	ns
$t_{d(off)}$	turn-off delay time		-	10.5	-	ns
t_f	fall time		-	14	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.95	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\ \text{A}$; $dI_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	-	23	-	ns
Q_r	recovered charge		-	12	-	nC



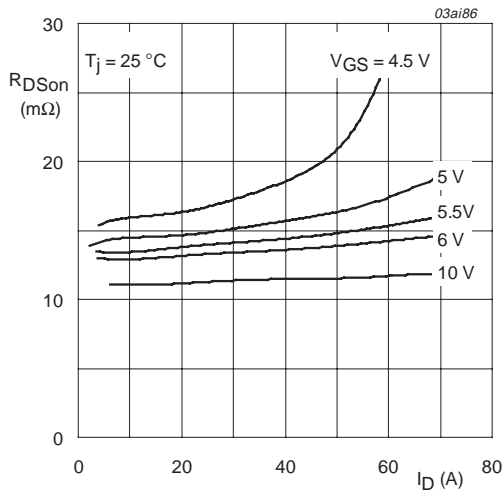
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



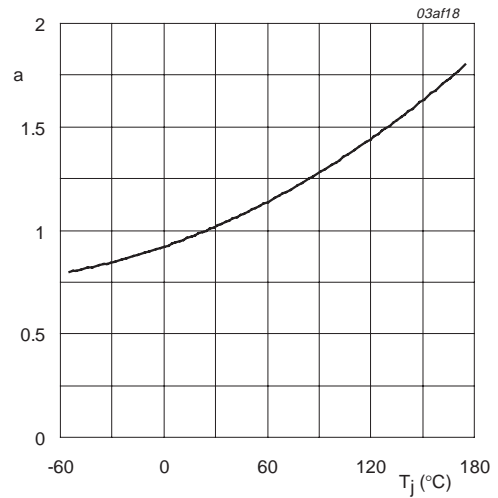
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



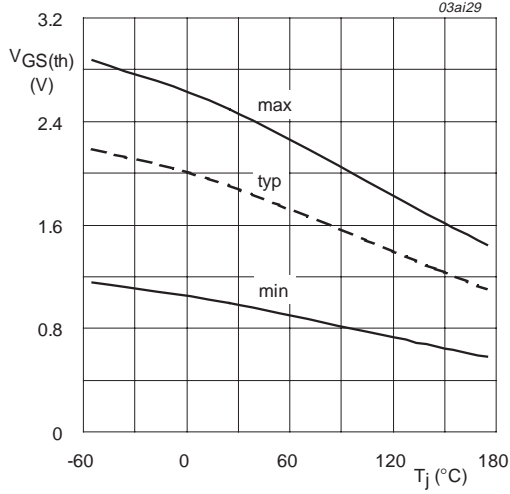
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



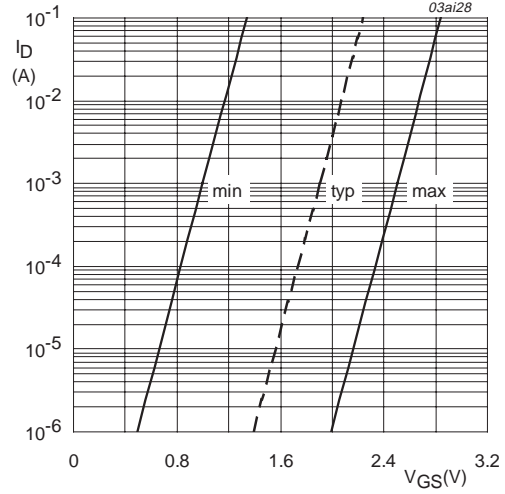
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



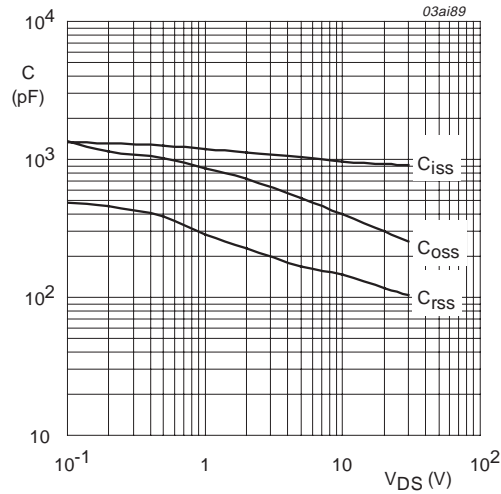
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



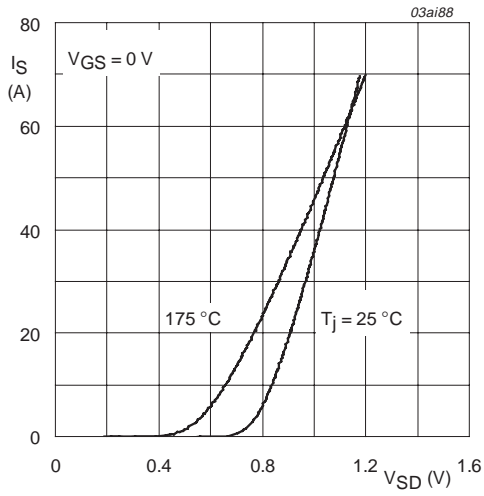
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



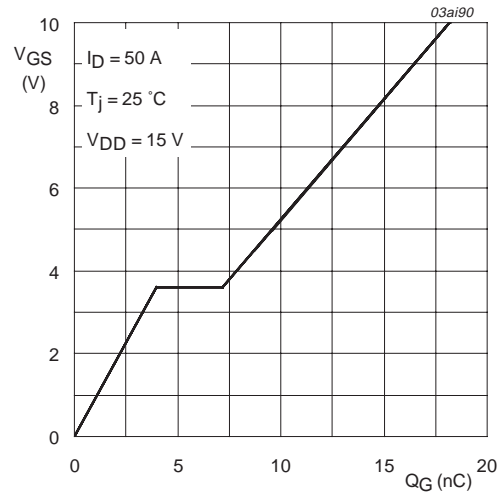
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 50\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



Fig 14. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



Fig 15. SOT404 (D²-PAK)

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428



Fig 16. SOT428 (D-PAK)

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20020614	-	Product data; initial version

8. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Contents

1	Product profile	1
1.1	Description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Limiting values	2
4	Thermal characteristics	4
4.1	Transient thermal impedance	4
5	Characteristics	5
6	Package outline	9
7	Revision history	12
8	Data sheet status	13
9	Definitions	13
10	Disclaimers	13
11	Trademarks	13

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