

PHK04P02T

P-channel vertical D-MOS logic level FET

Rev. 02 — 14 December 2010

Product data sheet

1. Product profile

1.1 General description

Logic level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using vertical D-MOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources
- Suitable for very low gate drive sources voltage

1.3 Applications

- Battery powered applications
- High-speed digital interfaces

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	-	-16	V
I _D	drain current	T _{sp} = 25 °C	-	-	-4.6 6	A
P _{tot}	total power dissipation		-	-	5	W
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = -2.5 V; I _D = -1 A; T _j = 25 °C	-	117	150	mΩ
		V _{GS} = -4.5 V; I _D = -1 A; T _j = 25 °C	-	80	120	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = -4.5 V; I _D = -1 A; V _{DS} = -10 V; T _j = 25 °C	-	1.83	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	SOT96-1 (SO8)	001aaa025
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHK04P02T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-16	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	-16	V
V_{GS}	gate-source voltage		-8	8	V
I_D	drain current	$T_{sp} = 100\text{ °C}$	-	-1.87	A
		$T_{sp} = 25\text{ °C}$	-	-4.66	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed	-	-26.4	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	5	W
		$T_{sp} = 100\text{ °C}$	-	2	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	-4.66	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 5\text{ s}$	-	-26	A

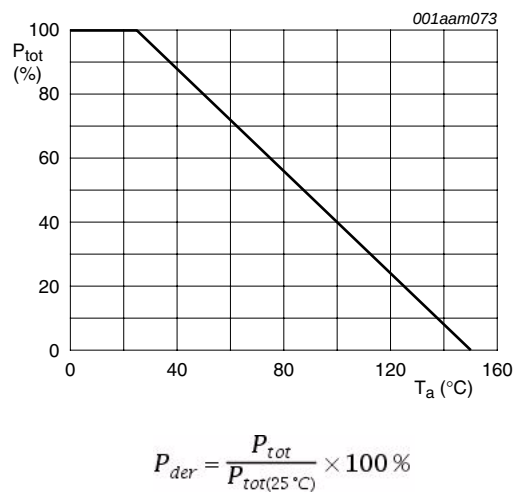


Fig 1. Normalised power dissipation as a function of ambient temperature

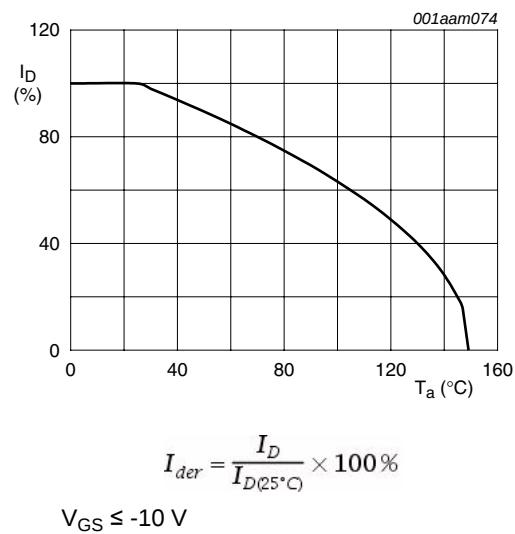
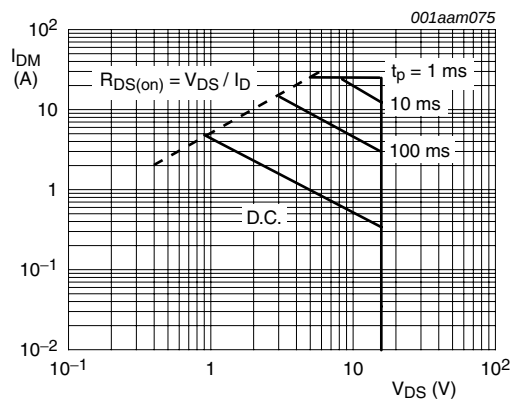


Fig 2. Normalized continuous drain current as a function of ambient temperature



$T_{sp} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on metal clad substrate	-	25	-	K/W

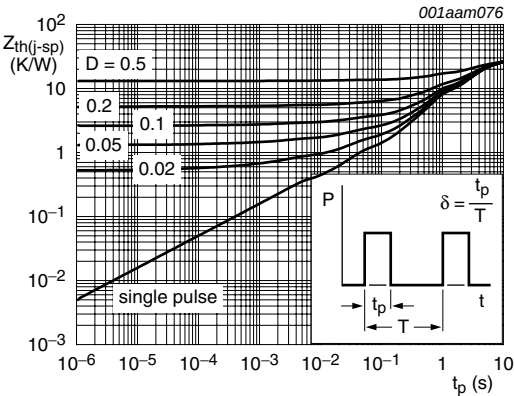


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -10 μA; V _{GS} = 0 V; T _j = 25 °C	-16	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = -1 mA; V _{DS} = V _{GS} ; T _j = 25 °C	-0.4	-0.6	-	V
		I _D = -1 mA; V _{DS} = V _{GS} ; T _j = 150 °C	-0.1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = -13 V; V _{GS} = 0 V; T _j = 25 °C	-	-50	-100	nA
		V _{DS} = -13 V; V _{GS} = 0 V; T _j = 150 °C	-	-13	-100	μA
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
		V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -2.5 V; I _D = -1 A; T _j = 25 °C	-	117	150	mΩ
		V _{GS} = -2.5 V; I _D = -1 A; T _j = 150 °C	-	175	230	mΩ
		V _{GS} = -1.8 V; I _D = -0.5 A; T _j = 25 °C	-	140	180	mΩ
		V _{GS} = -4.5 V; I _D = -1 A; T _j = 25 °C	-	80	120	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = -1 A; V _{DS} = -10 V; V _{GS} = -4.5 V; T _j = 25 °C	-	7.2	-	nC
Q _{GS}	gate-source charge		-	1.7	-	nC
Q _{GD}	gate-drain charge		-	1.83	-	nC
C _{iss}	input capacitance	V _{DS} = -13 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C	-	528	-	pF
C _{oss}	output capacitance		-	200	-	pF
C _{rss}	reverse transfer capacitance		-	57	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; R _L = 10 Ω; V _{GS} = -8 V; R _{G(ext)} = 6 Ω; T _j = 25 °C; I _D = -1 A	-	2	-	ns
t _r	rise time		-	4.5	-	ns
t _{d(off)}	turn-off delay time		-	45	-	ns
t _f	fall time		-	20	-	ns
g _{fs}	transfer conductance	V _{DS} = -13 V; I _D = -1 A; T _j = 25 °C	1.5	4.5	-	S
Source-drain diode						
V _{SD}	source-drain voltage	I _S = -0.62 A; V _{GS} = 0 V; T _j = 25 °C	-	-0.62	-1.3	V
t _{rr}	reverse recovery time	I _S = -0.5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = -12.8 V; T _j = 25 °C	-	75	-	ns
Q _r	recovered charge		-	69	-	nC

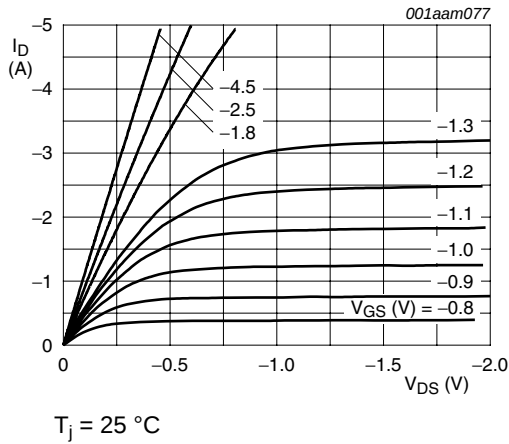


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

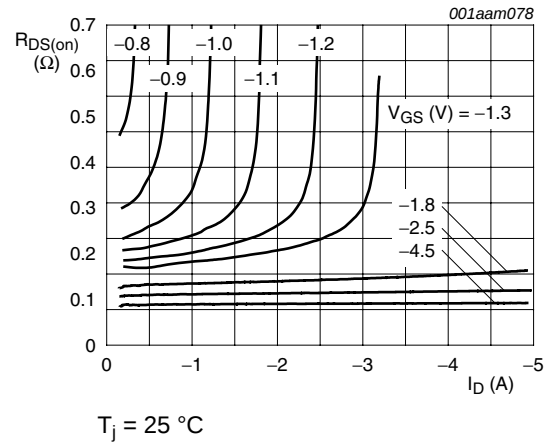


Fig 6. Drain-source on-state resistance as a function of drain current; typical values

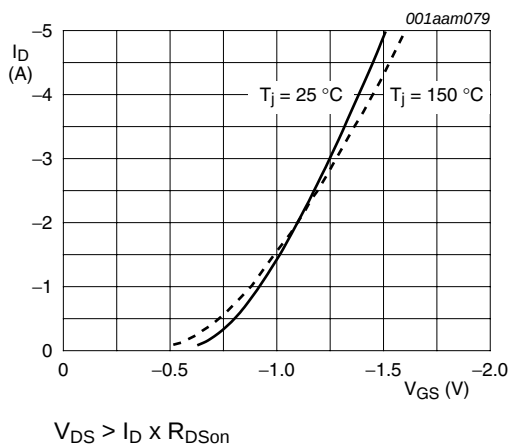


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

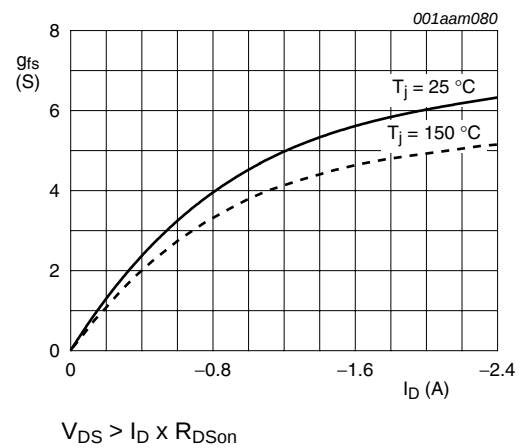


Fig 8. Forward transconductance as a function of drain current; typical values

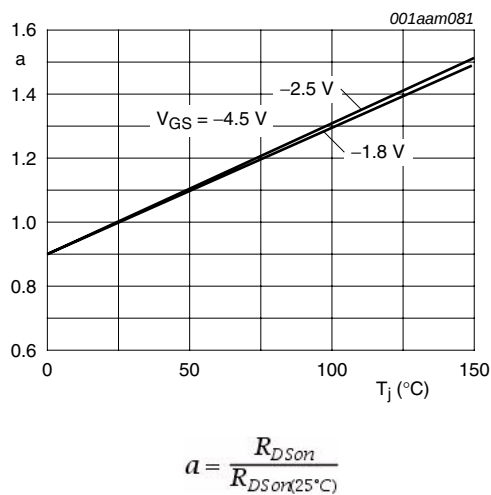


Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature

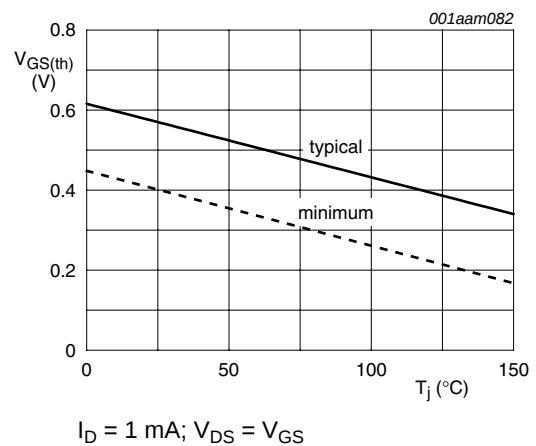


Fig 10. Gate-source threshold voltage as a function of junction temperature

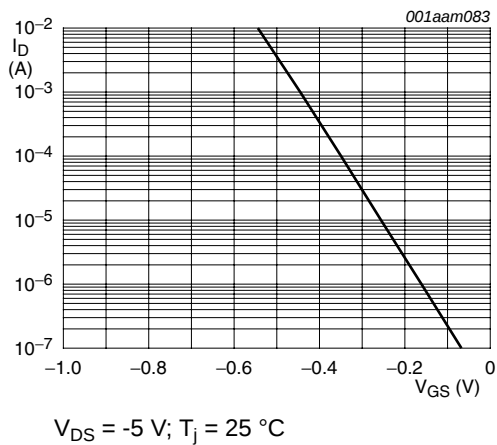


Fig 11. Sub-threshold drain current as a function of gate-source voltage

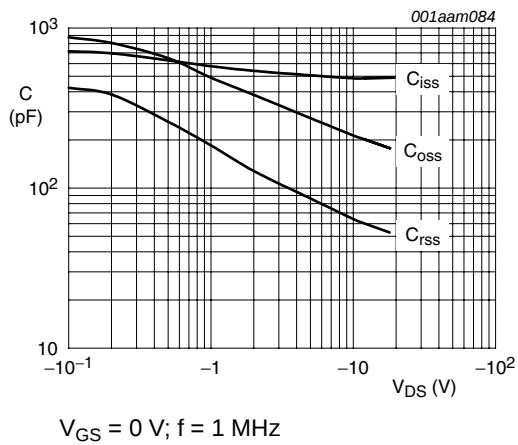


Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

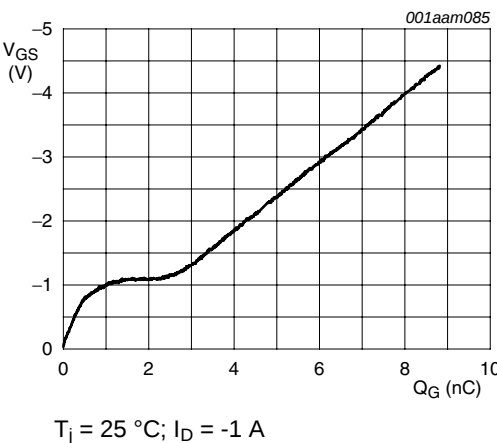


Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values

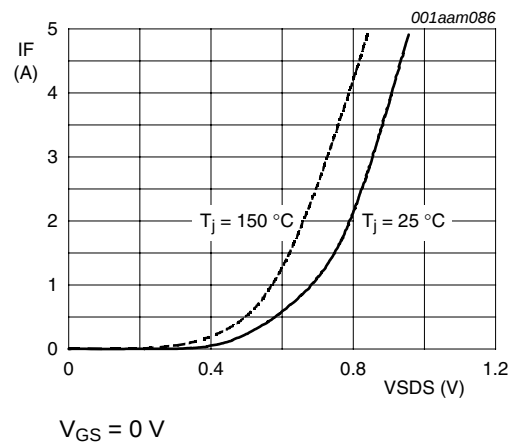


Fig 14. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

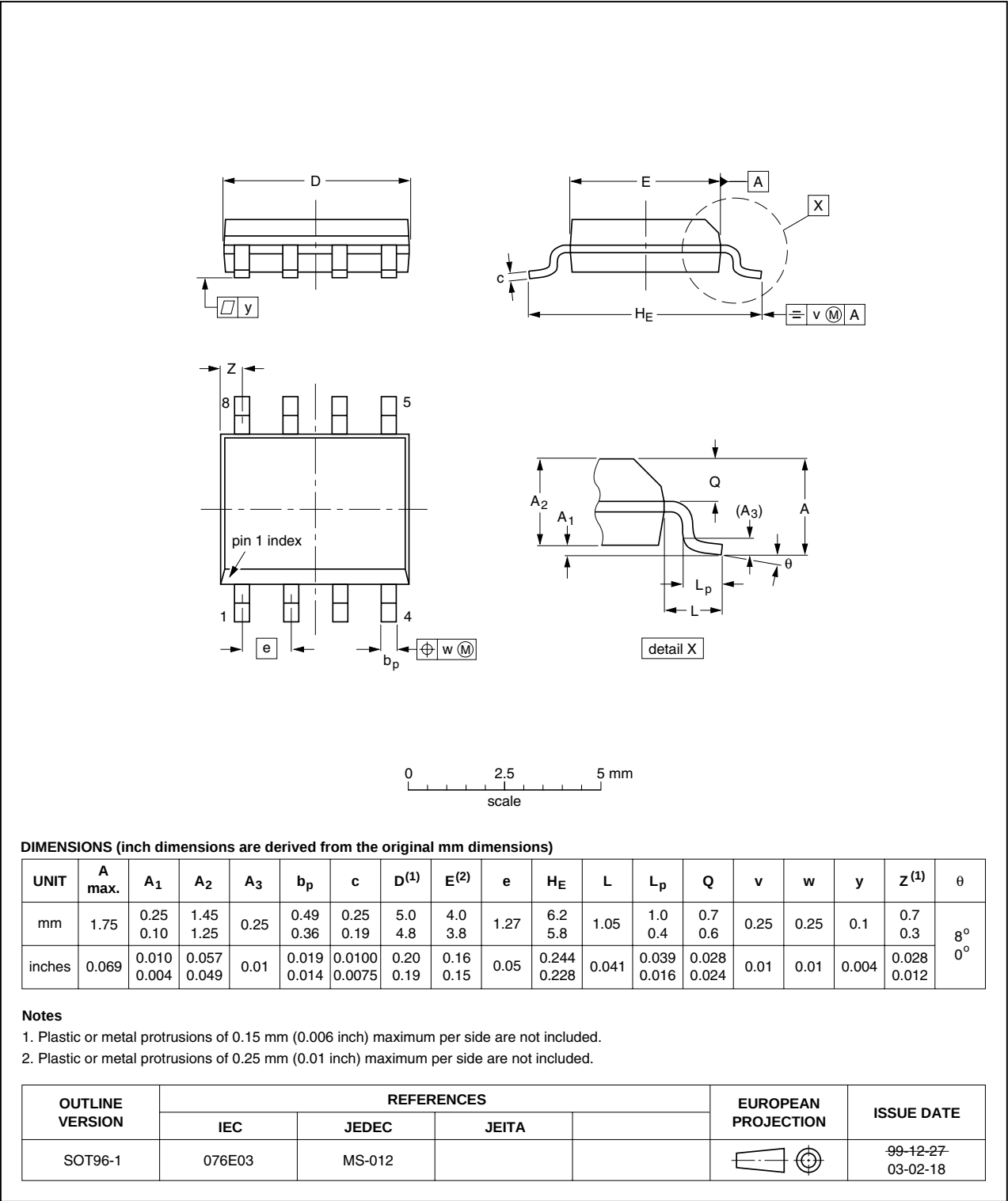


Fig 15. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK04P02T v.2	20101214	Product data sheet	-	PHK04P02T v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PHK04P02T v.1	20020501	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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