

PHK12NQ10T

TrenchMOS™ standard level FET

Rev. 01 — 15 September 2003

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Surface mounting package
- Low on-state resistance.

1.3 Applications

- DC-to-DC converter primary side
- Portable equipment applications.

1.4 Quick reference data

- $V_{DS} \leq 100 \text{ V}$
- $I_D \leq 11.6 \text{ A}$
- $P_{tot} \leq 8.9 \text{ W}$
- $R_{DSon} \leq 28 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT96-1 (SO8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBK187</p>	
4	gate (g)		
5,6,7,8	drain (d)		

SOT96-1 (SO8)

3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PHK12NQ10T	SO8	Plastic small outline package; 8 leads.	SOT96-1

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	11.6	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	7.4	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	48	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	8.9	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

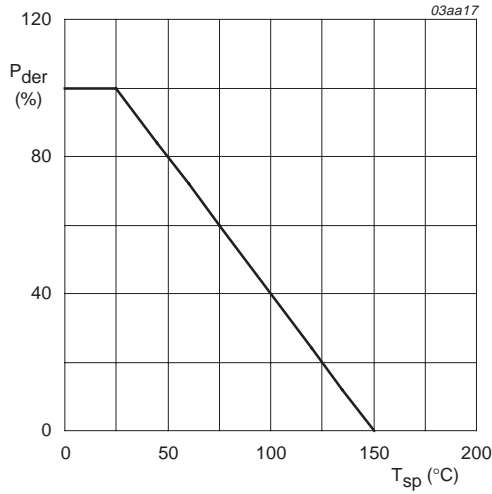
Source-drain diode

I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	12	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	48	A

Avalanche ruggedness

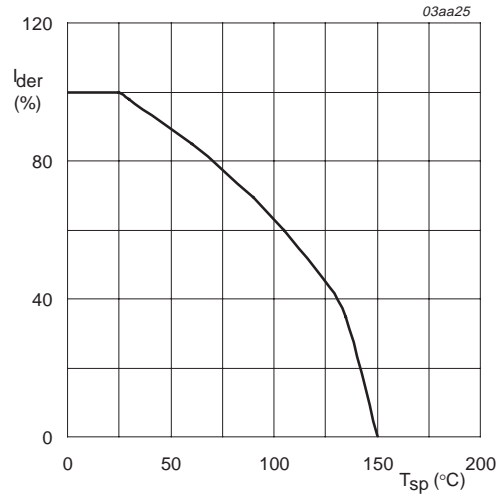
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 11.5\text{ A}$; $t_p = 0.1\text{ ms}$; $V_{DD} \leq 100\text{ V}$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$	-	65	mJ
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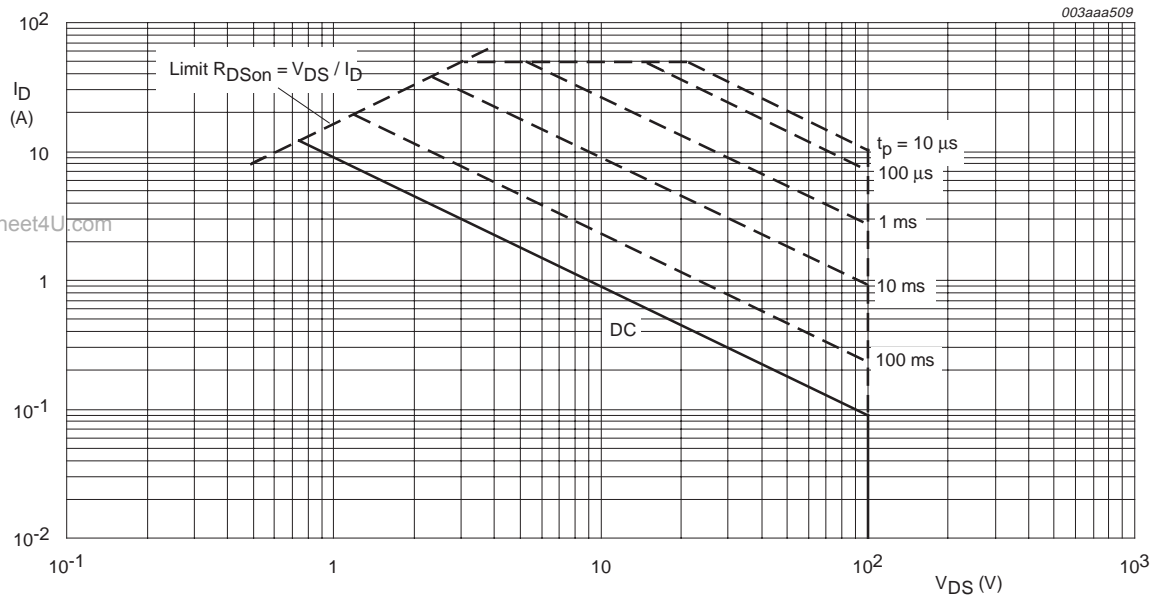
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	15	K/W

5.1 Transient thermal impedance

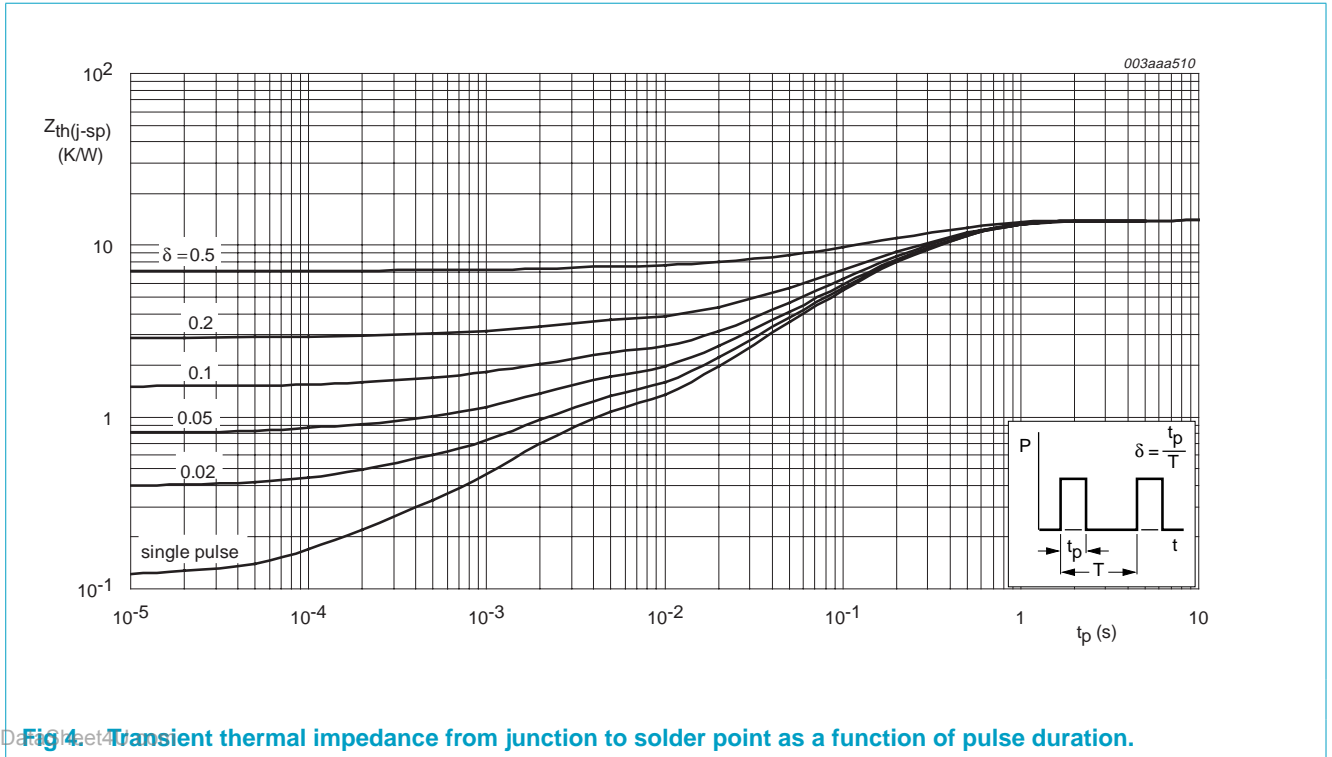
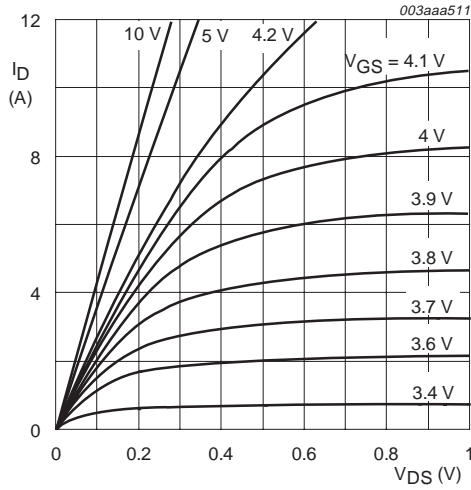


Fig 4 Transient thermal impedance from junction to solder point as a function of pulse duration.

6. Characteristics

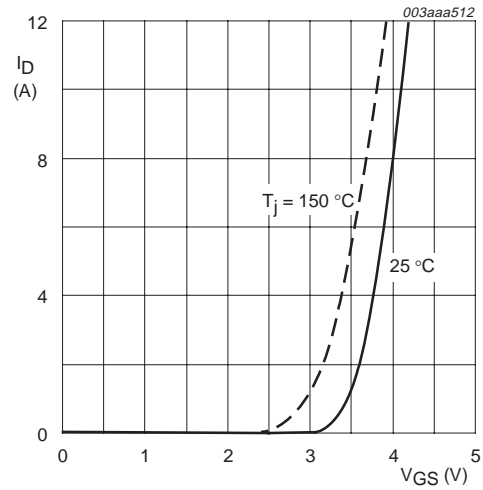
Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	100	-	-	V
		$T_j = -55\text{ °C}$	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 150\text{ °C}$	1.2	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 100\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	-	1	μA
		$T_j = 150\text{ °C}$	-	-	100	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 6\ \text{A}$; Figure 7 and 8 $T_j = 25\text{ °C}$	-	23.7	28	m Ω
		$T_j = 150\text{ °C}$	-	52.1	61.6	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 12\ \text{A}$; $V_{DD} = 50\ \text{V}$; $V_{GS} = 10\ \text{V}$; Figure 13	-	35	-	nC
Q_{gs}	gate-source charge		-	7.8	-	nC
Q_{gd}	gate-drain (Miller) charge		-	9	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	1965	-	pF
C_{oss}	output capacitance		-	260	-	pF
C_{rss}	reverse transfer capacitance		-	90	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 50\ \text{V}$; $I_D = 6\ \text{A}$; $V_{GS} = 10\ \text{V}$; $R_G = 6\ \Omega$	-	23	-	ns
t_r	rise time		-	21	-	ns
$t_{d(off)}$	turn-off delay time		-	52	-	ns
t_f	fall time		-	11	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 12\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.83	1.0	V
t_{rr}	reverse recovery time	$I_S = 12\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	-	86	-	ns
Q_r	recovered charge		-	120	-	nC



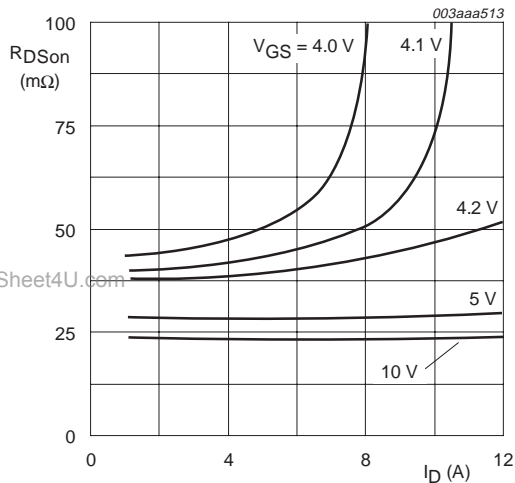
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



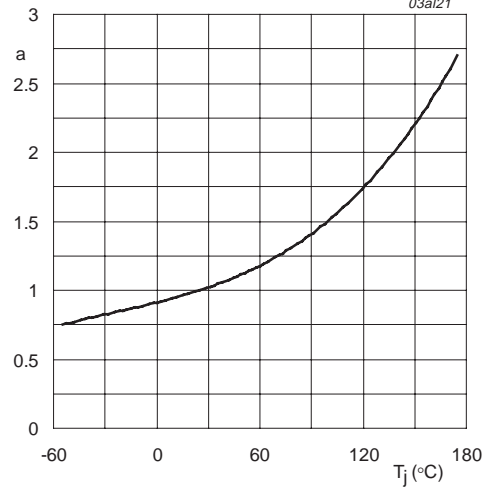
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



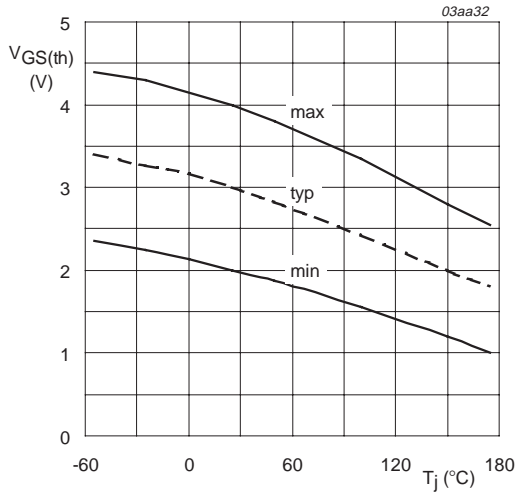
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



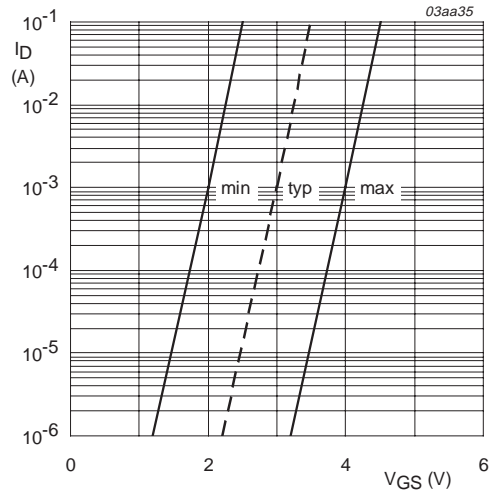
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



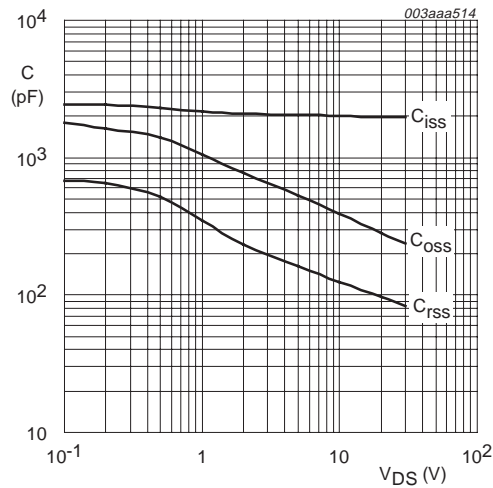
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

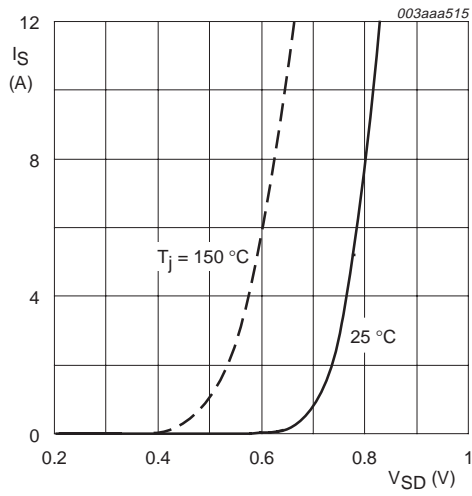
Fig 10. Sub-threshold drain current as a function of gate-source voltage.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

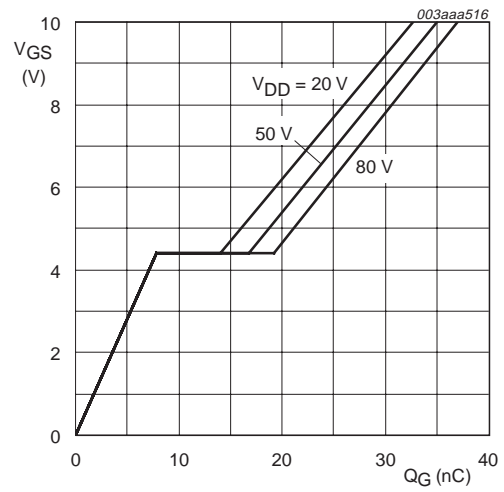
Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

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$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 12\text{ A}$; $V_{DD} = 20\text{ V}$, 50 V and 80 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

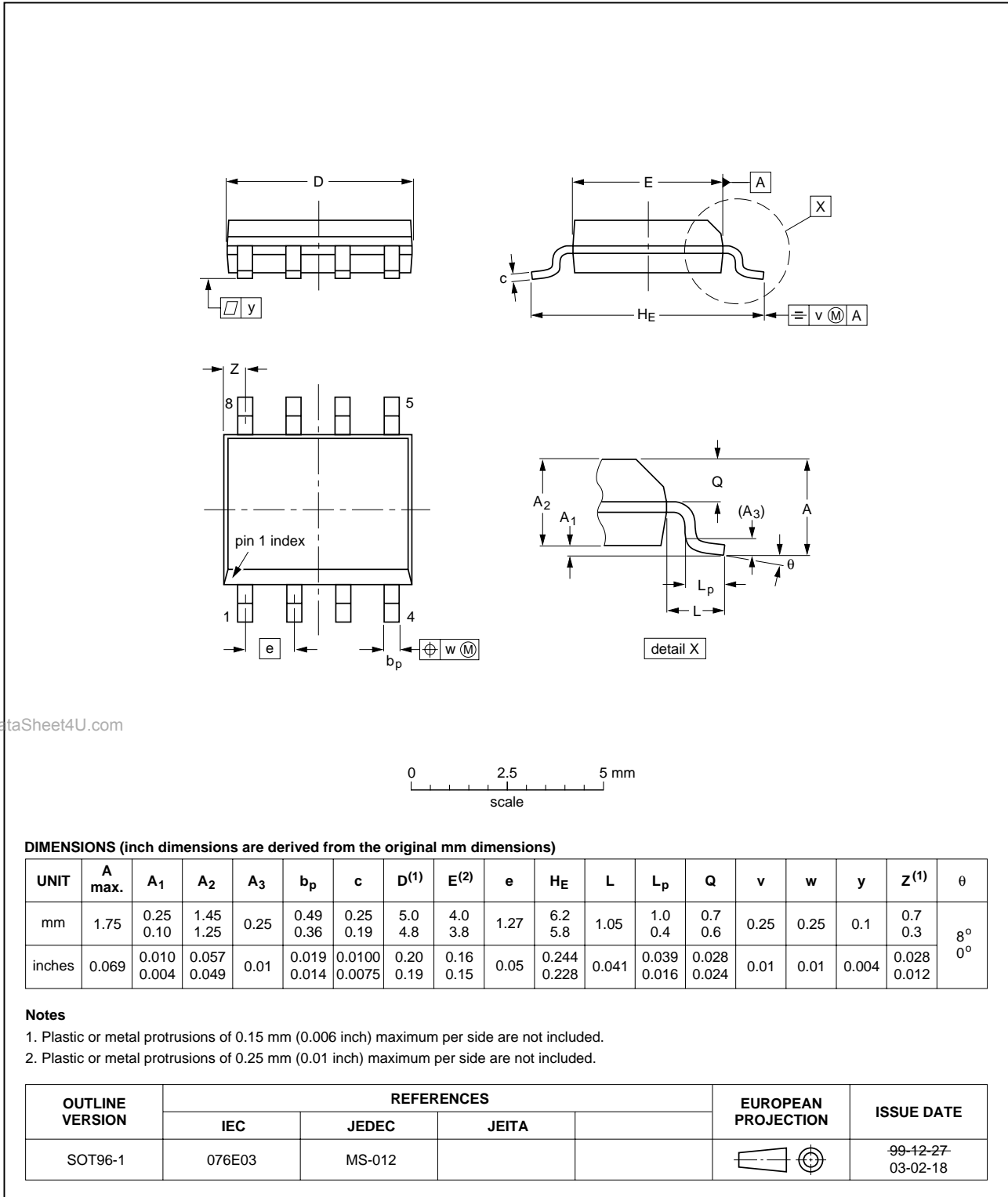


Fig 14. SOT96-1 (SO8).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20030915	-	Product data (9397 750 11949).

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Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

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