

DATA SHEET

PHN1013

N-channel enhancement mode
MOS transistor

Objective specification
File under Discrete Semiconductors, SC13b

1997 Jun 20

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MOS transistor

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FEATURES

- Very low on-state resistance.

APPLICATIONS

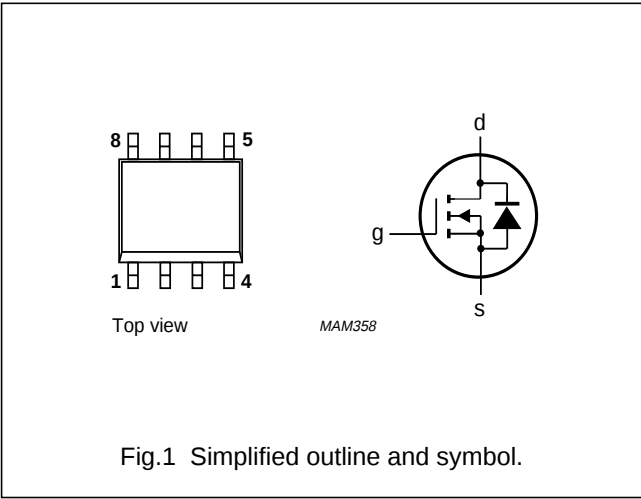
- DC to DC converters
- General purpose switching applications.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s	source
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor using 'trench' technology, in an 8-pin plastic SOT96-1 (SO8) package.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		30	V
I_D	drain current (DC)		10	A
P_{tot}	total power dissipation		2.5	W
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$	13.5	m Ω
T_j	junction temperature		150	$^{\circ}\text{C}$

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	30	V
V_{DG}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	–	30	V
V_{GS}	gate-source voltage		–	± 20	V
I_D	drain current (DC)	$T_{amb} = 25\text{ }^{\circ}\text{C}; t_p \leq 10\text{ s}$	–	10	A
		$T_{amb} = 70\text{ }^{\circ}\text{C}; t_p \leq 10\text{ s}$	–	8	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	–	50	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	–	2.5	W
		$T_{amb} = 70\text{ }^{\circ}\text{C}$	–	1.6	W
T_{stg}	storage temperature		–55	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–55	+150	$^{\circ}\text{C}$

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	minimum footprint; $t_p \leq 10$ s; note 1	50	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 250$ μ A	30	–	–	V
		$V_{GS} = 0$; $I_D = 250$ μ A; $T_j = -55$ °C	27	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 250$ μ A	2.1	3	4	V
		$V_{DS} = V_{GS}$; $I_D = 250$ μ A; $T_j = 150$ °C	1.4	–	–	V
		$V_{DS} = V_{GS}$; $I_D = 250$ μ A; $T_j = -55$ °C	–	–	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30$ V; $V_{GS} = 0$	–	0.05	10	μ A
		$V_{DS} = 30$ V; $V_{GS} = 0$; $T_j = 150$ °C	–	–	500	μ A
I_{GSS}	gate leakage current	$V_{GS} = \pm 10$ V; $V_{DS} = 0$	–	10	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A	–	11	13.5	m Ω
		$V_{GS} = 10$ V; $I_D = 10$ A; $T_j = 150$ °C	–	–	26	m Ω

DYNAMIC CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	forward transconductance	$V_{DS} = 25$ V; $I_D = 10$ A	4	8	–	S
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = 25$ V; $f = 1$ MHz	–	1700	2200	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = 25$ V; $f = 1$ MHz	–	325	450	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = 25$ V; $f = 1$ MHz	–	214	260	pF
Q_G	total gate charge	$V_{GS} = 5$ V; $V_{DD} = 24$ V; $I_D = 10$ A	–	27	–	nC
Q_{GS}	gate-source charge	$V_{GS} = 5$ V; $V_{DD} = 24$ V; $I_D = 10$ A	–	3.5	–	nC
Q_{GD}	gate-drain charge	$V_{GS} = 5$ V; $V_{DD} = 24$ V; $I_D = 10$ A	–	15	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	$V_{GS} = 5$ V; $V_{DD} = 25$ V; $I_D = 10$ A; $R_{gen} = 10$ Ω resistive load	–	25	40	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = 5$ V; $V_{DD} = 25$ V; $I_D = 10$ A; $R_{gen} = 10$ Ω resistive load	–	90	130	ns
t_r	rise time	$V_{GS} = 5$ V; $V_{DD} = 25$ V; $I_D = 10$ A; $R_{gen} = 10$ Ω resistive load	–	75	125	ns
t_f	fall time	$V_{GS} = 5$ V; $V_{DD} = 25$ V; $I_D = 10$ A; $R_{gen} = 10$ Ω resistive load	–	35	50	ns

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
I_{DR}	continuous reverse drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}; t_p \leq 10\text{ s}$	–	10	A
I_{DRM}	pulsed reverse drain current		–	50	A
V_{SD}	source-drain diode forward voltage	$I_F = 10\text{ A}; V_{GS} = 0$	0.95	1.2	V
		$I_F = 50\text{ A}; V_{GS} = 0$	1	–	V
t_{rr}	reverse recovery time	$I_F = 10\text{ A}; di/dt = -100\text{ A}/\mu\text{s};$ $V_{GS} = -10\text{ V}; V_R = 25\text{ V}$	50	–	ns
Q_{rr}	reverse recovery charge	$I_F = 10\text{ A}; di/dt = -100\text{ A}/\mu\text{s};$ $V_{GS} = -10\text{ V}; V_R = 25\text{ V}$	0.1	–	μC

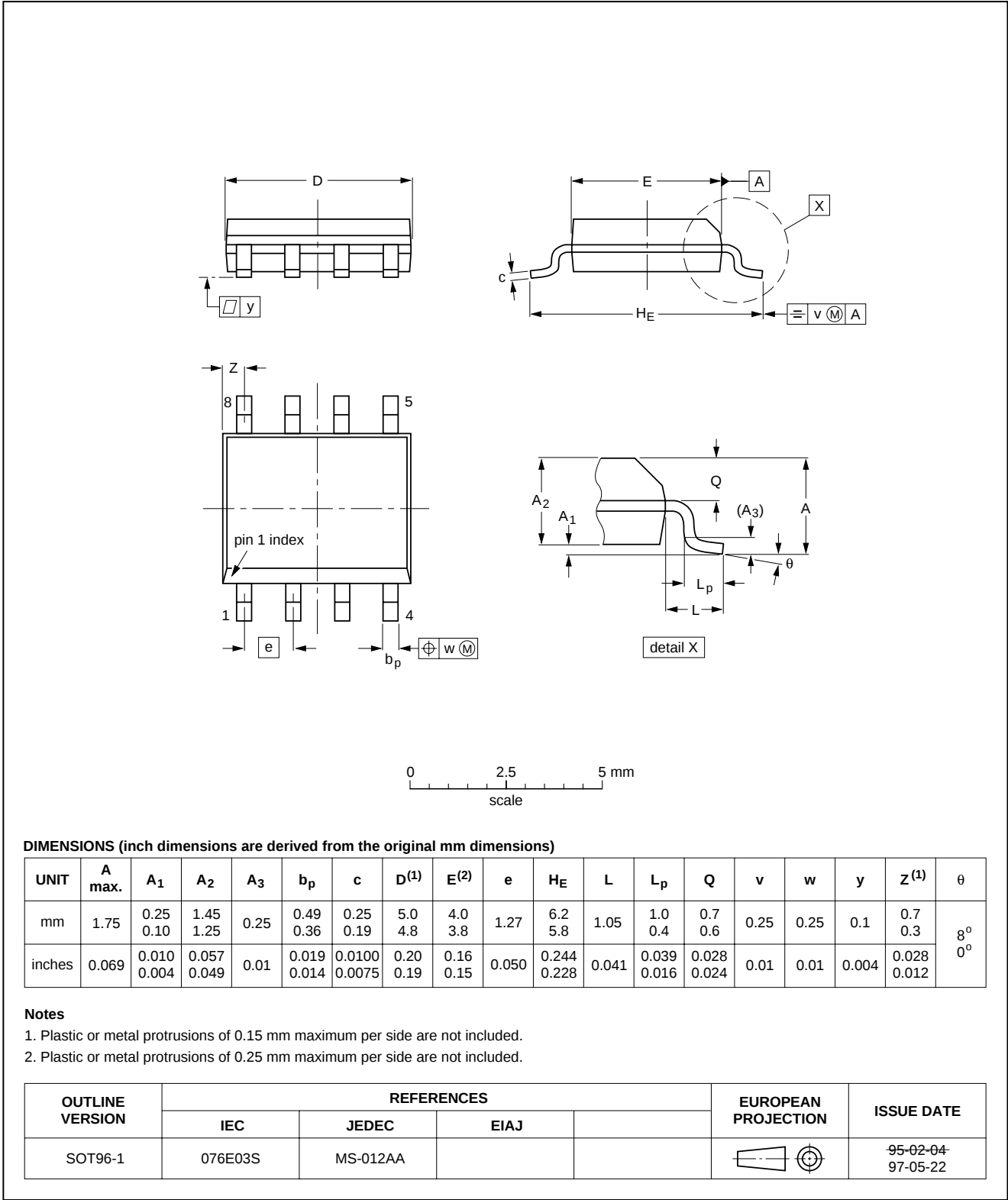
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PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Printed in The Netherlands

137107/00/01/pp8

Date of release: 1997 Jun 20

Document order number: 9397 750 02452

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