

# TrenchMOS™ transistor

## Standard level FET

PHT6N03T

### GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology, the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in DC-DC converters and general purpose switching applications.

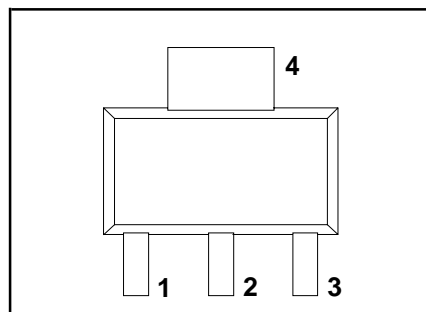
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	30	V
$I_D$	Drain current (DC) $T_{sp} = 25\text{ °C}$	12.8	A
	Drain current (DC) $T_{amb} = 25\text{ °C}$	5.9	A
$P_{tot}$	Total power dissipation	8.3	W
$T_j$	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	30	mΩ

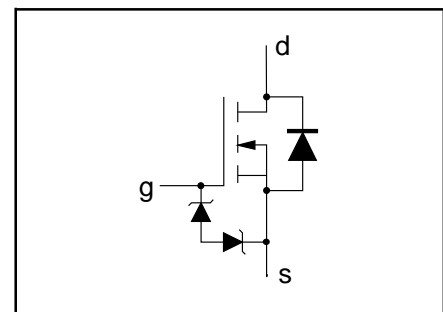
### PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

### PIN CONFIGURATION



### SYMBOL



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	30	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
$I_D$	Drain current (DC)	$T_{sp} = 25\text{ °C}$ $T_{amb} = 25\text{ °C}$	-	12.8	A
		$T_{sp} = 100\text{ °C}$ $T_{amb} = 100\text{ °C}$	-	9	A
$I_{DM}$	Drain current (pulse peak value)	$T_{sp} = 25\text{ °C}$ $T_{amb} = 25\text{ °C}$	-	51.2	A
		$T_{sp} = 100\text{ °C}$ $T_{amb} = 100\text{ °C}$	-	23.6	A
$P_{tot}$	Total power dissipation	$T_{sp} = 25\text{ °C}$ $T_{amb} = 25\text{ °C}$	-	8.3	W
		$T_{sp} = 100\text{ °C}$ $T_{amb} = 100\text{ °C}$	-	1.8	W
$T_{stg}, T_j$	Storage & operating temperature	-	-55	150	°C

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j-amb}$	Thermal resistance junction to ambient	Mounted on PCB of Fig.19	-	70	K/W

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### ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

### STATIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}; T_j = -55^\circ\text{C}$	30 27	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	2.0 1.0	3.0 -	4.0 -	V V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; T_j = -55^\circ\text{C}$	-	-	4.4	$\mu\text{A}$
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}; T_j = 150^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	$V_G = \pm 1\text{ mA}; T_j = 150^\circ\text{C}$	-	-	500	$\mu\text{A}$
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 3.2\text{ A}; T_j = 150^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
			16	-	20	$\mu\text{A}$
			-	24	30	mΩ
			-	-	51	mΩ

### DYNAMIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{fs}$	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 5.9\text{ A}$	5	10	-	S
$Q_{g(tot)}$	Total gate charge	$I_D = 5.9\text{ A}; V_{DD} = 24\text{ V}; V_{GS} = 10\text{ V}$	-	22.5	-	nC
$Q_{gs}$	Gate-source charge		-	4.5	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	13.5	-	nC
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	1500	2000	pF
$C_{oss}$	Output capacitance		-	370	470	pF
$C_{rss}$	Feedback capacitance		-	170	250	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 5.9\text{ A};$	-	16	22	ns
$t_r$	Turn-on rise time	$V_{GS} = 10\text{ V}; R_G = 5\ \Omega$	-	30	60	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	35	50	ns
$t_f$	Turn-off fall time		-	25	38	ns
$L_d$	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

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### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

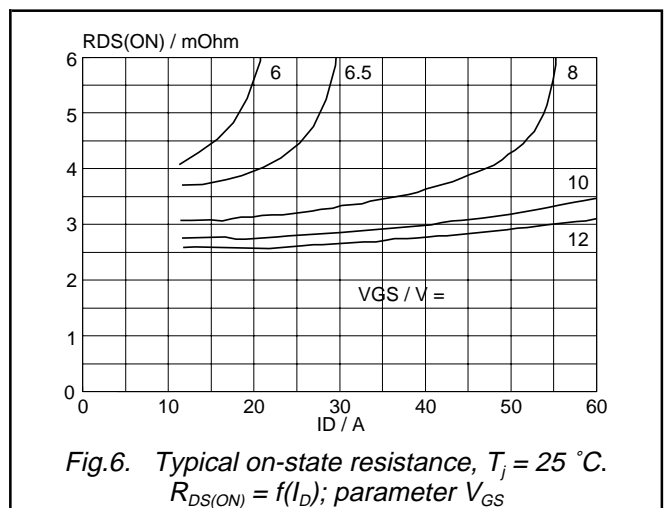
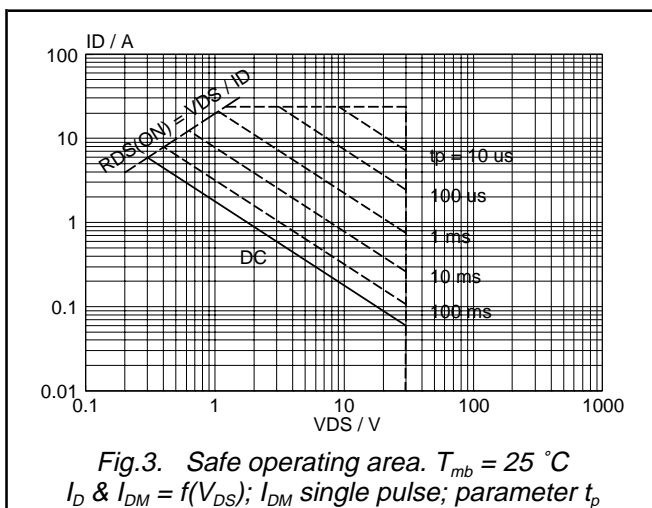
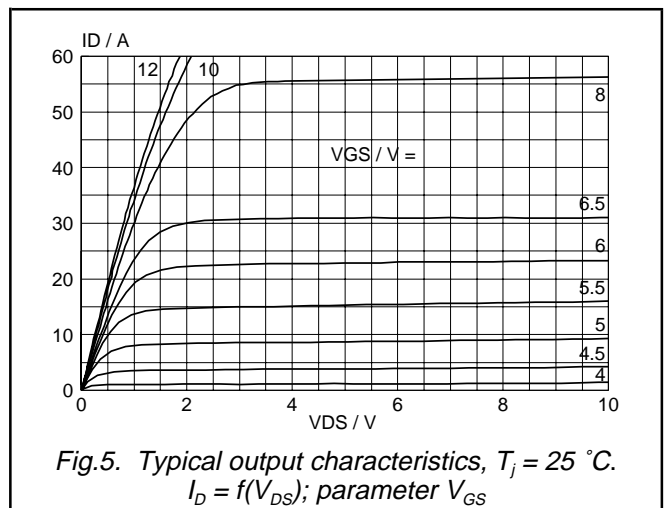
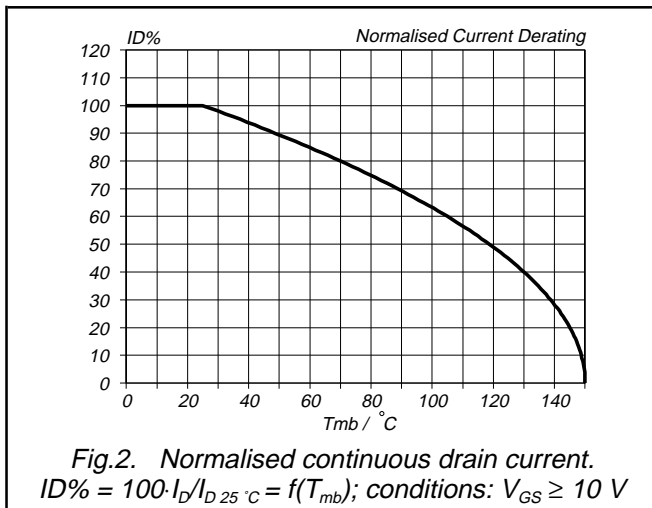
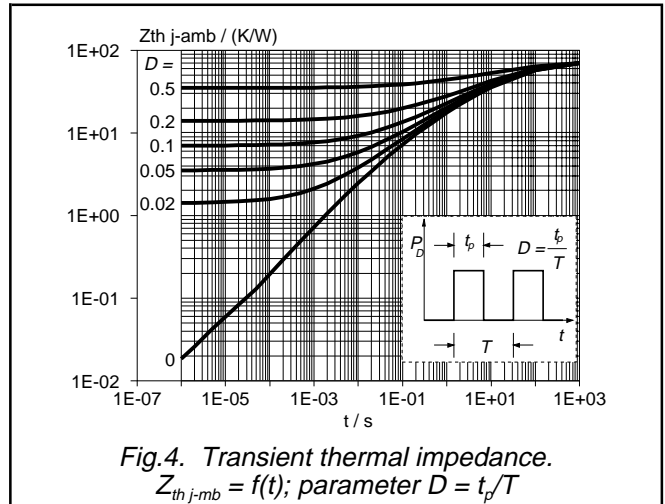
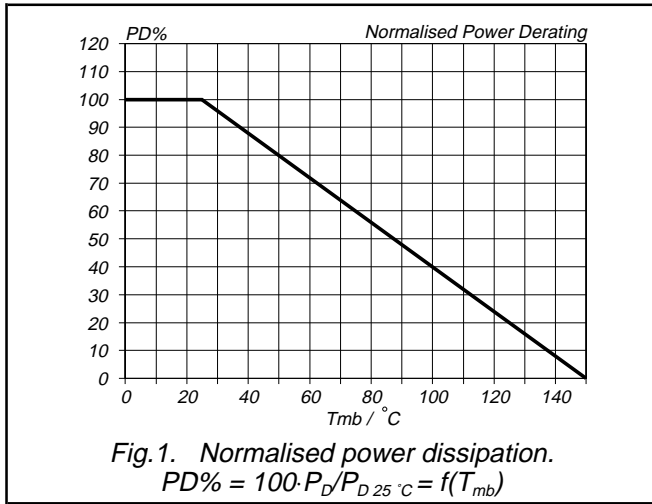
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current		-	-	6.2	A
$I_{DRM}$	Pulsed reverse drain current		-	-	24.8	A
$V_{SD}$	Diode forward voltage	$I_F = 3.2\text{ A}; V_{GS} = 0\text{ V}$	-	0.75	1.2	V
		$I_F = 5.9\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	-	
$t_{rr}$	Reverse recovery time	$I_F = 5.9\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	115	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = -10\text{ V}; V_R = 25\text{ V}$	-	0.3	-	$\mu\text{C}$

### AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 5.9\text{ A}; V_{DD} \leq 25\text{ V};$ $V_{GS} = 10\text{ V}; R_{GS} = 50\ \Omega; T_{sp} = 25\ ^\circ\text{C}$	-	-	60	mJ

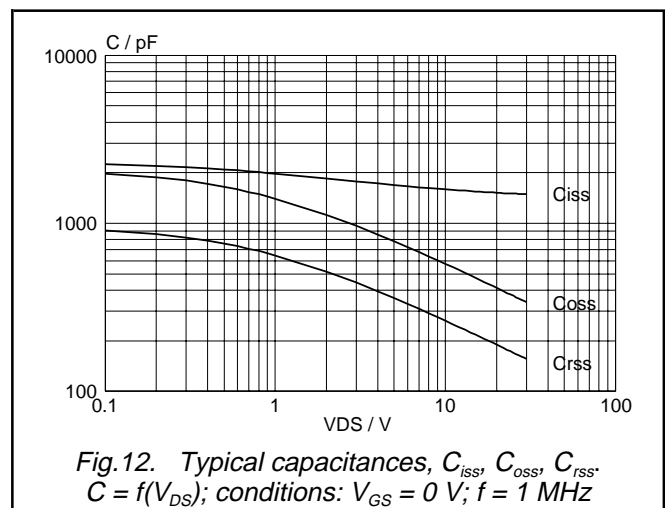
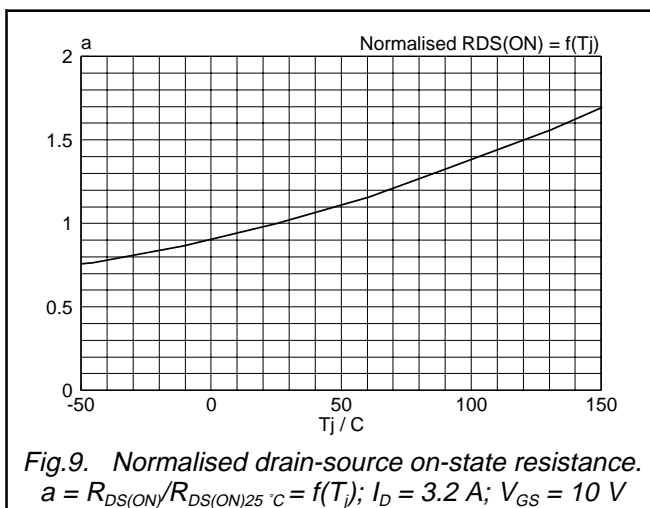
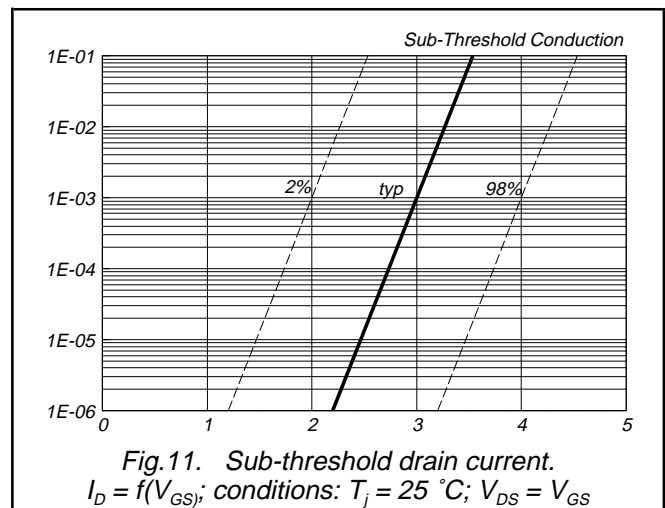
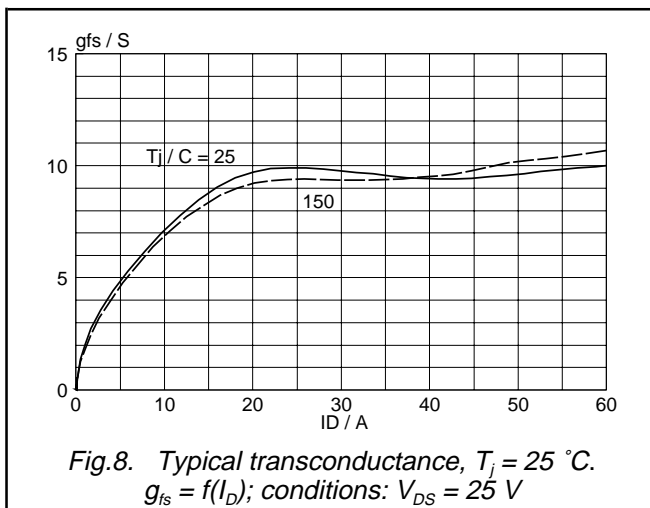
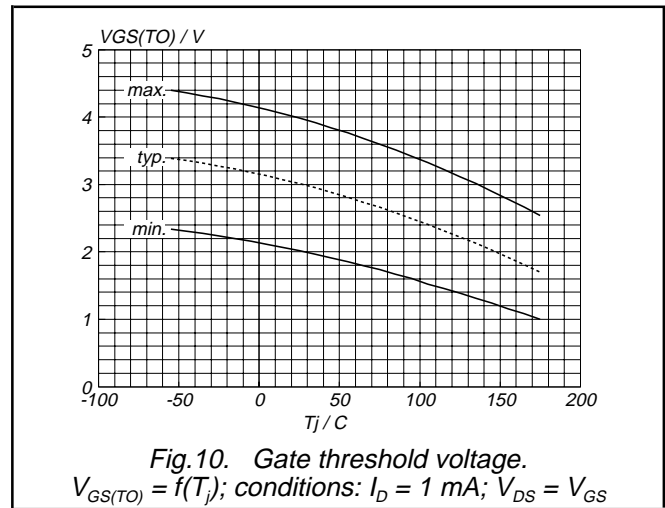
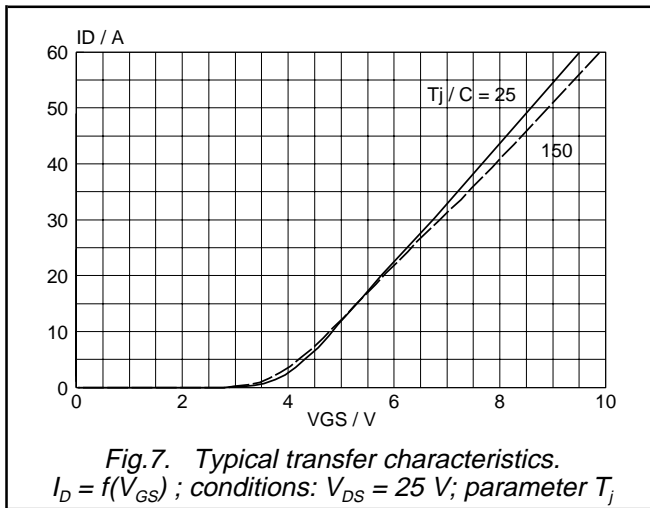
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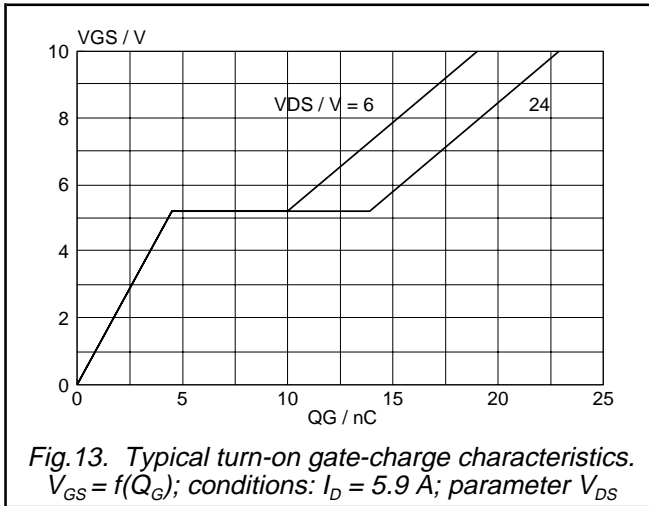


Fig. 13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 5.9$  A; parameter  $V_{DS}$

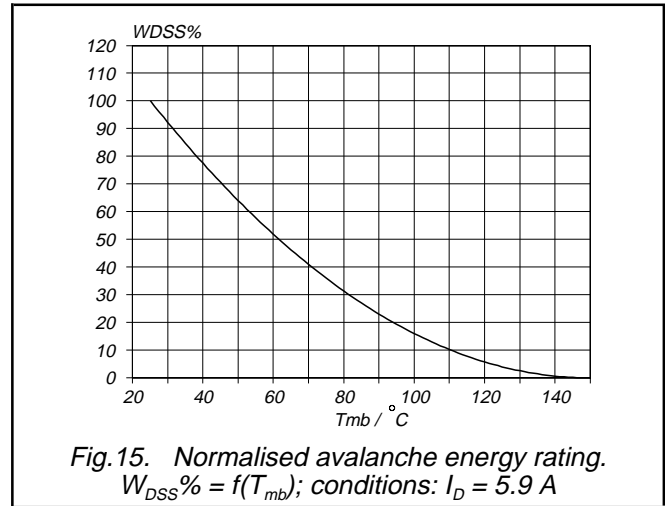


Fig. 15. Normalised avalanche energy rating.  
 $W_{DSS}\% = f(T_{mb})$ ; conditions:  $I_D = 5.9$  A

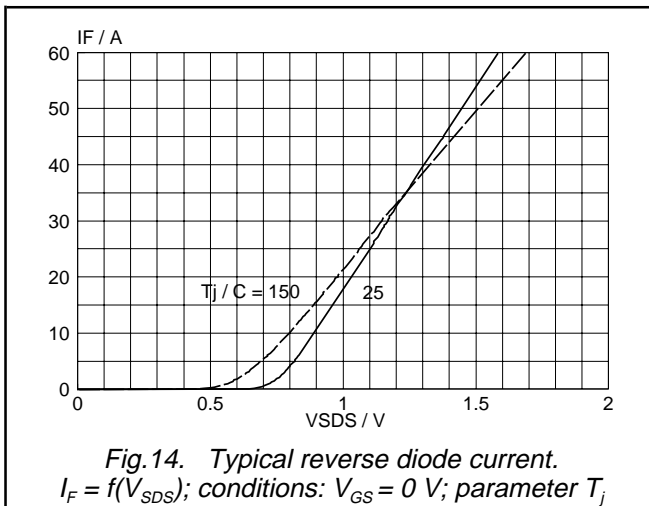


Fig. 14. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0$  V; parameter  $T_j$

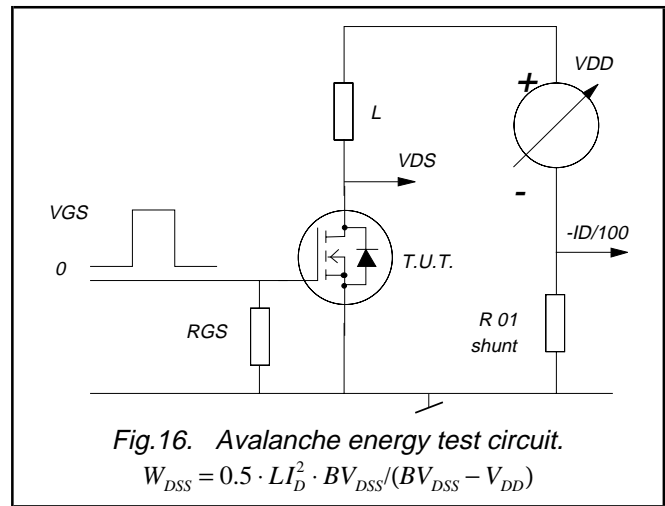


Fig. 16. Avalanche energy test circuit.  
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

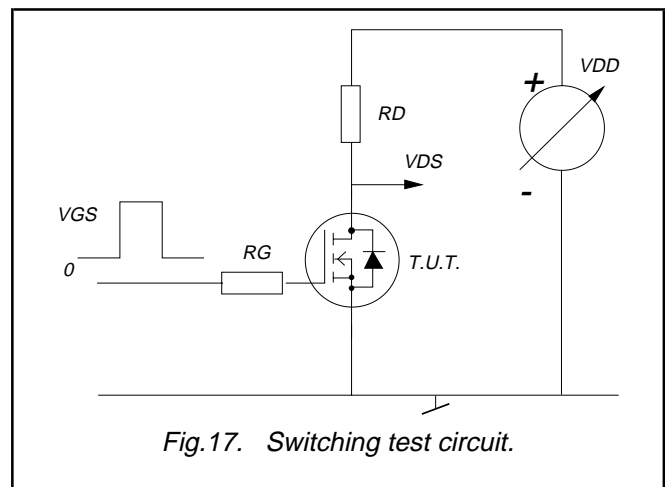


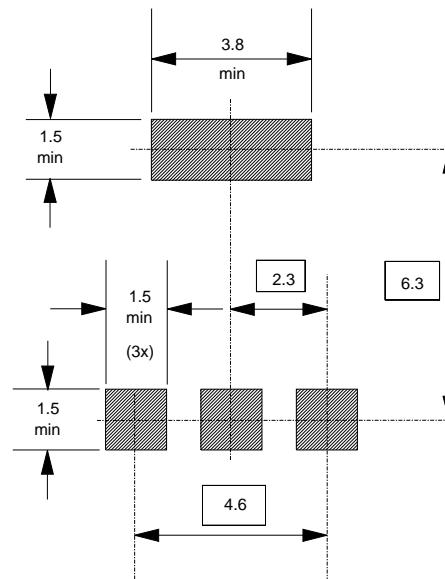
Fig. 17. Switching test circuit.

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**MOUNTING INSTRUCTIONS**

*Dimensions in mm.*



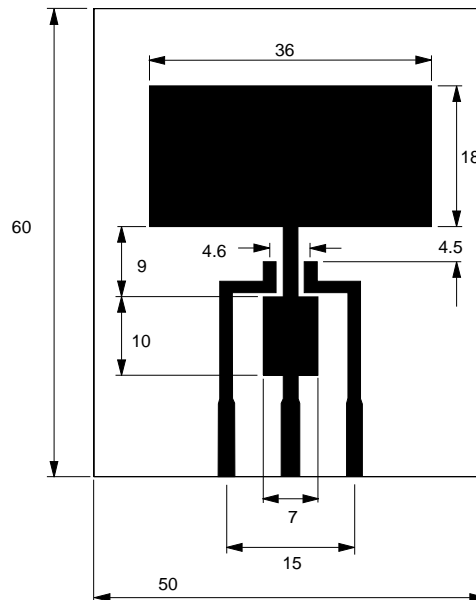
*Fig.18. soldering pattern for surface mounting SOT223.*

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**PRINTED CIRCUIT BOARD**

*Dimensions in mm.*



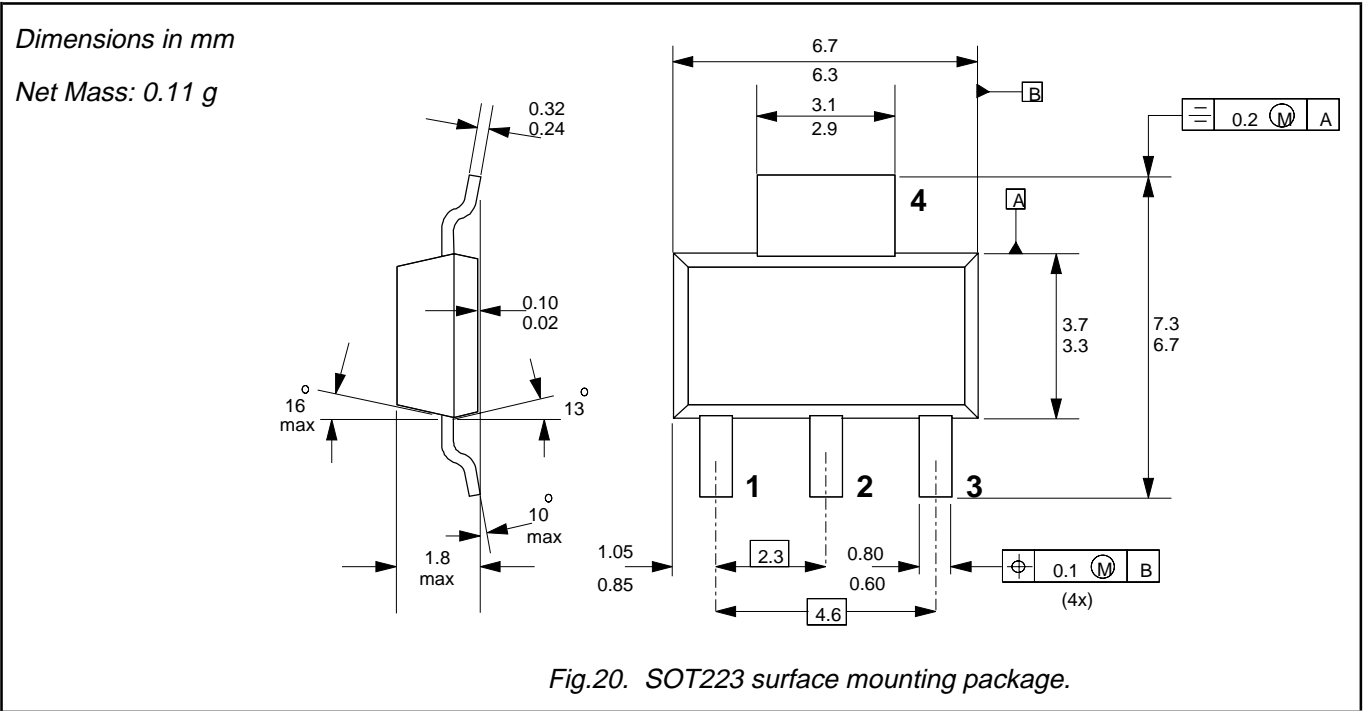
*Fig.19. PCB for thermal resistance and power rating for SOT223.  
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*



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**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".

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### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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