XWAY™ PHY

Ethernet Physical Layer Devices

XWAY™ PHY11G

Single Port Gigabit Ethernet PHY (10/100/1000 Mbit/s)
PEF 7071, Version 1.5

User's Manual

Hardware Description
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XWAY™ PHY11G, Single Port Gigabit Ethernet PHY (10/100/1000 Mbit/s)

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1 Introduction

This document specifies the functionality of the Lantiq XWAY™ PHY11G Version 1.5 Gigabit Ethernet (GbE) transceiver integrated circuit. It describes all aspects required for the development of systems based on XWAY™ PHY11G technology.

1.1 About XWAY™ PHY11G

The XWAY™ PHY11G is an ultra-low power, multi-mode Gigabit Ethernet (GbE) PHY IC, supporting speeds of 10, 100 and 1000 Mbit/s in full-duplex or half-duplex mode. It can be used in various data flows based on twisted-pair and fiber-optic communication links. The main application is the copper mode, where Media-Independent Interface (MII) data is converted to a Media-Dependent Interface (MDI) based on the 10BASE-T(e), 100BASE-TX and 1000BASE-T Ethernet standards according to **[1]**.

The XWAY™ PHY11G supports a number of features for convenience and reliability, including auto-negotiation (**Chapter 3.3.2**), auto-MDIX, auto-downspeed (**Chapter 3.3.3**) and cable wiring fault correction. In addition, the integrated cable diagnostics mode, the test packet generator, and the various test loops can be used for analysis and debugging of the target system. The XWAY™ PHY11G includes an integrated serializer/deserializer (SerDes) that can be used to operate a fiber link in conjunction with a 1000BASE-X fiber module. This capability enables media-converter data flow applications.

The MII pins of the XWAY™ PHY11G can be re-assigned to form one of several standard MII interfaces such as RMII, RGMII, RTBI and SGMII. In RGMII mode, the integrated delay function for the TX and RX clock simplifies PCB design. In SGMII mode, the PHY does not require a receive clock and instead uses the integrated Clock and Data Recovery (CDR).

Configuration management of the XWAY™ PHY11G can be done using its MDIO interface. Alternatively, the device can be pre-configured by means of an external I^2C-based EEPROM. Simple basic settings can be made using the novel soft pin-strapping feature available for the LED pins (see **Chapter 3.4.1**). The device also integrates a standard Test Access Port (TAP) for boundary scan.

The XWAY™ PHY11G is encased in the industry's smallest package (VQFN48) for a GbE PHY device with a given feature set and considering the level of integration. It therefore provides an ideal solution for footprint-sensitive applications such as SFP copper modules or LAN-on-Motherboard. Furthermore, the XWAY™ PHY11G design supports a reduced external bill of materials, for example through the integration of termination resistances at both the MDI and MII. The CLKOUT pin can optionally be used to provide a 25/125 MHz reference clock, allowing for multiple PHY devices to be cascaded while using only one crystal.

With an effectiveness of more than 80%, the XWAY™ PHY11G is tailored for energy efficiency. It can be operated from a single power supply ranging from 2.5 V to 3.3 V, in which case the 1.0 V domains are self-supplied using the device's integrated DC/DC switching regulator. By supporting the Energy-Efficient Ethernet (EEE) standard as defined in the IEEE 802.3az standard (**[2]**), the PHY is able to reduce active power consumption during periods of low link utilization, to as little as 10% of the nominal consumption. Through implementation of a real voltage mode line-driver, the active nominal power of the device is significantly reduced when compared to other devices of the same kind. Additionally, this line-driver technology does not require any center tap supply at the magnetics. This further simplifies the magnetics as there is now no need to use common-mode chokes.

The XWAY™ PHY11G supports further power savings at system level by means of the integrated Wake-on-LAN (WoL) feature. This mode can be activated at all Ethernet speeds. A WoL event is indicated to the SoC via an interrupt pin. It is possible to configure the polarity and functionality of this interrupt. Various events may be indicated via this interrupt, so as to reduce the need for MDIO polling by the SoC.

The XWAY™ PHY11G provides a set of 3 freely-configurable LED pins. Although LEDs can also be directly driven by the SoC (for example a network processor) via MDIO registers, the built-in functionality covers application needs such as bi-color LED support, configurable blinking frequencies, and configurable multiple-function assignment per LED.

1.2 Overview

This section gives an overview of the features and capabilities of the XWAY™ PHY11G Version 1.5.

1.2.1 Logic Symbol

Figure 1 shows the logic symbol of the XWAY™ PHY11G.

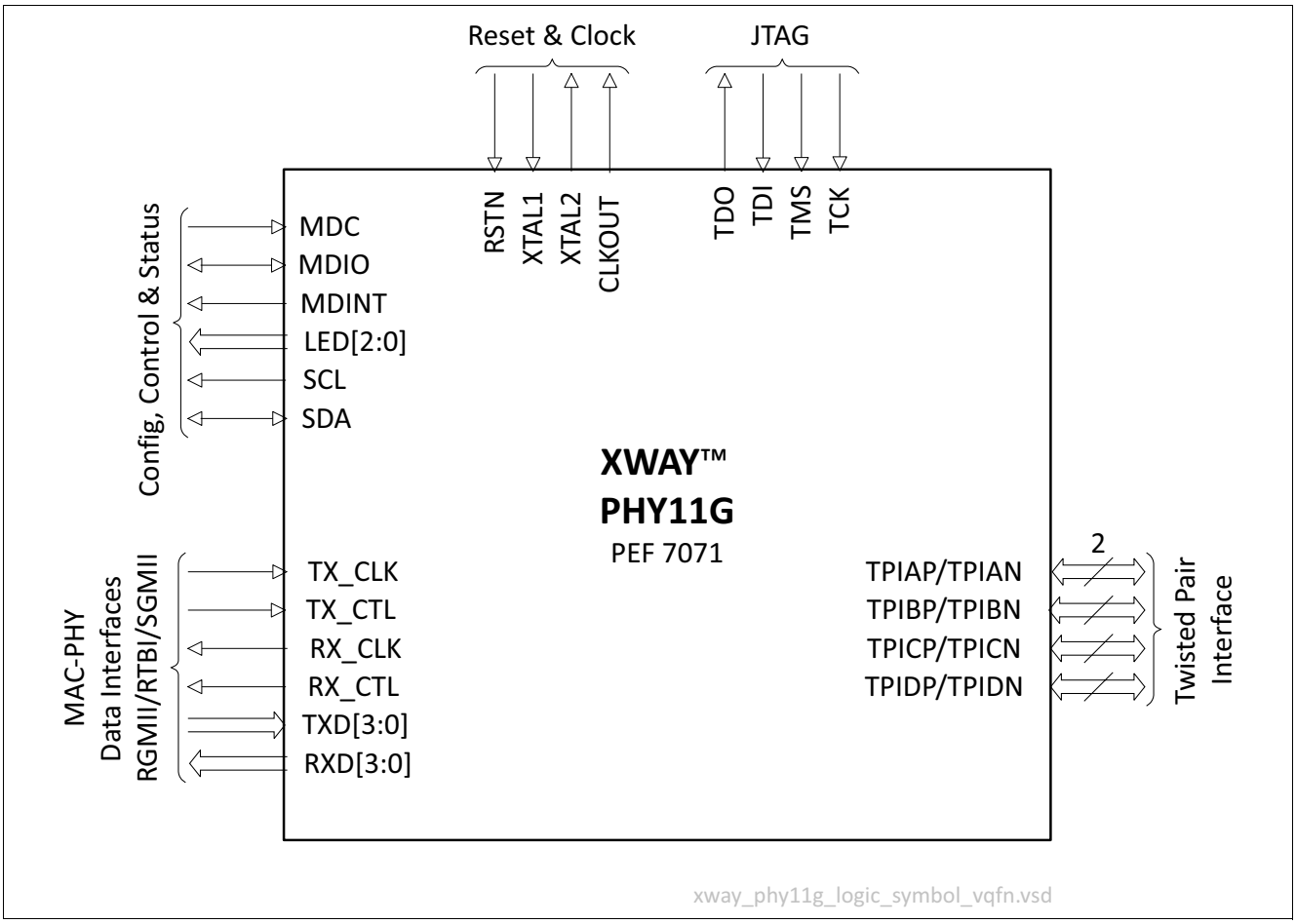


Figure 1 Logic Symbol of the XWAY™ PHY11G

1.2.2 Features

This section outlines the features of the XWAY™ PHY11G Version 1.5.

General:

- Flexible power supply: V_{DDH} = 2.5 V... 3.3 V
- Single power supply optionally using the integrated DC/DC converter
- Low power consumption of 400 mW in Gigabit Ethernet mode
- Configurable startup mode using sophisticated pin-strappings
- Flexible architecture using an integrated device controller

Interfaces:

- Twisted-pair interface:
  - 10BASE-T(e), 100BASE-TX, 1000BASE-T[1)]
  - Support of Power over Ethernet (PoE, see **Chapter 3.5.2**)
  - Support of transformerless Ethernet for backplane applications
- Data interfaces (xMII1):
  - RMII
  - RGMII
  - RTBI
  - SGMII /1000BASE-X SerDes at 1.25 Gbaud
  - Jumbo packets of up to 10 kB
- Control interfaces:
  - MDIO
  - JTAG interface for boundary scan
  - Support of stand-alone operational mode using EEPROM interface (I^2C, Two-Wire)
- Clocking:
  - Support of 25 MHz and 125 MHz input clock
  - Support of 25 MHz crystal using integrated oscillator
  - 25 MHz or 125 MHz clock output

Ethernet:

- Auto-negotiation with next-page support
- Wake-on-LAN support
- Auto-downspeed
- Support of auto-MDIX at all copper media speeds
- Support of auto polarity-correction at all copper media speeds
- Various test features:
  - Test loops
  - Dummy frame generation and frame error counters
  - Analog self-test
- Cable diagnostics:
  - Cable open/short detection
  - Cable length estimation

External circuitry optimization:

- Integrated termination resistors at twisted-pair interface
- Integrated termination resistors at RGMII

1) 10BASE-T operation is only standard-conform at V_{DDH} = 3.3 V. This limitation does not apply to 10BASE-Te Ethernet.

- Support of low-cost transformers (magnetics)
- Support of low-cost crystal

1.2.3 Typical Applications

This section introduces typical applications of the XWAY™ PHY11G, sorted according to the medium type used in the application.

1.2.3.1 Copper Application

In applications using the copper medium, the XWAY™ PHY11G is used to connect a 10/100/1000BASE-T capable MAC unit to a twisted-pair medium, such as a CAT5 cable infrastructure. The connection between MAC and PHY can be established using one of the supported xMII interface types: RGMII, RTBI or SGMII.

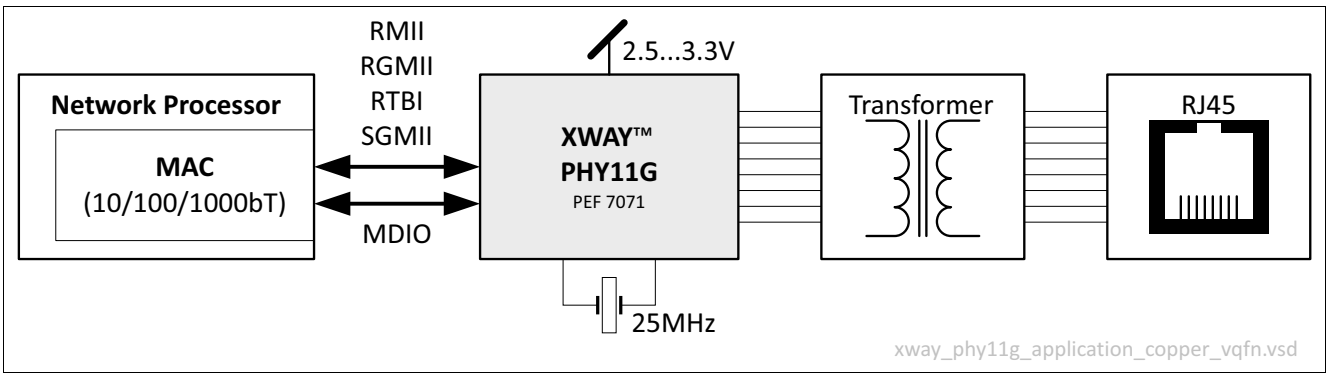


Figure 2 XWAY™ PHY11G Used in Copper Applications

1.2.3.2 Media Converter Application

In media converter applications, the PHY is used to interface between fiber and copper media. The fiber medium can be connected using a fiber or SFP module, which is connected via a 1000BASE-X or SGMII interface. The copper medium is connected via a twisted-pair interface (RJ45), using a transformer for galvanic de-coupling. Only one instance of the XWAY™ PHY11G device is required to address this application. Stand-alone operation is possible using the EEPROM (see **Chapter 3.4.2**) self-configuration capability.

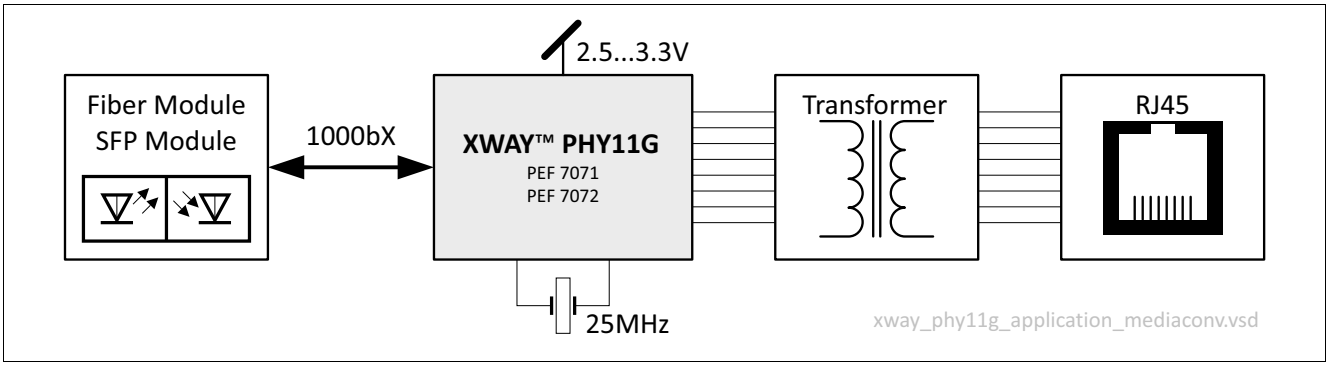


Figure 3 XWAY™ PHY11G Used in Media Converter Applications

1.2.3.3 Gigabit Interface Converter (GBIC) Application

The GBIC **[12]** application is used to support a 10/100/1000BASE-T GBIC/SFP module implementation, as illustrated in **Figure 4**. The MDIO interface of the XWAY™ PHY11G device is now not available, but an EEPROM can optionally be used to upload customer-specific configuration settings (see **Chapter 3.4.2**).

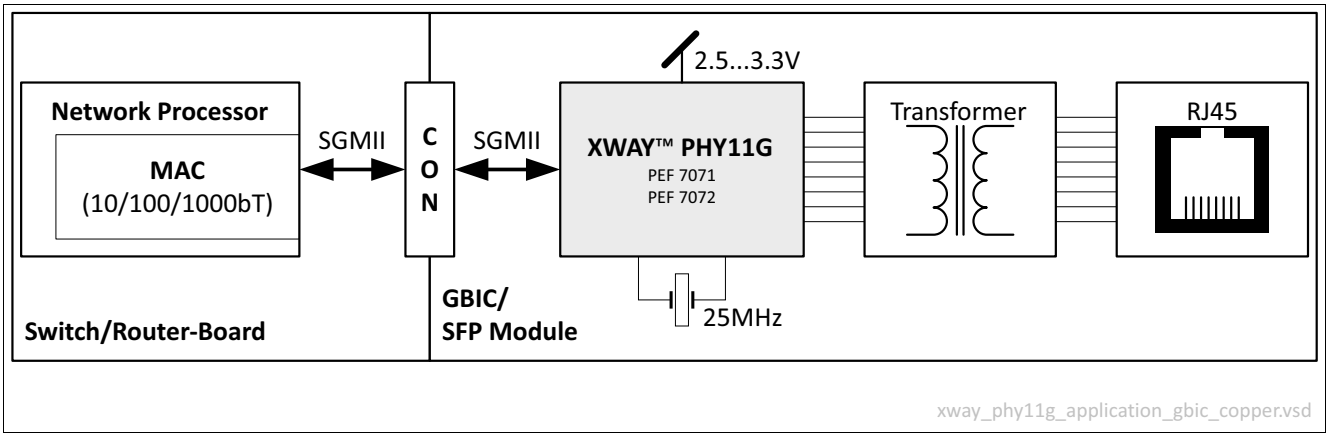


Figure 4 XWAY™ PHY11G Used in 10/100/1000BASE-T GBIC/SFP Application

1.2.4 Terminology and Nomenclature

Throughout this document, the terms transmit (TX) and receive (RX) are used to specify the data and signal flow directions. Unless stated otherwise, the TX direction refers to the flow of data and signals from the MII to the MDI, that is from the MAC interface to the transmission medium. The transmission of data actually refers to the transport of data towards the next lower layer in the OSI reference model. The RX direction refers to the flow of data and signals in the opposite directions.

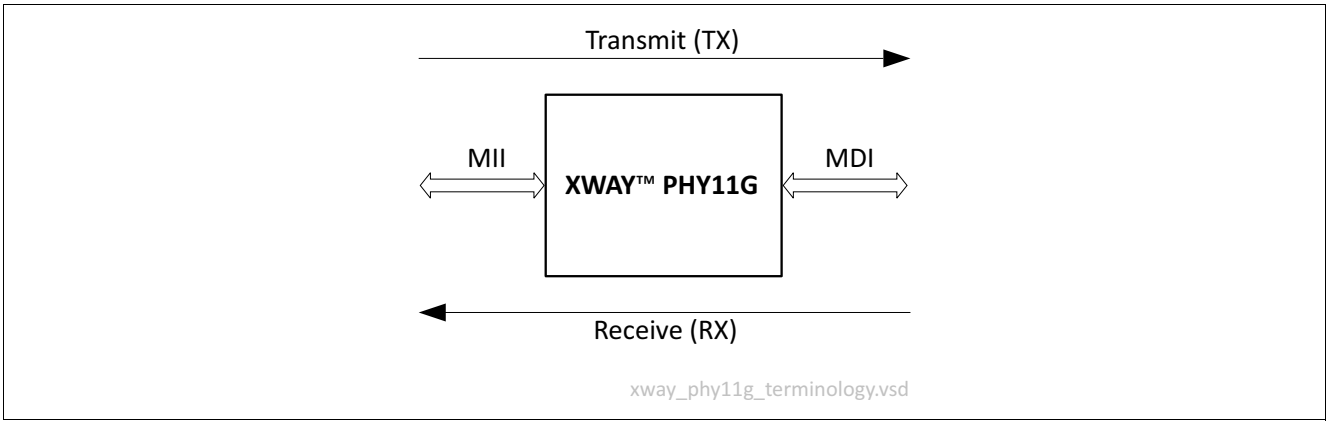


Figure 5 Transmit and Receive Terminology

Abbreviations are used throughout this document. Each abbreviation is explained once at its first appearance in the text, and is also included in a consolidated list of acronyms in **Terminology**.

When referring to registers, the document uses the following nomenclature:

`[Address-Space].[Sub-Space].[Register].[Register-Element]`

As an example,

`MDIO.STD.CTRL.PD`

refers to the PD bit inside the CTRL register, which is located inside the STD register's space of the MDIO address space (see also **Chapter 4**).

Alternatively, the text uses register references according to IEEE8 02.3-2005. These references are only applicable to the `MDIO.*` address space. Such references use the format:

`(Register-Number.Register-Bit-Number)`

As an example, the reference `(0.11)` refers to the same `MDIO.STD.CTRL.PD` bit.

2 External Signals

This chapter describes the external signals of the XWAY™ PHY11G.

2.1 Pin Diagram

Figure 6 shows the pin diagram of the XWAY™ PHY11G when taking a top view of the VQFN48 package. The pins and the common ground pad (EPAD) are visible on the bottom side of the package. The latter is illustrated using dashed lines. The subsequent sections describe each of these pins in more detail.

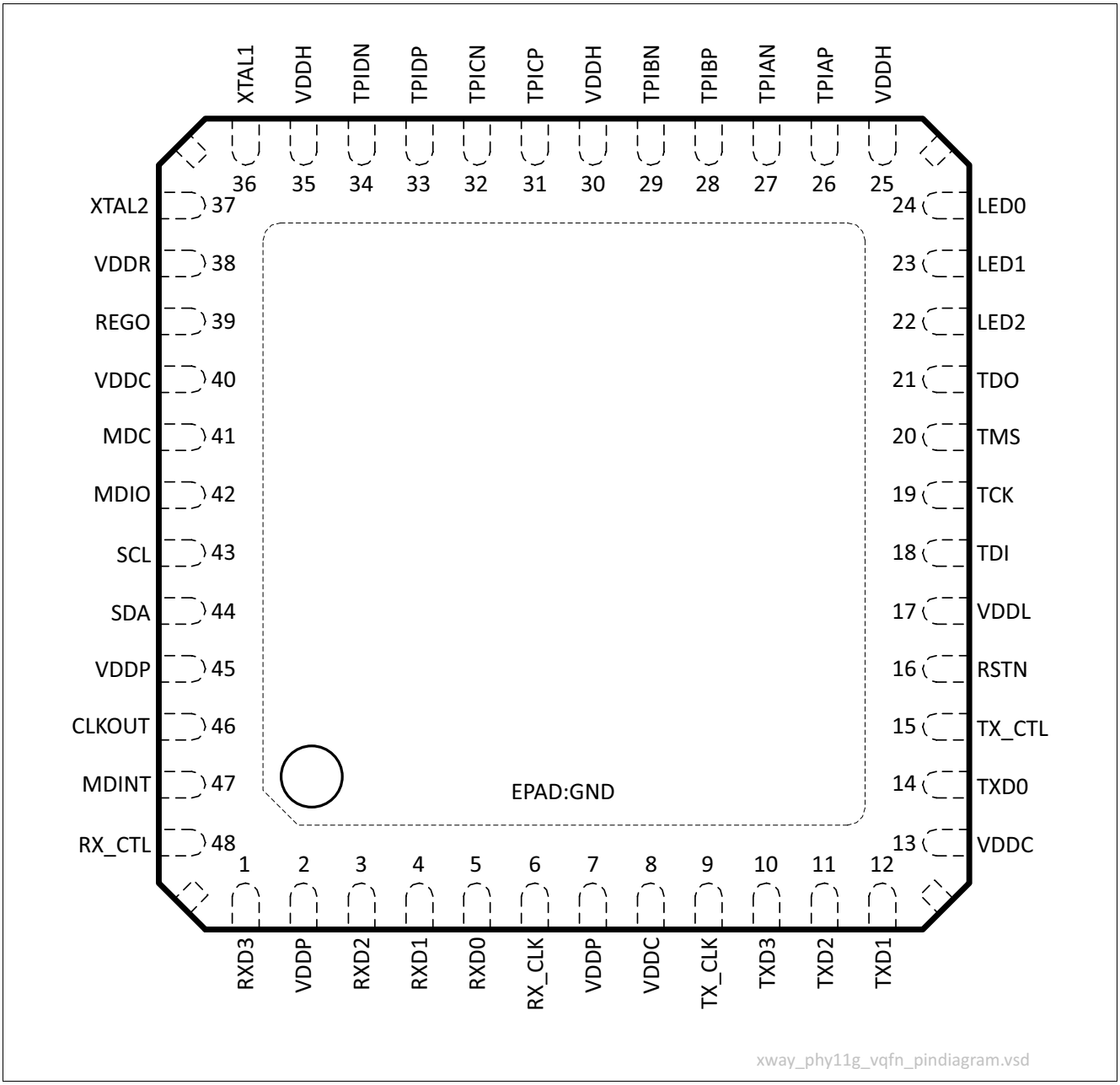


Figure 6 Pin Diagram of the XWAY™ PHY11G (Top View of VQFN48 Package)

2.2 Pin Description

In this section, all the XWAY™ PHY11G pins are grouped according to their functionality and described in detail in **Chapter 2.2.2** through to **Chapter 2.2.7** respectively. **Chapter 2.2.1** explains the terminology used for the pin and buffer types.

2.2.1 Pin Identifications

The abbreviations used in the following sub-sections for the pin types and buffer types are explained in **Table 1** and **Table 2** respectively.

Table 1 Abbreviations for Pin Types

Type	Long Name	Remarks
I	Input pin	
O	Output pin	
I/O	Bi-directional pin	
PWR	Power supply pin	
GND	Ground pin	

Table 2 Abbreviations for Buffer Types

Type	Long Name	Remarks
A	Analog levels	This buffer type is used for purely analog levels. The exact electrical characteristics are specified in the corresponding sections of **Chapter 6**.
HD	High-speed differential	This buffer type is used for SerDes pins, for example for SGMII or 1000BASE-X. These pins are properly terminated with a resistance of 50/75 Ω and must be AC-coupled. More details on the mandatory and optional external circuitry are given in **Chapter 6.8.6**.
PU	Internal pull-up resistor	This buffer type includes a weak internal pull-up resistor which pulls the signal to V_{DDP} (logic 1_B) when left unconnected or tristated (high-impedance).
PD	Internal pull-down resistor	This buffer type includes a weak internal pull-down resistor which pulls the signal to V_{SSP} (logic 0_B) when left unconnected or tristated (high-impedance).
LVTTL	Digital LVTTL levels	LVTTL buffer types according to JESD8-B. Note that this buffer is only supported when the pad supply V_{DDP} is nominally 3.3 V.
CMOS	Digital CMOS 2v5 levels	CMOS 2v5 buffer types according to JESD8-5. Note that this buffer is only supported when the pad supply V_{DDP} is nominally 2.5 V.

Note: Several pins are marked as having LVTTL/CMOS buffer type. This nomenclature defines that when V_{DDP} = 3.3 V, the pin operates in LVTTL buffer type mode, and when V_{DDP} = 2.5 V, the pin operates in CMOS2v5 buffer type mode.

Note: In CMOS mode, the input pins must not be driven with LVTTL levels!

2.2.2 General Pins

This section describes the group of general pins required for the correct operation of the XWAY™ PHY11G, including the clock, reset and DC/DC converter interfaces.

Table 3 General Pins

Pin No.	Name	Pin Type	Buffer Type	Function
16	**RSTN**	I	LVTTL/ CMOS, PU	**Reset** Asynchronous low-active reset of the device to default
36	**XTAL1**	I	A	**Crystal Mode: Crystal Oscillator Pin 1** A 25 MHz crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also be used to tie both pins to GND.
	REFCLK		LVTTL/ CMOS, PU	**Reference Mode: Clock Input** The clock input for the XWAY™ PHY11G. This clock input can be either a 25 MHz or a 125 MHz clock. The reference clock must have a frequency accuracy of +/-50 ppm. The device automatically detects the frequency and adjusts its internal PLL accordingly.
37	**XTAL2**	O	A	**Crystal-Mode: Crystal Oscillator Pin 2** See XTAL1
	XTAL2			**Reference-Mode: Not used** Must be left unconnected in this mode
46	**CLKOUT**	O	LVTTL/ CMOS	**NORMAL: Clock Output** After de-assertion of the reset signal RSTN, this pin outputs a clock signal that can have a frequency of either 25 MHz or 125 MHz. The frequency is selected via the `CLKSEL` field in the **Physical Layer Control 2** MDIO register (default = 25 MHz).
39	**REGO**	O	A	**Integrated DC/DC Regulator Output** Provides a current output to self-supply the 1.0 V domains (V_{DDC}, V_{DDL}) of the XWAY™ PHY11G from the V_{DDR} supply

2.2.3 Media-Dependent Interface (MDI) Pins

This section describes the twisted-pair Media-Dependent Interface (MDI), which directly connects to the transformer device. No external termination resistors are required.

Table 4 Twisted-Pair Interface Pins

Pin No.	Name	Pin Type	Buffer Type	Function
26	**TPIAP**	I/O	A	**Differential Tx/Rx Port for Twisted-Pair A** This is the twisted-pair port A that can be directly connected to the corresponding transformer pins. *Note: This port has a 100 Ω nominal impedance due to integrated termination resistors.*
27	**TPIAN**			
28	**TPIBP**	I/O	A	**Differential Tx/Rx Port for Twisted-Pair B** This is the twisted-pair port B that can be directly connected to the corresponding transformer pins. *Note: This port has a 100 Ω nominal impedance due to integrated termination resistors.*
29	**TPIBN**			
31	**TPICP**	I/O	A	**Differential Tx/Rx Port for Twisted-Pair C** This is the twisted-pair port C that can be directly connected to the corresponding transformer pins. *Note: This port has a 100 Ω nominal impedance due to integrated termination resistors.*
32	**TPICN**			
33	**TPIDP**	I/O	A	**Differential Tx/Rx Port for Twisted-Pair D** This is the twisted-pair port D that can be directly connected to the corresponding transformer pins. *Note: This port has 100 Ω nominal impedance due to integrated termination resistors.*
34	**TPIDN**			

2.2.4 Media-Independent Interface (MII) Pins

This section describes the Media-Independent Interface (MII), which connects the MAC to the XWAY™ PHY11G. Multiplexed pins support several interface types, such as RMII, RGMII, RTBI and SGMII. Due to the pin limitations and the large number of supported interfaces, the multiplexing of pins between the different interfaces can be complex. This chapter gives a detailed view of each pin. **Table 10** gives an overview of MII pin multiplexing.

Table 5 Media-Independent Interface Pins

Pin No.	Name	Pin Type	Buffer Type	Function
9	**TX_CLK**	I	LVTTL/ CMOS, PD	**RGMII: Transmit Clock** The TXC signal is a continuous clock signal and provides the timing reference for the transfer of TX_EN_CTL and TXD[3:0]. The nominal frequency of this clock is 125 MHz for 1000 Mbit/s, 25 MHz for 100 Mbit/s, and 2.5 MHz for 10 Mbit/s. Depending on the speed selection, this clock is assumed to be properly adjusted by the MAC. The frequency deviation is assumed to be smaller than +/- 50 ppm.
	REFCLK			**RMII: Reference Clock for the Transmit and Receive MAC I/F** The REFCLK signal is used by the MAC and the PHY MII for synchronous data transfers. The nominal frequency of this clock is 50 MHz. The XWAY™ PHY11G optionally provides a suitable free-running 50 MHz clock on RX_CLK.
	TXC			**RTBI: Transmit Clock** The TXC signal is a continuous clock signal and provides the timing reference for the transfer of TX_EN_CTL and TXD[3:0]. The nominal frequency of this clock is 125 MHz, since RTBI is only defined for 1000 Mbit/s. The frequency deviation is assumed to be smaller than +/-50 ppm.
	SCP	O	HD	**SGMII: Serial Clock (Positive Pin)** This is the positive signal of the differential clock pair of the SGMII SerDes interface. In conjunction with SCN, it provides a 625 MHz differential clock that is source-synchronous with SOP/SON. If a MAC with CDR isused, this pin can be left open. The SCP pin must be AC-coupled. For more details, see **Chapter 6.8.6**.

Table 5 Media-Independent Interface Pins (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
6	**RX_CLK**	O	LVTTL/ CMOS	**RGMII: Receive Clock** The RXC signal is a continuous clock signal and provides the timing reference for the transfer of RX_EN_CTL and RXD[3:0]. The nominal frequency of this clock is 125 MHz for 1000 Mbit/s, 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. The frequency deviation is smaller than +/-50 ppm.
	CLK50			**RMII: Optional 50 MHz Reference Clock for the RMII** This pin optionally provides a free-running reference clock for the RMII. This clock can be wired to the MAC and the TX_CLK of the XWAY™ PHY11G device . The nominal frequency of this clock is 50 MHz.
	RXC			**RTBI: Receive Clock** The TXC signal is a continuous clock signal and provides the timing reference for the transfer of RX_DV_CTL and RXD[3:0]. The nominal frequency of this clock is 125 MHz, since RTBI is only defined for 1000 Mbit/s. The frequency deviation is assumed to be smaller than +/-50 ppm.
	-			**SGMII: Not Used** The XWAY™ PHY11G drives logic zero in this mode.
10	TXD3	I	LVTTL/ CMOS, PD	**RGMII: Transmit Data Bit 3** This pin carries bit 3 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
	-			**RMII: Not Used** Should be connected to GND or driven with logic zero
	TXD38			**RTBI: Transmit Data Bits 3 and 8** This pin carries bits 3 and 8 of the double data rate RTBI transmit data vector. It is synchronous with TBI_TXCKL. The bits are subject to the rising and falling edges respectively of the TBI_TXCLK signal.
	SCN	O	HD	**SGMII: Serial Clock (Negative Pin)** This is the negative signal of the differential clock pair of the SGMII SerDes interface. In conjunction with SCP, it provides a 625 MHz differential clock that is source-synchronous with SOP/SON. If a MAC with CDR is used, this pin can be left open. The pin must be AC-coupled. For more details, see **Chapter 6.8.6**.
	SIGDET	I	LVTTL/ CMOS	**1000BASE-X: Signal Detect** The signal detect pin is used in dual-media applications to detect whether a valid signal is present from the FO module. The polarity of this pin can be programmed via the `SDETP` field in the **Physical Layer Control 2** register.

Table 5 Media-Independent Interface Pins (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
11	TXD2	I	LVTTL/ CMOS, PD	**RGMII: Transmit Data Bit 2** This pin carries bit 2 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
	-			**RMII: Not Used** Should be connected to GND or driven with logic zero
	TXD27			**RTBI: Transmit Data Bits 2 and 7** This pin carries bits 2 and 7 of the double data rate RTBI transmit data vector. It is synchronous with TBI_TXCKL. The bits are subject to the rising and falling edges respectively of TBI_TXCLK.
	SOP	O	HD	**SGMII: Serial Output (positive pin)** This is the positive signal of the differential output (receive) pair of the SGMII SerDes interface. In conjunction with SON, it provides a 1.25 Gbit/s differential data signal that is source-synchronous with the differential 625 MHz clock SCP/SCN. This pin must be AC-coupled. For more details, see **Chapter 6.8.6**.
	TDP		HD	**1000BASE-X: Transmit Data (positive pin)** This is the positive signal of the differential transmit output pair of the 1000BASE-X SerDes interface. In conjunction with TDN, it provides a 1.25 Gbit/s differential data signal to the fiber-optic module. This pin must be AC-coupled. For more details, see **Chapter 6.8.7**.
12	TXD1	I	LVTTL/ CMOS, PD	**RGMII: Transmit Data Bit 1** This pin carries bit 1 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
	TXD1			**RMII: Transmit Data Bit 1** This pin carries bit 1 of the TXD[1:0] RMII transmit data vector. It is synchronous with REFCLK.
	TXD16			**RTBI: Transmit Data Bits 1 and 6** This pin carries bits 1and 6 of the double data rate RTBI transmit data vector. It is synchronous with TBI_TXCKL. The bits are subject to the rising and falling edges respectively of TBI_TXCLK.
	SON	O	HD	**SGMII: Serial Output (Negative Pin)** This is the negative signal of the differential output (receive) pair of the SGMII SerDes interface. In conjunction with SOP, it provides a 1.25 Gbit/s differential data signal that is source-synchronous with the differential 625 MHz clock SCP/SCN. This pin must be AC-coupled. For more details, see **Chapter 6.8.6**.
	TDN			**1000BASE-X: Transmit Data (Negative Pin)** This is the negative signal of the differential transmit output pair of the 1000BASE-X SerDes interface. In conjunction with TDP, it provides a 1.25 Gbit/s differential data signal to the fiber-optic module. This pin must be AC-coupled. For more details, see **Chapter 6.8.7**.

Table 5 Media-Independent Interface Pins (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
14	TXD0	I	LVTTL/ CMOS, PD	**RGMII: Transmit Data Bit 0** This pin carries bit 0 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
	TXD0			**RMII: Transmit Data Bit 0** This pin carries bit 0 of the TXD[1:0] RMII transmit data vector. It is synchronous with REFCLK.
	TXD05			**RTBI: Transmit Data Bits 0 and 5** This pin carries bits 0 and 5 of the double data rate RTBI transmit data vector. It is synchronous with TBI_TXCKL. The bits are subject to the rising and falling edges respectively of TBI_TXCLK.
	SIP		HD	**SGMII: Serial Input (Positive Pin)** This is the positive signal of the differential input (transmit) pair of the SGMII SerDes interface. In conjunction with SIN, it samples a 1.25 Gbit/s differential data signal. Due to the integrated CDR, no external MAC source-synchronous clock is required. This pin must be AC-coupled. For more details, see **Chapter 6.8.6**.
	RDP			**1000BASE-X: Receive Data (Positive Pin)** This is the positive signal of the differential receive input pair of the 1000BASE-X SerDes interface. In conjunction with RDN, it constitutes a 1.25 Gbit/s differential data signal driven by the fiber-optic module. This pin must be AC-coupled. For more details, see **Chapter 6.8.7**.
15	**TX_CTL**	I	LVTTL/ CMOS, PD	**RGMII: Transmit Control** This pin is the transmit control signal for the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.
	TX_EN			**RMII: Transmit Enable** This is the transmission-enable signal driven by the MAC, and which is synchronous with REFCLK. The signal indicates valid data frames on TXD[1:0] to the PHY. The signal polarity is active high.
	TXD49			**RTBI: Transmit Data Bits 4 and 9** This pin carries bits 4 and 9 of the double data rate RTBI transmit data vector. It is synchronous with TBI_TXCKL. The bits are subject to the rising and falling edges respectively of TBI_TXCLK.
	SIN		HD	**SGMII: Serial Input (Negative Pin)** This is the negative signal of the differential input (transmit) pair of the SGMII SerDes interface. In conjunction with SIP, it samples a 1.25 Gbit/s differential data signal. Due to the integrated CDR, no external MAC source-synchronous clock is required. This pin must be AC-coupled. For more details, see **Chapter 6.8.6**.
	RDN			**1000BASE-X: Receive Data (negative pin)** This is the negative signal of the differential receive input pair of the 1000BASE-X SerDes interface. In conjunction with RDP, it constitutes a 1.25 Gbit/s differential data signal driven by the fiber-optic module. This pin must be AC-coupled. For more details, see **Chapter 6.8.7**.

Table 5 Media-Independent Interface Pins (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
48	RX_CTL	O	LVTTL/ CMOS	**RGMII: Receive Control** This is the receive control signal driven by the PHY, and which is synchronous with RXC. The signal encodes the RX_DV and RX_ER signals of the GMII, according to the RGMII specification. The signal polarity is active high.
	CRS_DV			**RMII: Carrier Sense and Data Valid** This is the carrier sense/data valid signal driven by the PHY, and which is synchronous with REFCLK. The signal encodes the RX_DV and CRS signals of the RMII, according to the RMII specification. The signal polarity is active high.
	-			**RTBI: Not Used** The XWAY™ PHY11G drives logic zero in this mode.
	-			**SGMII: Not Used** The XWAY™ PHY11G drives logic zero in this mode.
1	**RXD3**	O	LVTTL/ CMOS	**RGMII: Receive Data Bit 3** This pin carries bit 3 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC.
	-			**RMII: Not Used** The XWAY™ PHY11G drives logic zero in this mode.
	RXD38			**RTBI: Receive Data Bits 3 and 8** This pin carries bits 3 and 8 of the double data rate RTBI receive data vector. It is synchronous with RXC. The bits are subject to the rising and falling edges respectively of RXC.
	-			**SGMII: Not Used** The XWAY™ PHY11G drives logic zero in this mode.
3	**RXD2**	O	LVTTL/ CMOS	**RGMII: Receive Data Bit 2** This pin carries bit 2 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC.
	-			**RMII: Not Used** The XWAY™ PHY11G drives logic zero in this mode.
	RXD27			**RTBI: Receive Data Bits 2 and 7** This pin carries bits 2 and 7 of the double data rate RTBI receive data vector. It is synchronous with RXC. The bits are subject to the rising and falling edges respectively of RXC.
	-			**SGMII: Not Used** The XWAY™ PHY11G drives logic zero in this mode.

Table 5 Media-Independent Interface Pins (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
4	**RXD1**	O	LVTTL/ CMOS	**RGMII: Receive Data Bit 1** This pin carries bit 1 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC.
	RXD1			**RMII: Receive Data Bit 1** This pin carries bit 1 of the RXD[1:0] RMII receive data vector. It is synchronous with REFCLK.
	RXD16			**RTBI: Receive Data Bit 1 and 6** This pin carries bit 1 and 6 of the double data rate RTBI receive data vector. It is synchronous with RXC. The bits are subject to the rising and falling edges respectively of RXC.
	-			**SGMII: Not Used** The XWAY™ PHY11G drives logic zero in this mode.
5	**RXD0**	O	LVTTL/ CMOS	**RGMII: Receive Data Bit 0** This pin carries bit 0 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC.
	RXD0			**RMII: Receive Data Bit 0** This pin carries bit 0 of the RXD[1:0] RMII receive data vector. It is synchronous with REFCLK.
	RXD05			**RTBI: Receive Data Bit 0 and 5** This pin carries bit 0 and 5 of the double data rate RTBI receive data vector. It is synchronous with RXC. The bits are subject to the rising and falling edges respectively of RXC.
	-			**SGMII: Not Used** The XWAY™ PHY11G drives logic zero in this mode.

2.2.5 Control Interface Pins

This section specifies the MDIO Interface according to clause 22 in [1]. The AC characteristics of this interface are defined in Chapter 6.6.5.

Table 6 Control Interface Pins

Pin No.	Name	Pin Type	Buffer Type	Function
41	**MDC**	I	LVTTL/ CMOS, PD	**MDIO: Management Data Clock** This is the MDIO data clock signal with which the serial management interface signals on MDIO are synchronized. All MDIO signals are subject to change at the rising edge of MDC.
42	**MDIO**	I/O	LVTTL/ CMOS, PU	**MDIO: Management Data Input/Output** The management data input/output pin carries control information written by the higher-level management entity to the PHY. This includes command, address and write information. The MDIO is registered on the rising edge of MDC. The pin is pulled up in input mode only.
47	**MDINT**	O	LVTTL/ CMOS	**MDIO: Management Interrupt** This pin can be used to drive an interrupt signal to the higher-level management entity. The event for which this interrupt should be issued is configurable via the MDIO registers. If no interrupt is active, then the pin is in a high-impedance state. The polarity of the pin can be set via an external pull-up (low-active MDINT) or pull-down (high-active MDINT) resistor. A value of 10 kΩ is recommended. In case multiple XWAY™ PHY11G devices are controlled by one higher-level management entity, these signals can be combined using a wired-or. After the XWAY™ PHY11G is reset, the signal becomes active to indicate that it is ready to accept MDIO inputs. The register MDIO.PHY.ISTAT needs to be read to deactivate this signal.
LED Interface				
24	**LED0**	I/O	A	**LED0** This is a freely configurable LED port that can be used to connect a preferably low-current LED. *Note: This pin reads in soft pin-strapping information during reset.*
23	**LED1**	I/O	A	**LED1** This is a freely configurable LED port that can be used to connect a preferably low-current LED. *Note: This pin reads in soft pin-strapping information during reset.*
22	**LED2**	I/O	A	**LED2** This is a freely configurable LED port that can be used to connect a preferably low-current LED. *Note: This pin reads in soft pin-strapping information during reset.*

Table 6 Control Interface Pins (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
EEPROM/I²C/Two-Wire Interface				
43	**SCL**	O	LVTTL/ CMOS, PU	**Serial Clock** This is the serial clock of the I²C interface. The maximum frequency of this interface is 1 MHz. The frequency is configurable via the soft pin-strapping pins. This clock is only active when an EEPROM is connected and during an access to the EEPROM. The duty cycle is 50%.
44	**SDA**	I/O	LVTTL/ CMOS, PU	**Serial Data/Address** This is the serial data/address of the I²C interface that shall (optionally) be connected to an external EEPROM supporting an I²C (or Two-Wire) interface. An operational mode using an external EEPROM is useful in systems without a higher-level management entity. The XWAY™ PHY11G automatically detects a connected EEPROM by monitoring the SDA pin after reset or power-up. This pin must be connected to GND to indicate that no EEPROM is present. If an EEPROM is present, the soft pin-strapping pins are used to define the speed and operational mode of the EEPROM interface.

2.2.6 JTAG Interface

This section describes the JTAG test pins used for boundary scan testing[1)].

Table 7 JTAG Interface Pins

Pin No.	Name	Pin Type	Buffer Type	Function
21	**TDO**	O	LVTTL/ CMOS	**JTAG Serial Test Data Output**
18	**TDI**	I	LVTTL/ CMOS, PU	**JTAG Serial Test Data Input**
20	**TMS**	I		**JTAG Test Mode Select**
19	**TCK**	I		**JTAG Test Clock** The TDI, TDO and TMS signals are synchronized with this JTAG test clock. *Note: If the JTAG interface is not used, this pin must be tied to V_{DDH} using a pull-up resistor!*

1) JTAG reset is achieved by an internal power-on-reset module and therefore a TRST input is unnecessary.

2.2.7 Power Supply Pins

This section specifies the power supply pins of the XWAY™ PHY11G. The operating ranges of the power domains are specified in **Chapter 6.2**.

Table 8 Power Supply Pins

Pin No.	Name	Pin Type	Buffer Type	Function
25,30,35	**VDDH**	PWR		**High-Voltage Domain Supply** This is the group of supply pins for the high-voltage domain, which supplies the line driver in the PMA of the XWAY™ PHY11G. This supply has to provide a nominal voltage of V_{DDH} = 2.5 V...3.3 V, with a worst case tolerance of ±5% at the respective corners. *Note: For optimal power consumption, the lowest possible voltage is selected in the system.*
38	**VDDR**	PWR		**Regulator Voltage Domain Supply** This is the group of supply pins for the DC/DC switching regulator voltage domain, which supplies the integrated DC/DC converter of the XWAY™ PHY11G. This supply has to provide a nominal voltage of V_{DDR} = 2.5 V...3.3 V, with a worst case tolerance of ±5% at the respective corners. *Note: For optimal power consumption, the lowest possible voltage is selected in the system.*
2,7,45	**VDDP**	PWR		**Pad Voltage Domain Supply** This is the group of supply pins for the pad supply of the XWAY™ PHY11G. This supply has to provide a nominal voltage of V_{DDP} = 2.5 V...3.3 V, with a worst case tolerance of ±5% at the respective corners. *Note: For optimal power consumption, the lowest possible voltage is selected in the system.*
17	**VDDL**	PWR		**Low-Voltage Domain Supply** This is the group of supply pins for the low-voltage domain, which supplies mixed signal blocks in the PMA of the XWAY™ PHY11G. The supply has to provide a nominal voltage of V_{DDL} = 1.0 V, with a worst case tolerance of ±5%.
8,13,40	**VDDC**	PWR		**Core Voltage Domain Supply** This is the group of supply pins for the core voltage domain. It supplies the digital core blocks of the XWAY™ PHY11G. This supply has to provide a nominal voltage of V_{DDL} = 1.0 V with a worst case tolerance of ±5%.
EPAD[1)]	**VSS**	GND		**General Device Ground**

1) The EPAD is the exposed pad at the bottom of the package. This pad must be properly connected to the PCB ground plane.

3 Functional Description

Figure 7 shows a block diagram of the XWAY™ PHY11G device. It also outlines the relationship of the device pins to the main functional blocks. The following sections describe the functionality of these blocks in more detail.

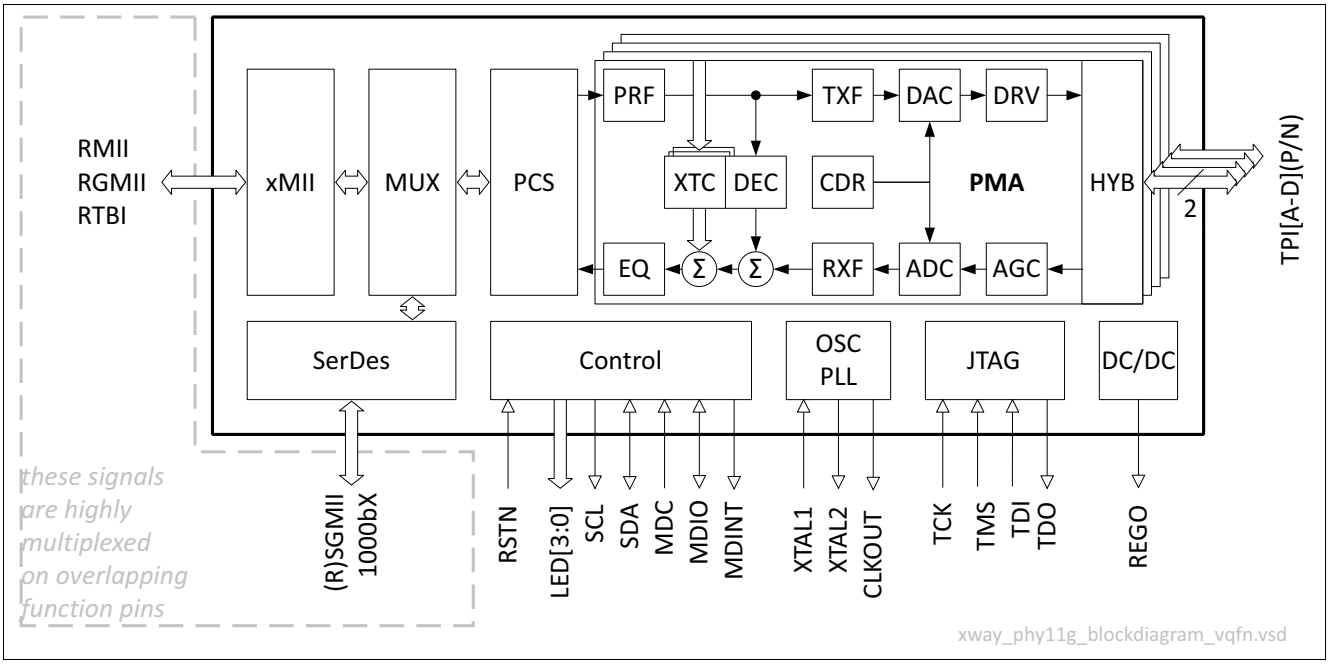


Figure 7 Functional High-Level Block Diagram of XWAY™ PHY11G

3.1 Modes of Operation

The XWAY™ PHY11G supports various MII types, such as RMII, RGMII, SGMII and RTBI. These can be combined with two MDI modes of operation, namely those based on copper or fiber (1000BASE-X). This section outlines the supported combinations of these interfaces, as illustrated in Table 9.

Table 9 MII and MDI Combinations Supported by XWAY™ PHY11G

xMII Mode (Chapter 3.2.1)	MDI Mode (Chapter 3.3.1)			
	Copper (Chapter 3.3.1.1)			Fiber (Chapter 3.3.1.1)
	10BASE-T(e)	100BASE-TX	1000BASE-T	1000BASE-X
RMII	X	X		Fiber is only available in media-converter applications!
RGMII	X	X	X	
SGMII	X	X	X	
RTBI			X	

In general, a particular combination of MIIs and MDIs defines one of 2 different data flows:

- Copper flow
- Media-converter flow

The flows can be configured via pin-strapping (see Chapter 3.4.1) or after an EEPROM boot (see Chapter 3.4.2), and are controlled by means of the MDIO interface pins (see Chapter 3.4.3).

3.1.1 Copper Flow

In the copper flow, the XWAY™ PHY11G operates as a standard multi-speed twisted-pair copper PHY, according to the standards defining the 10BASE-T(e), 100BASE-TX and 1000BASE-T modes of operation on the MDI. All the xMII-supported MII interface types may be used to connect to a MAC-layer device. Note that the data rate of the MDI can be restricted by the MII type used. For example, the RMII does not support the higher rates of the 1000BASE-T mode, while the RTBI only supports the 1000BASE-T mode. Refer to **Table 9** for details.

3.1.2 Media Converter Flow

In this type of data-flow configuration, the XWAY™ PHY11G acts as an interface between a fiber-based MDI and a copper-based MDI. In this configuration, the device does not require a MAC connection. It can operate fully unmanaged, meaning that no management entity must be connected to the MDIO interface. The media-converter flow only supports the 1000 Mbit/s data rate, converting the flow of data between 1000BASE-X and 1000BASE-T. The XWAY™ PHY11G uses auto-negotiation to resolve the proper conversion configuration. The copper MDI is forced into the correct speed mode by restricting the auto-negotiation feature to using only 1000BASE-T in full-duplex and half-duplex mode.

3.2 Media-Independent Interfaces (MII)

This section describes the supported MIIs of the XWAY™ PHY11G. Each individual MII mode is investigated in detail and its particular requirements and properties are outlined.

3.2.1 X-speed Media-Independent Interface (xMII)

This section investigates all functional aspects of the xMII interface block.

3.2.1.1 xMII Signal Multiplexing

The XWAY™ PHY11G deals with the large variety of standard MAC interfaces (MIIs) by converting the different signaling schemes into native internal MII signals according to IEEE 802.3 **[1]**. This conversion is done by the xMII block on the XWAY™ PHY11G, as illustrated in **Figure 7**.

Table 10 summarizes the assignment of xMII pins to standard MAC interface signals according to **Chapter 2.2.4**.

Table 10 xMII Signal Multiplexing

Logic Port		xMII			SerDes	
Pin Name	**I/O**	**RMII**	**RGMII**	**RTBI**	**SGMII**	**1000BASE-X**
TX_CLK	I	REFCLK	TXC	TXC	SCP	
TXD3	I		TXD3	TXD38	SCN	SIGDET
TXD2	I		TXD2	TXD27	SOP	TDP
TXD1	I	TXD1	TXD1	TXD16	SON	TDN
TXD0	I	TXD0	TXD0	TXD05	SIP	RDP
TX_CTL	I	TX_EN	TX_EN_CTL	TXD49	SIN	RDN
RX_CLK	O	CLK50[1)]	RXC	RXC		
RX_CTL	O	CRS_DV	RX_DV_CTL	RXD49		
RXD3	O		RXD3	RXD38		
RXD2	O	RX_ER	RXD2	RXD27		
RXD1	O	RXD1	RXD1	RXD16		
RXD0	O	RXD0	RXD0	RXD05		

1) By default, a free-running 50 MHz clock is sourced at RX_CLK in RMII mode and can be used as REFCLK.

3.2.1.2 xMII Signal Conditioning

To reduce the cost in materials and effort for the PCB layout, the XWAY™ PHY11G supports extended signal conditioning on the xMII, as depicted in **Figure 8**. The high-speed MAC interface signals are internally conditioned such that only a straight strip wire is required to connect a MAC device to the XWAY™ PHY11G in the receive direction. In particular, this means that configurable series termination resistors are integrated into the driving pad. Additionally, the RX_CLK and TX_CLK pins implement an adjustable delay line that allows for skewing of the clock with respect to the data. This guarantees correct data samplings in both the MAC and PHY devices. For MAC devices that do not support internal signal conditioning, an appropriately dimensioned series resistance needs to be included on the PCB. Signal conditioning on the xMII is valid for all non-SerDes interfaces such as MII, GMII, RGMII, TBI and RTBI. However, the integrated delay is only intended for use with the RGMII and RTBI. In all other modes, the integrated ingress and egress delays are set to zero, but can be modified via the MDIO interface.

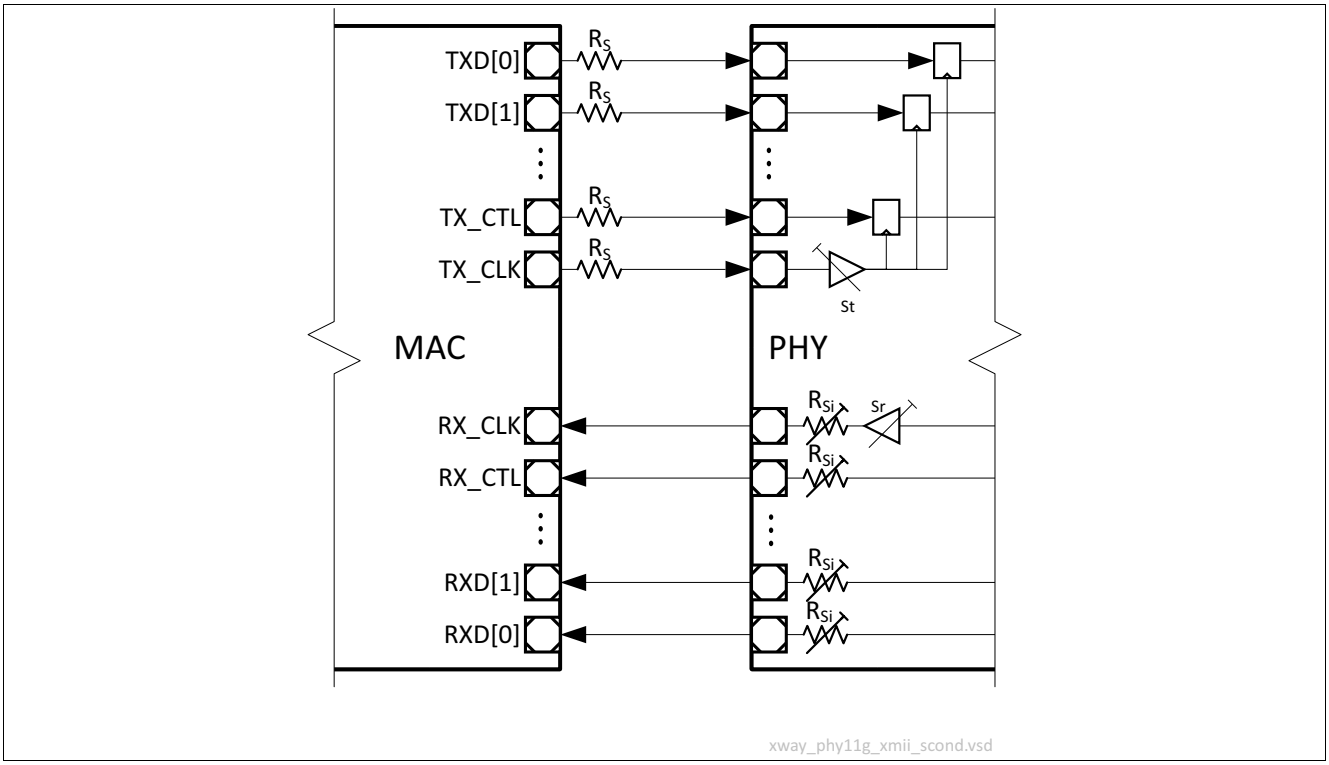


Figure 8 xMII Signal Conditioning between MAC and XWAY™ PHY11G

3.2.2 Reduced Media-Independent Interface (RMII)

The Reduced Media-Independent Interface (RMII) implements a MAC interface with a reduced pin count, but only supporting speeds of 10 Mbit/s and 100 Mbit/s. If the MAC interface is configured in RMII mode, then the XWAY™ PHY11G device does not negotiate 1000 Mbit/s functionality and therefore behaves like a fast Ethernet PHY. The RMII is fully compliant with the specification of the RMII consortium **[11]**. The pin-to-signals mapping is defined in **Table 10**. As a special feature of the XWAY™ PHY11G , the RX_CLK pin drives a continuous 50 MHz clock that can be used as the reference clock (CLK50). This clock is free-running and not locked to the receiver clock. The elastic buffering as required by **[11]** is performed in the PHY. The RX_CLK pin can be connected to the REFCLK pins of both the PHY and the MAC devices.

3.2.3 Reduced Gigabit Media-Independent Interface (RGMII)

The RGMII implements a MAC interface that can be used for all supported speeds, that is at 10 Mbit/s, 100 Mbit/s and 1000 Mbit/s, but with a reduced pin count when compared to a GMII. This interface is implemented according to the RGMIIv1.2 **[9]** and RGMIIv2.0[1)] **[10]** specification, and is therefore referred to as RGMII-ID. The mapping of standardized signals to device pins is defined in **Table 4**.

The transfer of data between the MAC and PHY devices is handled via a clock signal, a control signal and a four-bit data vector in both the transmit and receive directions. The clock signal is always driven by the signal source, that is the MAC in the transmit direction and the PHY in the receive direction. The control and data signals change with both the rising and falling edges of the driving clock. The nominal driving clock frequency at data speeds in gigabits is of 125 MHz. Lower speeds of 10 Mbit/s and 100 Mbit/s can be achieved by reducing the clock frequency to 2.5 MHz and 25 MHz respectively. At these speed grades, the higher half of the data octet has no content. Instead, the XWAY™ PHY11G device accepts a replicated version of TXD[3:0] on the falling clock edge, thus

1) HSTL logic drivers are not supported. Instead standard LVTTL drivers are used.

reducing power consumption. This is not possible for the TX_CTL and RX_CTL control signals, as these still need to multiplex the GMII_TX_EN/GMII_TX_ER and the GMII_RX_EN/GMII_RX_DV signals.

In order to reduce the power consumption on this interface, the RGMII specification defines a special coding of these control signals such that:

```
TX_EN = GMII_TX_EN
TX_ER = GMII_TX_EN XOR GMII_TX_ER
RX_EN = GMII_RX_EN
RX_ER = GMII_RX_DV XOR GMII_RX_ER
```

The TX_CTL signal transports the TX_EN subject to the rising edge, whereas TX_ER is driven by the falling edge of the TX_CLK. The RX_CTL signal is defined in the same way as TX_CTL. The exact encoding for TX_CTL and RX_CTL is depicted in **Table 11** and **Table 12**, respectively. As can be seen in **Table 12**, the XWAY™ PHY11G supports in-band status via RGMII.

The AC characteristics of the RGMII are specified in **Chapter 6.6.7**. In order to simplify PCB design, the XWAY™ PHY11G supports XMII signal conditioning between MAC and PHY, as described in **Chapter 3.2.1.2**. The clock signals can be delayed using a programmable skew value, in order to obtain a robust setup and hold the time relationships between the clock and the data/control signals at the receiving pins. The programmability of the skew value addresses the particularities of the given PCB environment in which the XWAY™ PHY11G device is embedded.

Supported test loops (**Chapter 3.6.3**) can be activated at any time. The speed at which the test loop operates depends on the state of the transceiver. Activating a test loop during an active link implies that the currently selected link speed, for example after auto-negotiation (**Chapter 3.3.2**) or auto-downspeed (**Chapter 3.3.3**) is used. Otherwise the test loop is operated at the speed grade specified by the registers (0.13) and (0.6).

Table 11 Transmit Control Encoding

TX_CTL	GMII_TX_EN	GMII_TX_ER	TXD[7:0]	Description
↑0↓0	0	0	00_H...FF_H	Normal inter-frame
↑0↓1	0	1	00_H	Reserved
↑0↓1	0	1	01_H	Low-power IDLE assert
↑0↓1	0	1	02_H...$0E_H$	Reserved
↑0↓1	0	1	$0F_H$	Carrier extend
↑0↓1	0	1	10_H...FE_H	Reserved
↑0↓1	0	1	$1F_H$	Carrier-extend error
↑0↓1	0	1	20_H...FF_H	Reserved
↑1↓1	1	0	00_H...FF_H	Transmit data frame
↑1↓0	1	1	00_H...FF_H	Transmit error propagation

Table 12 Receive Control Encoding

RX_CTL	GMII_RX_DV	GMII_RX_ER	RXD[7:0]	Description	PHY Status
↑0↓0	0	0	$xxx0xxx0_B$	Normal inter-frame	Link down
			$xxx1xxx1_B$		Link up
↑0↓0	0	0	$x00xx00x_B$	Normal inter-frame	RX_CLK = 2.5 MHz
			$x01xx01x_B$		RX_CLK = 25 MHz
			$x10xx10x_B$		RX_CLK = 125 MHz
			$x11xx11x_B$		Reserved

Table 12 Receive Control Encoding (cont'd)

RX_CTL	GMII_RX_DV	GMII_RX_ER	RXD[7:0]	Description	PHY Status
↑0↓0	0	0	$0xxx0xxx_B$	Normal inter-frame	Half-duplex mode
			$1xxx1xxx_B$		Full-duplex mode
↑0↓1	0	1	00_H	Reserved	
↑0↓1	0	1	01_H	Low-power IDLE assert	
↑0↓1	0	1	$02_H...0D_H$	Reserved	
↑0↓1	0	1	$0E_H$	False carrier indication	False carrier present
↑0↓1	0	1	$0F_H$	Carrier extend	EXTEND
↑0↓1	0	1	$10_H...FE_H$	Reserved	
↑0↓1	0	1	$1F_H$	Carrier-extend error	ZERO, ONE
↑0↓1	0	1	$20_H...FE_H$	Reserved	
↑0↓1	0	1	FF_H	Carrier sense	PLS_Carrier.Indicate
↑1↓1	1	0	$00_H...FF_H$	Receive data frame	ZERO, ONE
↑1↓0	1	1	$00_H...FF_H$	Receive data error	ZERO, ONE

3.2.4 Serial Gigabit Media-Independent Interface (SGMII)

The Serial Gigabit Media-Independent Interface (SGMII) implements a MAC interface that can be used for all supported speeds, namely 10 Mbit/s, 100 Mbit/s and 1000 Mbit/s. This interface is implemented according to the SGMII **[13]** specification. The mapping of the standardized signals to the device pins is shown in **Table 4**. Note that the integrated SGMII uses Clock and Data Recovery (CDR) to extract the TXCLK clock from the TX data. This significantly reduces cost and power. The RXCLK is driven as specified by the standard, but can be switched off via MDIO to reduce power, in case the MAC also supports CDR.

The AC characteristics of the SGMII are described in **Chapter 6.6.9**.

Supported test loops (**Chapter 3.6.3**) can be activated at any time.

The external circuitry required to connect the XWAY™ PHY11G properly via SGMII is described in **Chapter 6.8.6**.

3.2.5 Reduced Ten Bit Interface (RTBI)

The Reduced Ten Bit Interface (RTBI) implements a MAC interface that can be used solely for speeds of 1000 Mbit/s. This interface is implemented according to the RGMIIv1.2 **[9]** and RGMIIv2.0[1] **[10]** specifications, and is therefore referred to as an RTBI-ID interface. The mapping of the standardized signals to the device pins is shown in **Table 4**. The RTBI interface is simply a reduced version of the TBI interface.

In order to provide an RTBI-to-copper flow, a Physical Coding Sublayer (PCS) is integrated as defined in IEEE 802.3, clause 36 (**[1]**). This is because the RTBI interface is not a real MAC interface but already-encoded data. Therefore, the XWAY™ PHY11G integrates this PCS module in order to convert the TBI-based signals back to an on-chip GMII interface which is a defined interface for the copper-media PHY. The auto-negotiation of the MAC communicates with the intermediate PCS module instead of with the link partner. This scenario is similar to a GBIC application. The XWAY™ PHY11G performs auto-negotiation on both sides and ensures that important information is passed to either side, for example pause, duplex mode. In RTBI mode, the speed is naturally fixed to 1000 Mbit/s. Hence the auto-negotiation functionality of the PHY is forced to this speed for the copper media.

The same concept as described for copper is also used for fiber. The XWAY™ PHY11G operates the intermediate PCS in a manner that is transparent to the MAC.

1) HSTL logic drivers are not supported. Instead, standard LVTTL drivers are used.

The AC characteristics of the RTBI are described in **Chapter 6.6.8**. In order to simplify PCB design, the XWAY™ PHY11G supports XMII signal conditioning between MAC and PHY, as described in **Chapter 3.2.1.2**. The clock signals can be delayed using a programmable skew value, in order to obtain a robust setup and hold the time relationships between the clock and the data/control signals at the receiving pins. The programmability of the skew value addresses the particularities of the given PCB environment in which the XWAY™ PHY11G device is embedded.

Supported test loops (**Chapter 3.6.3**) can be activated at any time. The speed at which the test loop operates depends on the state of the transceiver. Activating a test loop during an active link implies that the currently selected link speed, for example after auto-negotiation (**Chapter 3.3.2**) or auto-downspeed (**Chapter 3.3.3**) is used. Otherwise the test loop is operated at the speed grade specified by the registers (0.13) and (0.6).

3.3 Media Functions

This chapter describes the media functions supported by the XWAY™ PHY11G.

3.3.1 Media-Dependent Interfaces (MDI)

This section describes the Media-Dependent Interfaces (MDIs) that are supported by the XWAY™ PHY11G.

3.3.1.1 Copper Interface

The Twisted-Pair Interface (TPI) of the XWAY™ PHY11G is fully compliant with IEEE 802.3 **[1]**. To facilitate low-power implementation and reduce PCB costs, the series resistors that are required to terminate the twisted-pair link to nominally 100 Ω are integrated into the device. As a consequence, the TPI pins (see **Chapter 2.2.3**) can be directly connected via the transformer to the RJ45 plug. Additional external circuitry is only required for proper common-mode termination and rejection. The electrical characteristics of the transformer and the plug are outlined in **Chapter 6.8.3** and **Chapter 6.8.4**, respectively. A high-level schematic of the TPI circuitry is shown in **Figure 9**, taking these components into account. The twisted-pair wires are connected to the RJ45 plug pins according to the specification in **[5]**. The common-mode external circuitry is described in **Chapter 6.8.5**.

Note that the twisted-pair port C is terminated with high-precision, high-ohmic resistors R_{CAL}, which are in turn connected to the common-mode ground. This configuration is only required for the port C and is used to auto-calibrate the IC after reset.

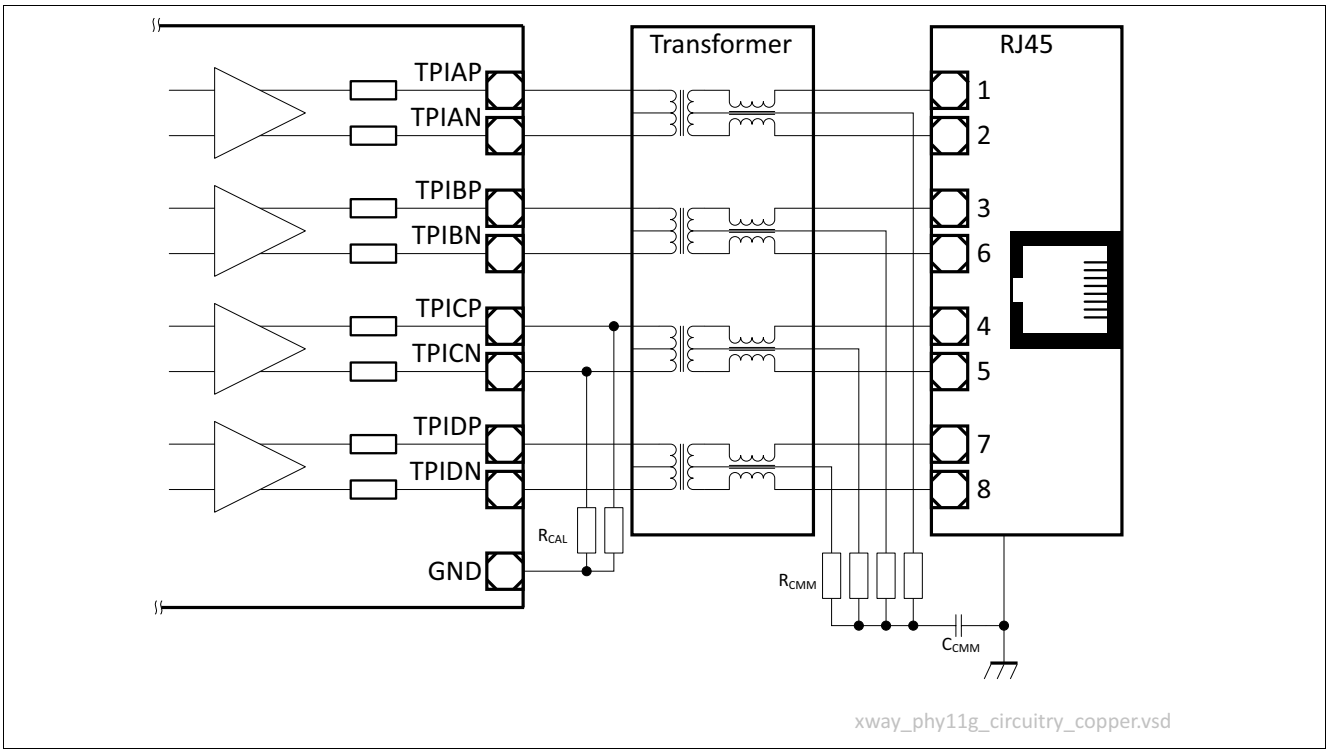


Figure 9 Twisted-Pair Interface of XWAY™ PHY11G Including Transformer and RJ45 Plug

3.3.1.2 Fiber Interface

Using the integrated SerDes module, the XWAY™ PHY11G supports fiber-based PHY Ethernet applications compliant with IEEE 802.3, clause 36 **[1]** (1000BASE-X). 1000BASE-X-specific auto-negotiation, according to IEEE 802.3 clause 37 **[1]**, is also supported. A signal-detect input is optionally available to indicate the signal status from the optics module to the XWAY™ PHY11G. This input is used in the particular case of dual-media applications, for auto-selection of the active interface. The external circuitry and wiring connection to the optics

module is specified in **Chapter 6.8.7**. Accordingly, **Chapter 6.6.10** specifies the timing characteristics of this interface.

Note that the integrated SerDes is compatible with both 1000 BASE-X and the SGMII standard, which in turn means that the differential high-speed pins can operate in both modes, depending on the configuration. However, since XWAY™ PHY11G integrates only one SerDes, this means that only one of these interface modes can be operated at any one time.

The fiber interface supports only speeds of 1000 Mbit/s; it is only compatible with gigabit-speed MIIs.

3.3.2 Auto-Negotiation

The XWAY™ PHY11G supports self-contained Auto-Negotiation (ANEG) as a startup procedure to exchange capability information with the link partner. Unless ANEG is manually disabled using the `MDIO.STD.CTRL.ANEN` register, the XWAY™ PHY11G will initiate each link-up using an ANEG procedure. This is recommended by the IEEE and essentially required for the 1000BASE-T mode.

ANEG is done after the following events:

- Power up
- Software power up (`MDIO.STD.CTRL.PD` = $\downarrow 0_B$)
- Hardware reset
- Software reset (`MDIO.STD.CTRL.RST` = $\downarrow 0_B$)
- Command to restart ANEG (`MDIO.STD.CTRL.ANRS` = $\uparrow 1_B$)
- Link-down

Unless otherwise configured, the XWAY™ PHY11G carries out an auto-crossover detect/enable procedure prior to the start of the ANEG process. This ensures optimal interoperability even in inadequate cable infrastructure environments. However, if ANEG is disabled, the auto-crossover procedure is still done during link-up. More details are given in **Chapter 3.3.4**.

The implementation of the ANEG procedure is compliant with the standards given in IEEE 802.3, clause 28 (**[1]**). If the link partner does not support ANEG, the XWAY™ PHY11G extracts the link-speed configuration using parallel detection. Once this is detected, the PHY links up at the speed of the link partner. Since the duplex mode cannot be extracted during parallel detection, the duplex mode is set to half-duplex, which also works in case the link partner operates in full-duplex mode. Since ANEG is a mandatory feature for 1000BASE-T transceivers, the XWAY™ PHY11G only does parallel detection for 10BASE-T and 100BASE-TX.

The default advertisements during ANEG are according to standard. **Chapter 3.4** specifies how these settings can be overwritten with other values.

The XWAY™ PHY11G supports Next Page (NP) exchange, since this is mandatory for advertising 1000BASE-T capabilities. By default, NPs are exchanged autonomously and do not require interaction with any management device. If no NPs are intended to be transmitted by the management device, the `MDIO.STD.AN_NPTX.NP` register bit should be set to logic 1_B.

If the XWAY™ PHY11G is configured in a particular MAC interface mode which does not support all PHY speeds, the ANEG-capability registers are automatically restricted to the MAC speeds possible. More details about the MAC interfaces and the supported speed modes are listed in **Table 9**.

When the XWAY™ PHY11G is configured to operate with a MAC via the SGMII, the SGMII also incorporates auto-negotiation on the MAC-to-PHY interface. This auto-negotiation is automatically initiated by the XWAY™ PHY11G whenever there are link-speed changes on the TPI. This means that, after ANEG is completed on the TPI-side, the link speed is advertised to the MAC via the SGMII ANEG capability.

3.3.3 Auto-Downspeed

The Auto-Downspeed (ADS) feature ensures maximum interoperability even in harsh or inadequate cable infrastructure environments. In particular, ADS is applied during 1000BASE-T training. This is necessary because the information available about the cabling during ANEG is insufficient. It is possible to advertise 1000BASE-T

during ANEG, even though it might happen that both link partners are connected via a CAT-3 cable, which does not support the 4-pair Gigabit Ethernet mode. In order to avoid continuous link-up failures in such a situation, the XWAY™ PHY11G operates a detection algorithm to identify this situation. As a consequence, Gigabit-capability indication is cleared from the ANEG registers. After the resulting link-down, the next ANEG process does not advertise 1000BASE-T anymore, such that even when the link partner does not implement this kind of ADS algorithm, the next link-up will be done at the next advertised speed below 1000 Mbit/s.

It can also happen that the existing cable infrastructure is adequate, but that the integrity of received signals is not suitable for a 1000BASE-T link-up, for example due to increased alien noise, or over-length cables. If such a condition is detected, the XWAY™ PHY11G also does an ADS procedure.

Finally, it can also happen that, even though the XWAY™ PHY11G is able to link up properly, for example in slave mode, the link partner is not able to. In this situation, ADS criterion described previously does not become active, but the link also never comes up. In order to address this corner situation, the XWAY™ PHY11G counts the number of attempts to link up to 1000BASE-T. If this number is greater than 3, the ADS procedure is carried out. This number is reset internally after each successful 1000BASE-T link-up.

In all flow and mode settings that support only speeds of 1000 Mbit/s, the ADS feature is automatically disabled.

3.3.4 Auto-Crossover and Polarity-Reversal Correction

In order to maximize interoperability even in inadequate wiring environments, the XWAY ™ PHY11G supports auto-crossover[1)] and polarity-reversal detection and correction. Both features are enabled by default.

Auto-crossover detection and correction operates at all supported twisted-pair speeds. The supported pair-mappings detectable and correctable by the device are listed in **Table 13**. However, in 10BASE-T and 100BASE-TX, pairs C and D are not used. Consequently, mode 2 and 3 as well as 1 and 4 are identical. However, in 1000BASE-T all modes are applicable.

The auto-crossover functionality is fully compliant with IEEE 802.3 **[1]**, clause 40.4.4, in 1000BASE-T mode. In the 10BASE-T and 100BASE-TX modes, this functionality depends on the detection of valid link pulses.

Table 13 Supported Twisted-Pair Mappings

Crossover Modes on a RJ45[1)]		RJ45 Pinning							
#	**Description**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
1	Normal, straight CAT5 cable	TPIAP **(A+)**	TPIAN **(A-)**	TPIBP **(B+)**	TPICP **(C+)**	TPICN **(C-)**	TPIBN **(B-)**	TPIDP **(D+)**	TPIDN **(D-)**
2	Fast Ethernet-only MDI-X	TPIBP **(B+)**	TPIBN **(B-)**	TPIAP **(A+)**	TPICP **(C+)**	TPICN **(C-)**	TPIAN **(A-)**	TPIDP **(D+)**	TPIDN **(D-)**
3	Full Gigabit Ethernet MDI-X	TPIBP **(B+)**	TPIBN **(B-)**	TPIAP **(A+)**	TPIDP **(D+)**	TPIDN **(D-)**	TPIAN **(A-)**	TPICP **(C+)**	TPICN **(C-)**
4	Normal, straight CAT5 cable with C/D pair-swap	TPIAP **(A+)**	TPIAN **(A-)**	TPIBP **(B+)**	TPIDP **(D+)**	TPIDN **(D-)**	TPIBN **(B-)**	TPICP **(C+)**	TPICN **(C-)**

1) Pin assignment according to TIA/EIA-568-A/B

Polarity-reversal errors caused by improper wiring are automatically corrected by the XWAY™ PHY11G. This correction is done on all pairs in the receive direction for all supported twisted-pair media modes. In 10BASE-T mode, the polarity correction is based on the detection of valid link pulses. In 100BASE-TX, the polarity of the receive signal is inherently corrected by the negation invariance of line code. In the 1000BASE-T mode, polarity detection is part of the training sequence. In all the modes, the detected polarity is frozen once the link has been established, and remains unchanged until the link is dropped.

1) A subset of this feature is also known as MDI/MDI-X from 10BASE-T and 100BASE-TX.

3.3.5 Transformerless Ethernet (TLE)

Transformer-Less Ethernet (TLE) is required for back-plane or PICMG applications, where the use of a transformer (magnetics) is not necessarily required in order to fulfill the galvanic-decoupling requirements of the isolation specifications. In such applications, removing the transformer reduces both the external bill of materials and the space requirements on the PCB.

As the XWAY™ PHY11G incorporates a novel type of voltage-mode line-driver, the only stringent requirement is to use AC coupling. AC coupling can be achieved using simple SMD-type series capacitors, the value of which is selected such that the high-pass characteristics correspond to an equivalent transformer-based standard application (recommended $C_{coupling}$ = 100 nF). The external circuitry for TLE is shown in **Figure 10**. Note that the RJ45 connector is shown only for illustration purposes. Back-plane applications use different connectors.

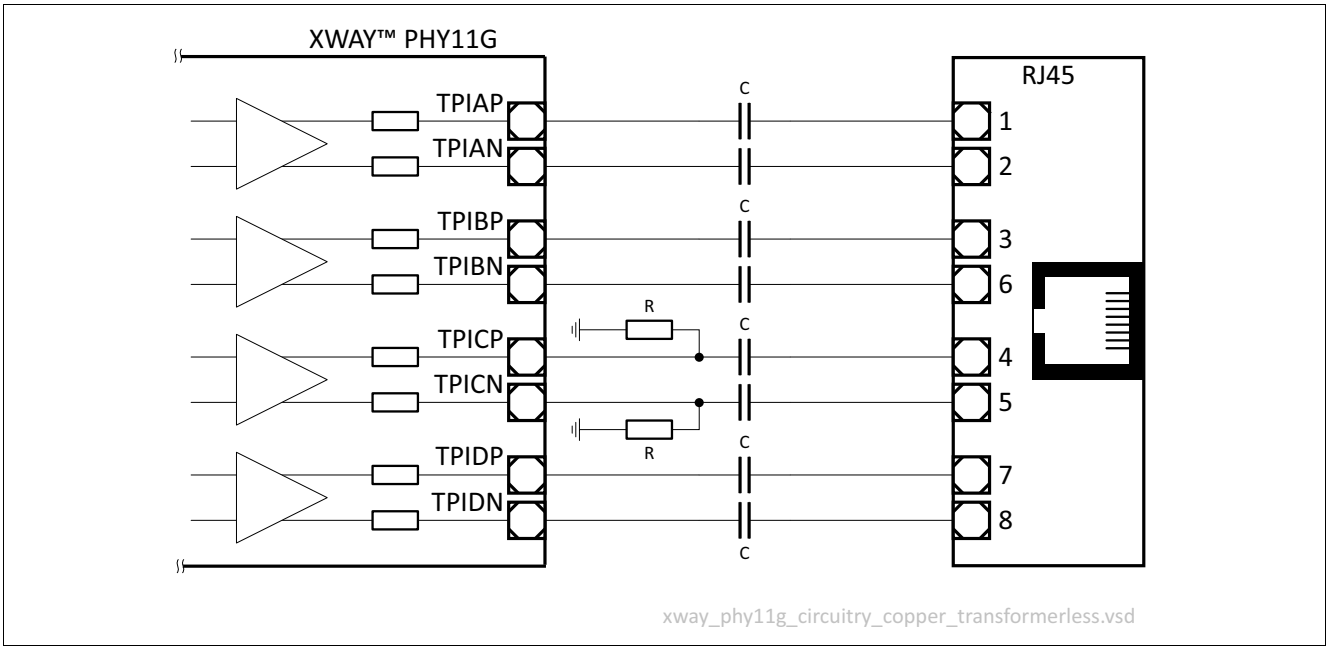


Figure 10 External Circuitry for the Transformerless Ethernet Application

If the XWAY™ PHY11G is to be connected to current-mode line-driver based Ethernet PHYs of another vendor, the circuitry for the current-mode line-driver must be properly selected. Proper selection of transformerless external circuitry for a current-mode line-driver based PHY is beyond the scope of this document. However, **Figure 11** outlines the circuitry for such a configuration. In particular, two separate PCB designs are shown, one for each type of line-driver technology (only channel A for simplicity). Both PCBs can be connected by means of a back-plane connector. The current-mode line-driver must provide a current-sinking voltage source in addition to AC coupling.

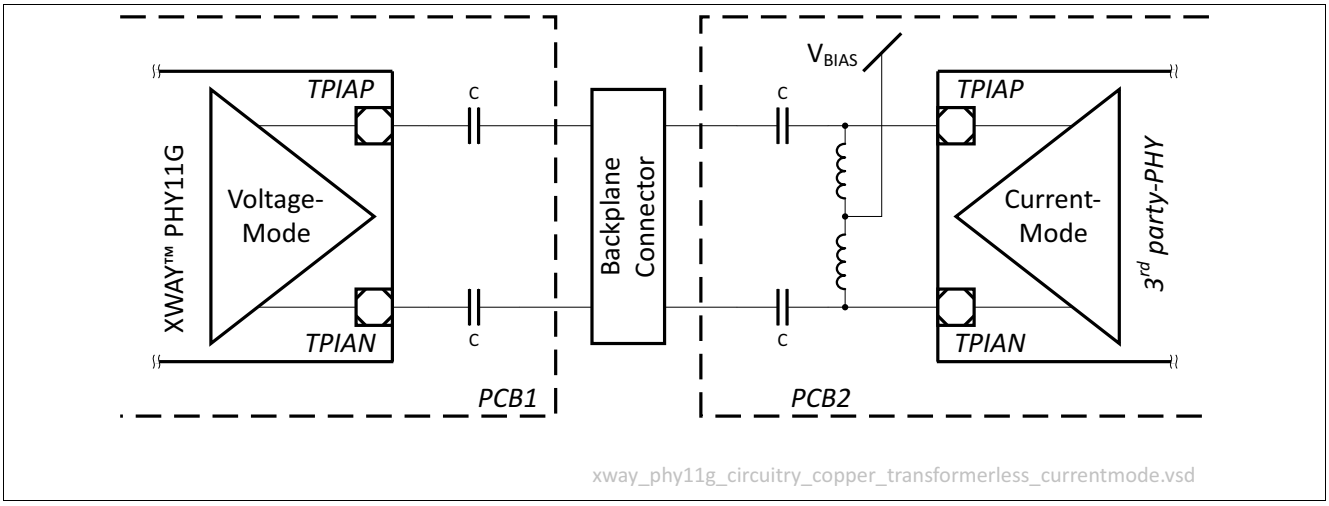


Figure 11 External Circuitry for TLE when Connected to Current-Mode Line-Driver Based PHY

3.4 Configuration, Control and Status Functions

This chapter investigates control and configuration of the XWAY™ PHY11G. It distinguishes between control and configuration operations. Configuration of the device can be done either via pin-strappings (**Chapter 3.4.1**) or via configuration content on an external EEPROM (**Chapter 3.4.2**). Configuration and control can be done using the MDIO interface (**Chapter 3.4.3.1**), according to IEEE 802.3 **[1]**. Furthermore, the chapter outlines how status information can be extracted from the XWAY™ PHY11G, either using the LED pins (**Chapter 3.4.4**), or by using a higher-level management entity on the MDIO interface together with an external interrupt (**Chapter 3.4.3.3**).

Figure 12 illustrates the configuration flow in the form of a flow chart. Note that configuration is only performed once after hardware reset or power-up. A simple software reset does not restart the configuration sequence. MDIO configuration and control access can only start after the configuration sequence has finished. The XWAY™ PHY11G indicates the time at which this is possible by clearing the MDIO reset register (`MDIO.STD.CTRL.RST` = 0_B).

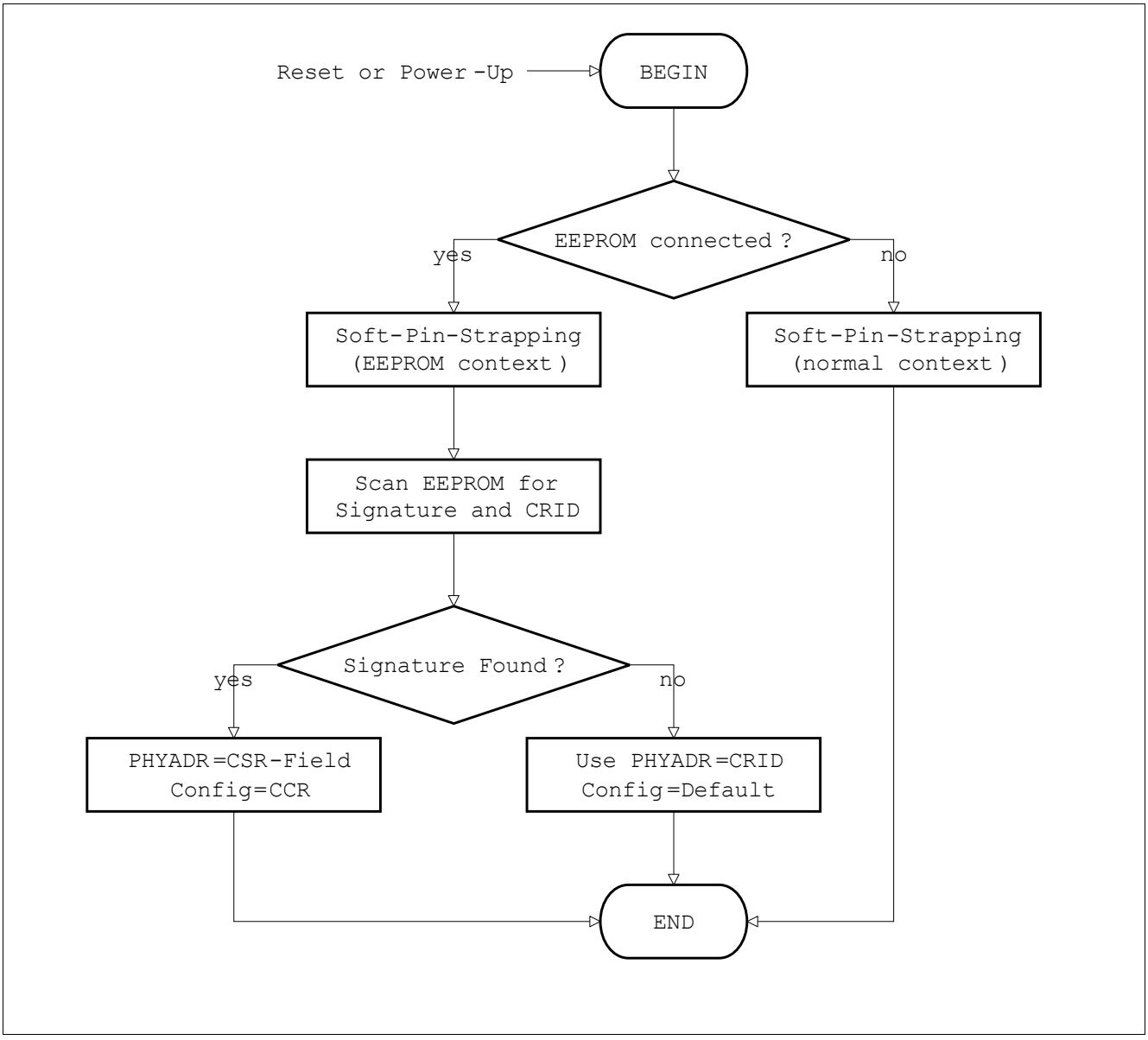


Figure 12 Overview of the Configuration Flow

3.4.1 Configuration of XWAY™ PHY11G via Pin-Strapping

This section describes the configuration of the XWAY™ PHY11G by means of pin-strapping. The limited pin count of the device means that reserving enough pins to encode all the configuration bits (by simply pulling these pins to V_{DDP} or V_{SS} in order to encode a logic one or zero respectively) is not an affordable option. Instead, the device supports soft pin-strapping using external resistors and capacitors[1]. Using this technology, an entire bit vector can be read on one pin, instead of just a single configuration bit. The content of the bit vector is determined by the component value of the pull-down resistor or capacitance used. The component value of this resistor is measured by the XWAY™ PHY11G shortly after reset. A schematic of the required external circuitry is shown in **Figure 13**.

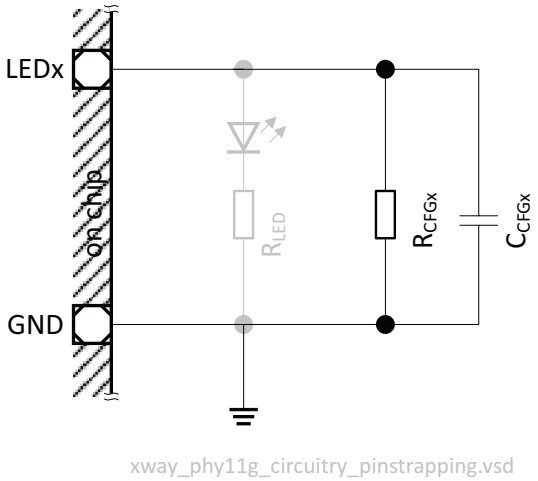


Figure 13 Soft Pin-Strapping External Circuitry

As shown in the figure, a further saving in pin count is achieved by sharing the pins used to drive LEDs (LEDx) with the pin-strapping configuration. The choice of soft pin-strapping configuration component values is such that normal LED operation is left unaffected. The LED components are shown in gray in **Figure 13**. Note that the pin-strapping passive components weakly tie the LEDx pin to the chip's ground. More details on the external circuitry for using LEDs can be found in **Chapter 3.4.4**.

A 4-bit vector is encoded by the appropriate choice the component values. The relationship between component values and the soft pin-strapping bit vector is shown in **Table 14**.

Table 14 Soft Pin-Strapping: Mapping of Pull-Down Capacitance/Resistor Values to Configuration Bits

Capacitance Value[1]	Resistor Value[2]	Soft Pin-Strapping Configuration Bit Vector CBV[3:0]			
		CBV[3]	CBV[2]	CBV[1]	CBV[0]
Not mounted, 0 nF	11.00 kΩ	0_B	0_B	0_B	0_B
	8.66 kΩ	0_B	0_B	0_B	1_B
	6.81 kΩ	0_B	0_B	1_B	0_B
	5.23 kΩ	0_B	0_B	1_B	1_B
	3.92 kΩ	0_B	1_B	0_B	0_B
	2.74 kΩ	0_B	1_B	0_B	1_B
	1.78 kΩ	0_B	1_B	1_B	0_B
	0.91 kΩ	0_B	1_B	1_B	1_B

1) The encoding of soft pin-strappings is such that the use of external capacitors is rarely needed.

Table 14 Soft Pin-Strapping: Mapping of Pull-Down Capacitance/Resistor Values to Configuration Bits

Capacitance Value[1]	Resistor Value[2]	Soft Pin-Strapping Configuration Bit Vector CBV[3:0]			
		CBV[3]	CBV[2]	CBV[1]	CBV[0]
Mounted, 100 nF	11.00 kΩ	1_B	0_B	0_B	0_B
	8.66 kΩ	1_B	0_B	0_B	1_B
	6.81 kΩ	1_B	0_B	1_B	0_B
	5.23 kΩ	1_B	0_B	1_B	1_B
	3.92 kΩ	1_B	1_B	0_B	0_B
	2.74 kΩ	1_B	1_B	0_B	1_B
	1.78 kΩ	1_B	1_B	1_B	0_B
	0.91 kΩ	1_B	1_B	1_B	1_B

1) A maximum tolerance of 10% on temperature and aging must be guaranteed. Ceramic-type capacitors are suggested.
2) A maximum tolerance of 1% on temperature and aging must be guaranteed. Resistances are taken from the E96 series.

The soft pin-strapping configuration is read from all three LED pins after device reset. It is possible to encode a total of 12 information bits. **Table 15** outlines the mapping of bits to the supported pin-strapping device parameters. In this table, each row represents a bit vector read from one of the configuration pins. Each column corresponds to a bit position in the configuration bit vector. Note that this table is only valid in the case that no EEPROM is connected to the XWAY™ PHY11G. If a configuration EEPROM is connected, the soft pin-strapping device parameters are mapped to different functions, as described in **Table 17**. **Chapter 3.4.2** gives more details on EEPROM-based device configuration.

Table 15 Mapping of Configuration Pins/Bits to Device Parameters (No EEPROM Connected)

Configuration Pin	CBV[3:0] associated by resistor value according to Table 14			
	CBV[3]	CBV[2]	CBV[1]	CBV[0]
LED0	MDIOADR[3]	MDIOADR[2]	MDIOADR[1]	MDIOADR[0]
LED1	MDIOADR[4]	MODE[1]	MODE[0]	FLOW
LED2	CONF[1]	CONF[0]	ANEG[1]	ANEG[0]

The functions of the device parameters mapped in **Table 15** are described in **Table 16**.

Table 16 Functions of Device Parameters Controlled by Soft Pin-Strapping (No EEPROM Connected)

Device Parameter	Function
MDIOADR[4:0]	Sets the MDIO PHY address to which the XWAY™ PHY11G responds during MDIO transactions.
FLOW	Specifies the signal flow of the XWAY™ PHY11G. 0_B **Copper** MAC interface to twisted-pair mode 1_B **Converter** converts fiber (1000BASE-X, SerDes) to twisted pair

Table 16 Functions of Device Parameters Controlled by Soft Pin-Strapping (No EEPROM Connected)

Device Parameter	Function
MODE[1:0]	Configures the functional mode of the XWAY™ PHY11G. The meaning of these bits depends on the FLOW setting. **FLOW = Copper:** 00_B **RGMII** - the MAC connects to the XWAY™ PHY11G via RGMII 01_B **SGMII** - the MAC connects to the XWAY™ PHY11G via SGMII 10_B **RMII** - the MAC connects to the XWAY™ PHY11G via RMII 11_B **RTBI** - the MAC connects to the XWAY™ PHY11G via RTBI **FLOW = Converter:** 00_B **X2T1000** - convert 1000BASE-X to 1000BASE-T 01_B **X2T1000A** - convert 1000BASE-X (with ANEG) to 1000BASE-T 10_B **reserved** 11_B **reserved**
CONF[1:0]	Used to specify the transmit and receive timing skew in the RGMII mode using the integrated delay generation on TX_CLK/RX_CLK. The meaning of these bits depends on the FLOW setting.[1)] **FLOW = Copper:** $X0_B$ **RGMII_TXSKEW_1N5** - Transmit timing skew is 1.5 ns $X1_B$ **RGMII_TXSKEW_0N0** - Transmit timing skew is 0.0 ns $0X_B$ **RGMII_RXSKEW_1N5** - Receive timing skew is 1.5 ns $1X_B$ **RGMII_RXSKEW_0N0** - Receive timing skew is 0.0 ns
ANEG[1:0]	Configures the auto-negotiation behavior of the XWAY™ PHY11G. The meaning of these bits depends on the FLOW setting. **FLOW = Copper:** 00_B **DEFAULT** - advertise 10/100/1000 Mbit/s in both full and half duplex 01_B **FASTHDX** - advertise 10/100 Mbit/s in half duplex and 1000 Mbit/s in in both full and half duplex 10_B **GIGAONLY** - advertise only 1000 Mbit/s in both full and half duplex 11_B **FASTONLY** - advertise only 10/100 Mbit/s in both full and half duplex **FLOW = Converter:** 00_B **reserved** 01_B **reserved** 10_B **reserved** 11_B **reserved**

1) The initial duplex mode is determined by the default value of `MDIO.STD.CTRL.DPLX`.

Table 17 Mapping of Configuration Pins/Bits to Device Parameters (EEPROM is Connected)

Configuration Pin	CBV[3:0] associated by resistor value according to Table 14			
	BV[3]	BV[2]	BV[1]	BV[0]
LED0	0_B	SPEED[1]	SPEED[0]	ADRMODE
LED1	SIZE[1]	DEVADR[2]	DEVADR[1]	DEVADR[0]
LED2	SIZE[0]	CRID[2]	CRID[1]	CRID[0]

The functions of the device parameters mapped in **Table 17** are defined in **Table 18**.

Table 18 Functions of Device Parameters controlled by Soft Pin-Strapping (EEPROM is Connected)

Device Parameter	Function
ADRMODE	**Specifies the EEPROM Addressing Mode** 0_B **11-bit** EEPROM addressing mode (see also **Chapter 3.4.2.4.1**) 1_B **16-bit** EEPROM Addressing Mode (see also **Chapter 3.4.2.4.2**)
DEVADR[2:0]	**Specifies the EEPROM Device Address** The device address can be specified in case multiple EEPROM devices are connected to the same I^2C bus. The valid mapping of device address bits into the frame is specific to the ADRMODE (see **Chapter 3.4.2.4** for more details). In general, the DEVADR bits are mapped MSB-aligned into bits 3:1 of the I^2C instruction field. Note that some larger devices in 11-bit mode also use these bits for internal addressing. The XWAY™ PHY11G supports this feature, meaning that the DEVADR is OR-combined with the corresponding memory address bits. It is important to apply logic zeros wherever this overlap is present. In 11-bit addressing mode there are overlays for EEPROMs with a capacity larger than 4 kb.
CRID[2:0]	**Specifies the Configuration Record ID** The configuration record ID can be specified in case multiple PHYs source information from an EEPROM device, in which case this contains multiple configuration record ID entries. The CRID is part of the configuration record ID header, allowing for storage of one distinct record for each PHY accessing the EEPROM (see **Chapter 3.4.2.4** for more details). Note that in case the CRID is not found in the EEPROM, the XWAY™ PHY11G uses the specified CRID as the MDIO address, with the two MSBs set to zero.

Table 18 Functions of Device Parameters controlled by Soft Pin-Strapping (EEPROM is Connected)

Device Parameter	Function
SPEED[1:0]	**Specifies the EEPROM Access Speed** 00_B **STANDARD** - EEPROM is accessed at F_{SCL} = 100 kHz serial clock speed 10_B **FASTMODE** - EEPROM is accessed at F_{SCL} = 400 kHz serial clock speed 01_B **MEGASPEED** - EEPROM is accessed at F_{SCL} = 1 MHz serial clock speed 11_B **HIGHSPEED** - EEPROM is accessed at F_{SCL} = 3.4 MHz serial clock speed
SIZE[1:0]	**Specifies the EEPROM Scan Size** This parameter defines the EEPROM scan size, which is the address range of the EEPROM in which the configuration record (more details in **Chapter 3.4.2.3**) is searched for during boot-up or after reset of the XWAY™ PHY11G. The physical size of the EEPROM is less important. The configuration signature record may contain pointer addresses to an address beyond the limit specified here. The scan starts at EEPROM address 0000_H. In order to yield a constant worst-case scan time over all supported EEPROM scan sizes, the address increment for the EEPROM configuration record scan is adjusted automatically, depending on the scan size, as follows: **ADRMODE = 0_B:** SIZE[1:0] = 00_B**<2 kb** - scan up to 256-byte addresses in steps of 32 SIZE[1:0] = 01_B**4 kb** - scan up to 512-byte addresses in steps of 64 SIZE[1:0] = 10_B**8 kb** - scan up to 1024-byte addresses in steps of 128 SIZE[1:0] = 11_B**16 kb** - scan up to 2048-byte addresses in steps of 256 **ADRMODE = 1_B:** SIZE[1:0] = 00_B**32 kb** - scan up to 4096-byte addresses in steps of 512 SIZE[1:0] = 01_B**64 kb** - scan up to 8192-byte addresses in steps of 1024 SIZE[1:0] = 10_B**128 kb** - scan up to 16384-byte addresses in steps of 2048 SIZE[1:0] = 11_B**>256 kb** - scan up to 32768-byte addresses in steps of 4096

3.4.2 Configuration of XWAY™ PHY11G via External EEPROM

This chapter describes the operation of the XWAY™ PHY11G with an externally connected EEPROM.

3.4.2.1 EEPROM Applications

Connection of an external EEPROM is used to enable the implementation of systems without any higher-level management entity to drive the control and configuration information on the MDIO interface (see **Chapter 3.4.3**). In addition, it is not possible to completely configure XWAY™ PHY11G functionality using only the soft pin-strapping interface (see **Chapter 3.4.1**). In such applications, the external EEPROM provides a cheap and efficient solution for storing all the configuration information that needs to be loaded by the XWAY™ PHY11G during startup.

The XWAY™ PHY11G supports various EEPROM devices by means of its I^2C interface (see **Chapter 2.2.5**, pins SDA and SCL). The devices supported are listed in **Table 19**. Devices from other silicon vendors that are not listed in **Table 19** and which support I^2C may also be supported, but are not tested by Lantiq.

Table 19 Supported EEPROM Devices

Vendor	Device	Remark
AMTEL	AT24Cxx	Proper size selection by customers
CATALYST	CAT24Cxx	Proper size selection by customers
STM	M24Cxx	Proper size selection by customers

In the simplest application, the EEPROM is only used to store configuration information of the XWAY™ PHY11G. In particular, this contains the defaults for the internal MDIO registers. This configuration is loaded by the XWAY™ PHY11G directly after reset or power-up if an EEPROM has been detected. In order to support the sharing of a larger EEPROM device by several master devices, for example if an additional microcontroller also loads its configuration from the same device, the XWAY™ PHY11G scans the EEPROM content for a particular signature that corresponds to its configuration record. The XWAY™ PHY11G loads this configuration record and overrides its internal defaults. A detailed description of the configuration record is given in **Chapter 3.4.2.3**.

A more sophisticated type of application is used to enhance the functionality of the XWAY™ PHY11G by loading embedded firmware from the external EEPROM. The integrated device controller on the XWAY™ PHY11G is able to execute code from the external EEPROM. In order to reduce the load on the I^2C interface, this code is loaded into the XWAY™ PHY11G before execution. It is possible to change the existing functionality by modifying parts of the integrated firmware, as well as to extend its functionality by adding new firmware blocks. Dedicated support from Lantiq is required for this type of feature. The externally embedded firmware is also stored within the configuration record. Further details are specified in **Chapter 3.4.2.3**.

3.4.2.2 EEPROM Detection

The XWAY™ PHY11G automatically detects whether or not an external EEPROM is connected, by sensing the SDA pin during startup. Since the SDA pin is equipped with an internal pull-up resistor to comply with the I^2C specification, it is assumed that an EEPROM is connected when this pin is sensed as being at logic 1_B after reset. In case no external EEPROM is connected, it is required that this pin be pulled to ground, and thus sensed internally as being at 0_B after reset.

Attention: The SDA pin must not be left floating!

In case an EEPROM has been detected, the soft pin-strapping pins are used to properly configure the EEPROM. This includes information about speed, address mode, and slave device address. Refer to **Chapter 3.4.1** for more information.

If the XWAY™ PHY11G evaluates the SDA pin and detects an EEPROM device, it tries to access the EEPROM device by initiating a single byte read. If the device is present and understands the I^2C format, it will acknowledge

the read instruction after a certain amount of time. The XWAY™ PHY11G waits for this acknowledgement, and if none is received before a time-out, the attempt to access the EEPROM is aborted and no compatible device is assumed to be connected to the I^2C interface.

However, if the acknowledgement is successfully received, the XWAY™ PHY11G starts scanning the EEPROM content for a specific signature at the beginning of the Configuration Signature Record (CSR). The setup of the CSR is specified in **Table 20**. The signature is a sequence of predefined bytes: EE_H,$C0_H$,DE_H,$1F_H$. The XWAY™ PHY11G scans the entire EEPROM at address locations of k * STEP within the range of the predefined EEPROM size (see SIZE[3:0] in **Chapter 3.4.1**, **Table 17**). The STEP size is equal to SIZE / 64, so that for a 1 kb EEPROM the STEP size is STEP = 8 bytes. If no signature is found, the XWAY™ PHY11G aborts the search and skips any further EEPROM read operations. If a signature is detected, the XWAY™ PHY11G reads the CSR. Note that the CSR contains the PHYADR that is used for MDIO communication (see **Chapter 3.4.3.1**). The MDIO address is used only after the CSR has been successfully read by the XWAY™ PHY11G. Before this, the MDIO address is by default at logic 00000_B.

3.4.2.3 EEPROM Content

Table 20 depicts the Configuration Signature Record (CSR), containing the signature as well as several addresses. The signature is used to identify a part of the EEPROM content to be dedicated to the XWAY™ PHY11G, in case several different devices share the same memory. The subsequent byte contains the CRID that is dedicated to a single XWAY™ PHY11G in case multiple XWAY™ PHY11G devices retrieve configuration data from the same EEPROM. The subsequent fields are only evaluated if the CSR and the configuration record ID match. The CRID must match the value specified by the pin-strapping configuration (see also **Chapter 3.4.1**). The first address contained in the CSR is the PHYADR used to address the MDIO messages to the correct device, in case the MDIO is shared. More details can be found in **Chapter 3.4.3.1**. If no CSR is found during the scan process, the MDIO address is set internally to PHYADR[4:3] = 00_B, PHYADR[2:0] = CRID[2:0]. The subsequent field contains the Configuration Content Record (CCR) base address (CCR_ADR), which is a 16-bit pointer address pointing to the start address location of the CCR on the same EEPROM, as defined in **Table 21**. In case no CCR exists, the CCR_ADR must be set to $FFFF_H$. The 2 bytes following the CCR_ADR field are reserved for internal use and must be set to $FFFF_H$.

Table 20 Configuration Signature Record (CSR)

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
k * STEP + 0	1	1	1	0	1	1	1	0	**Configuration Record Signature**: EE_H,$C0_H$,DE_H,$1F_H$
k * STEP + 1	1	1	0	0	0	0	0	0	
k * STEP + 2	1	1	0	1	1	1	1	0	
k * STEP + 3	0	0	0	1	1	1	1	1	
k * STEP + 4	0	0	0	0	0	CRID[2:0]			Configuration record ID
k * STEP + 5	0	0	0	PHYADR[4:0]					PHY MDIO address
k * STEP + 6	CCR_ADR[15:8]								Configuration Content Record (CCR) base address. This vector must be set to CCR_ADR = $FFFF_H$ if no CCR exists.
k * STEP + 7	CCR_ADR[7:0]								
k * STEP + 8	1	1	1	1	1	1	1	1	Reserved for future use.
k * STEP + 9	1	1	1	1	1	1	1	1	Reserved for future use.

1) This is the byte-wise EEPROM address. The scheme is independent of the address mode used (11/16)

Table 21 Configuration Content Record

Address[1]	Content								Comment
	7	6	5	4	3	2	1	0	
CCR_ADR + 0	NOCE[7:0]								Number of configuration entries. A value of 00_H corresponds to 1 entry. A value of FF_H corresponds to 256 entries.
CCR_ADR + 1	ADDR(1)[7:0]								Address (MDIO address) and configuration data word (MDIO data) for entry 1
CCR_ADR + 2	DATA(1)[15:8]								
CCR_ADR + 3	DATA(1)[7:0]								
CCR_ADR + 4	ADDR(2)[7:0]								Address (MDIO address) and configuration data word (MDIO data) for entry 2
CCR_ADR + 5	DATA(2)[15:8]								
CCR_ADR + 6	DATA(2)[7:0]								
CCR_ADR + ...	...								...
CCR_ADR + 3 * NOCE + 1	ADDR(NOCE)[7:0]								Address (MDIO address) and configuration data word (MDIO data) for entry #NOCE
CCR_ADR + 3 * NOCE + 2	DATA(NOCE)[15:8]								
CCR_ADR + 3 * NOCE + 3	DATA(NOCE)[7:0]								

1) This is the byte-wise EEPROM address. The scheme is independent of the address mode used (11/16)

3.4.2.4 EEPROM Frame Formats

This chapter specifies the EEPROM frame formats supported. In particular, a subset of the I^2C protocol is represented which is supported by most of the EEPROM devices on the market. In order to comply with almost all EEPROM devices currently available on the market, and in particular with larger sizes, two addressing modes are supported: 11-bit addressing and 16-bit addressing. Note that this addressing relates to the EEPROM internal data addressing and not to the I^2C device address mode. For the latter, the XWAY™ PHY11G only supports the standard 7-bit device address mode. In compliance with most of the available EEPROM devices, the default value of the device address is DADR[7:1] = $1010XXX_B$. The last three bits are configurable using the soft pin-strappings (see **Chapter 3.4.1**), which also contain a configuration bit for the addressing mode. The following sections specify the frame formats for both addressing modes. Mixed addressing mode operation is not supported by the XWAY™ PHY11G.

3.4.2.4.1 Frame Formats in 11-Bit Addressing Mode

This addressing mode is used for the smallest available EEPROM devices. These devices are usually available in sizes ranging from 1 kb to 16 kb. Since the EEPROM devices are organized in 8-bit words, this requires between 7 and 11 address bits. However, only one address byte is defined following the I^2C instruction. Therefore, for larger EEPROM configurations, it is common practice to use up to 3 LSBs of the device address within the I^2C instruction to map these missing 3 bits. This is also illustrated in the frame structures specified in this chapter. In order to clarify this further, **Table 22** lists the address mappings for all supported EEPROM sizes.

Table 22 Address Bit Mapping in 11-Bit Addressing Mode

EEPROM Size	I²C Instruction Bit							Memory Content Address Byte							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1 kb	1010D				ADR[2:0]			0	ADR[6:0]							
2 kb					DADR[2:0]			ADR[7:0]								
4 kb					DADR[2:1]			ADR[8:0]								
8 kb					[2]1)			ADR[9:0]								
16 kb					ADR[10:0]											

1) DADR[2]

Figure 14 shows the 3-byte frame format for a single-byte write operation to a random address on the EEPROM. For maximum compatibility, this is the only write frame format supported. Following a start bit (a falling edge on SDA while SCL is active high), the I²C instruction is sent, containing the default device address DADR[7:1] = $1010XXX_B$ that is applicable to almost all EEPROM devices available. The last bit in the instruction is a read/write bit which is set to low to indicate a write transaction. The instruction byte is followed by an acknowledgement driven by the EEPROM. Following this acknowledgement, the XWAY™ PHY11G drives the memory address byte ADR[7:0], which also needs to be acknowledged by the EEPROM. The last of the three bytes in the write operation frame contains the data byte to be written, DATA[7:0]. After a successful write operation, this byte is acknowledged by the EEPROM and the XWAY™ PHY11G ends the write operation frame with a stop bit. In accordance with I²C, this stop bit is a rising edge on SDA while SCL is active high.

Table 22 showed how some devices exceed the address byte and therefore have to use parts of the device address. This is indicated in **Figure 14** by showing the assignment of the ADR[10:8] bits.

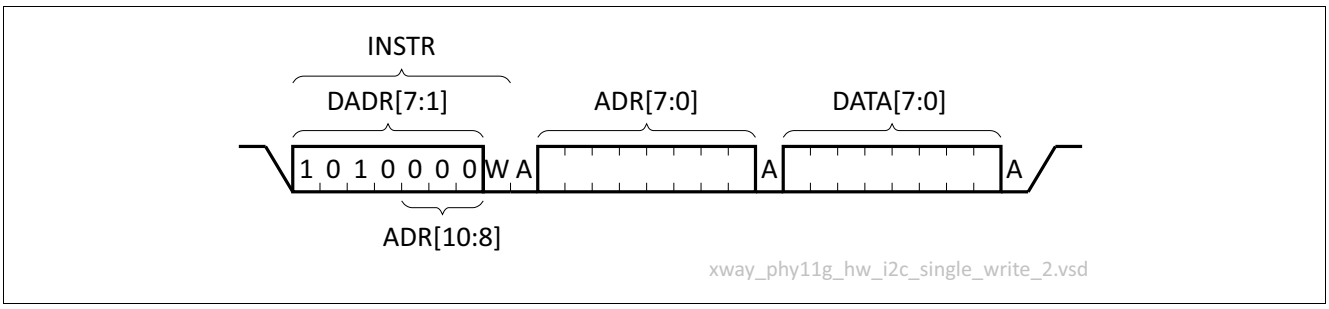


Figure 14 Timing Diagram for a Random Address Single Byte Write

Figure 15 shows a read frame similar to the write frame operation illustrated in **Figure 14**. In general, a read frame starts with a dummy write frame which lasts up to the write address. This is required to set the current address on the EEPROM. After acknowledgement of the address byte ADR[7:0], the XWAY™ PHY11G terminates the current dummy write by setting a new start bit. The instruction byte is repeated, except that the read/write bit is now set to active high to indicate that this instruction corresponds to a read access. Following acknowledgement of the read request, the EEPROM drives the desired read data byte DATA[7:0]. For a single read operation, the XWAY™ PHY11G does not acknowledge this byte, indicating that no further read is required. The read access is completed by the XWAY™ PHY11G driving the stop bit to SDA.

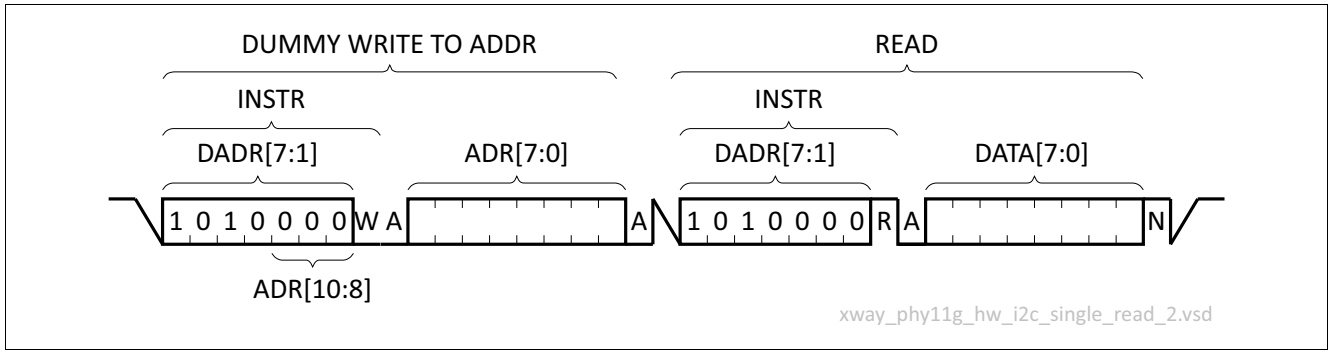


Figure 15 Timing Diagram for a Random Address Single Byte Read

A single-byte random read as depicted in **Figure 15** can easily be extended to a burst read. **Figure 16** shows the supported burst read frame structure. Note that the initialization of a burst-read access is the same as for a single-byte read. Therefore, the figure only shows the protocol sequence starting from the read instruction. Subsequent bytes are read from incrementing address locations, for as long as the XWAY™ PHY11G keeps acknowledging the read bytes driven by the EEPROM. The burst read access stops when the XWAY™ PHY11G does not acknowledge a read byte and instead issues the stop bit. The XWAY™ PHY11G uses the burst read operation only for the external firmware load feature. Normal configuration EEPROM-access operations are done using single-byte read/write operations.

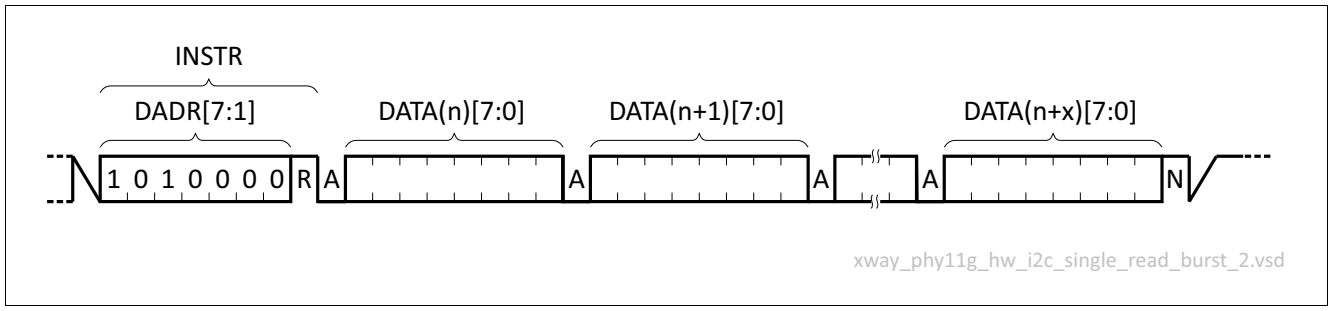


Figure 16 Timing Diagram for a Burst Read

3.4.2.4.2 Frame Formats in 16-Bit Addressing Mode

This addressing mode is used for the larger available EEPROM devices. These devices are usually available in sizes ranging from 32 kb up to 512 kb. Since the EEPROM devices are organized in 8-bit words, this requires 12 to 16 address bits. The larger storage space can be used for customized firmware code or for sharing among several devices by using I^2C functionality. In contrast to the 11-bit addressing mode, the 16-bit addressing mode uses two bytes following the I^2C instruction to encode the memory address. The three LSBs of the device address are available for selecting one out of eight EEPROM devices attached to the same I^2C serial bus. This device address is configurable using the soft pin-strappings as described in **Chapter 3.4.1**. In order to clarify this further, **Table 23** lists the address mappings for all supported EEPROM sizes.

Table 23 Address Bit Mapping in 16-Bit Addressing Mode

EEPROM Size	I²C Instruction Bit							1st Memory Content Address Byte								2nd Memory Content Address Byte							
	7	6	5	4	3	2	1	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
32 kb	1	0	1	0	X	X	X	0	0	0	0	ADR[11:0]											
64 kb					X	X	X	0	0	0	ADR[12:0]												
128 kb					X	X	X	0	0	ADR[13:0]													
256 kb					X	X	X	0	ADR[14:0]														
512 kb					X	X	X	ADR[15:0]															

Figure 17 shows the 4-byte frame format for a single-byte write operation to a random address on the EEPROM. For maximum compatibility, this is the only write frame format supported. Following a start bit (a falling edge on SDA while SCL is active high), the I²C instruction is sent, containing the default device address DADR[7:1] = $1010XXX_B$ that is applicable to almost all EEPROM devices available. The last bit in the instruction is a read/write bit which is set to low to indicate a write transaction. The instruction byte is followed by an acknowledgement driven by the EEPROM. Following this acknowledgement, the XWAY™ PHY11G drives the memory address bytes ADR[15:8] and ADR[7:0], both of which are also separately acknowledged by the EEPROM. The last of the four bytes in the write operation frame contains the data byte to be written, DATA[7:0]. After a successful write operation, this byte is acknowledged by the EEPROM, and the XWAY™ PHY11G ends the write frame with a stop bit (a rising edge on SDA while SCL is active high).

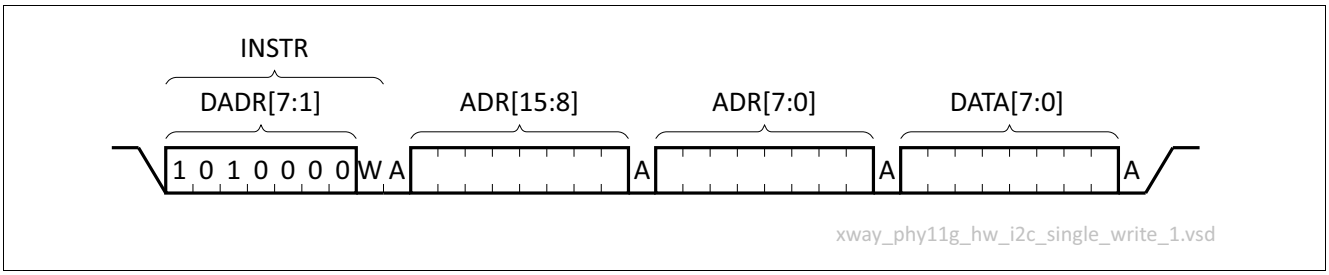


Figure 17 Timing Diagram for a Random Address Single Byte Write

Figure 18 shows a read frame similar to the write frame protocol illustrated in **Figure 17**. In general a read frame starts with a dummy write frame which lasts up to the write address. This is required to set the current address on the EEPROM. After acknowledgement of the address byte ADR[7:0], the XWAY™ PHY11G terminates the current dummy write by setting a new start bit. The instruction byte is repeated, except that the read/write bit is now set to active high to indicate that this instruction corresponds to a read access. Following acknowledgement of the read request, the EEPROM drives the desired read data byte DATA[7:0]. For a single read operation, the XWAY™ PHY11G does not acknowledge this byte, indicating that no further read is required. The read access is completed by the XWAY™ PHY11G driving the stop bit to SDA.

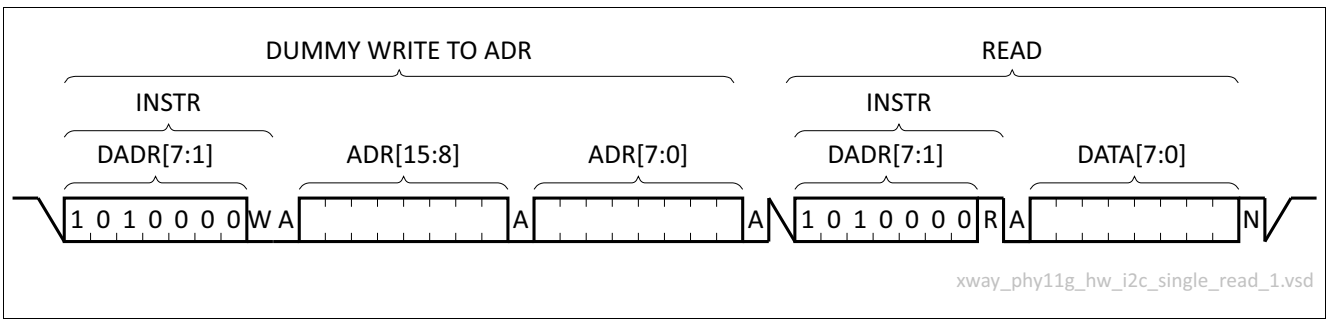


Figure 18 Timing Diagram for a Random Address Single Byte Read

A single-byte random read as depicted in **Figure 18** can easily be extended to a burst read. **Figure 19** shows the supported burst read frame structure. Note that the initialization of a burst-read access is the same as for a single-byte read. Therefore, the figure only shows the protocol sequence starting from the read instruction. Subsequent bytes are read from incrementing address locations, for as long as the XWAY™ PHY11G keeps acknowledging the read bytes driven by the EEPR OM. The burst read access stops when the XWAY™ PHY11G does not acknowledge a read byte and instead issues the stop bit. The XWAY™ PHY11G uses the burst read operation only for the exte rnal firmware load feature. Normal configuration EEPROM-access operations are done using single-byte read/write operations.

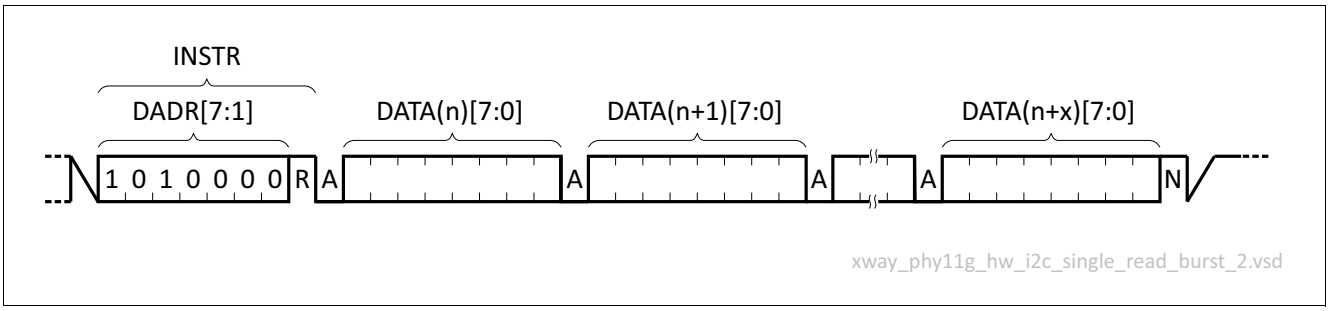


Figure 19 Timing Diagram for a Burst Read

3.4.2.4.3 EEPROM Access via MDIO

The XW AY™ PHY11G supports indirect access to the EEPROM via the MDIO interface. A special type of handshaking between the higher-level management entity and PHY is required for proper cycle-time arbitration. The flow charts in **Figure 20** and **Figure 21** illustrate this handshake mechanism for a write and a read cyc le respectively. Note that only single-byte accesses are supported, as opposed to EEPROM burst-mode options, for better compatibility and simplicity. As can be seen from the flow charts, the first action before any operation is to check whether the EEPROM is busy or ready to use. This is done usingthe `PHY.EECTRL.EXEC` bit. This bit could still be set from a past write cycle or other internal means, preventing a current EEPROM access. Any access to the EEPROM is performe d via MMD on device $1E_H$. The entire EEPROM is mapped onto this indirect MDIO addressable space (see also **Chapter 3.4.3.2**).

A write cycle is simply executed by setting address and write data in conjunction with the control bits. Once this is done, the XWAY™ PHY11G takes care of storing the byte into the E EPROM. A read cycle is similar, but after issuing a read access the higher-level management entity needs to wait until the data is read from the EEPROM. This is done by observing the `PHY.EECTRL.EXEC` bit. After this, the read byte can be loaded from `STD.MMDDATA`.

Note that it would make sense to check on the availabilityof an external EEPROM using the `PHY.EECTRL.EEDET` bit. This is set to active when an external EEPROM has been detected by the XWAY™ PHY11G.

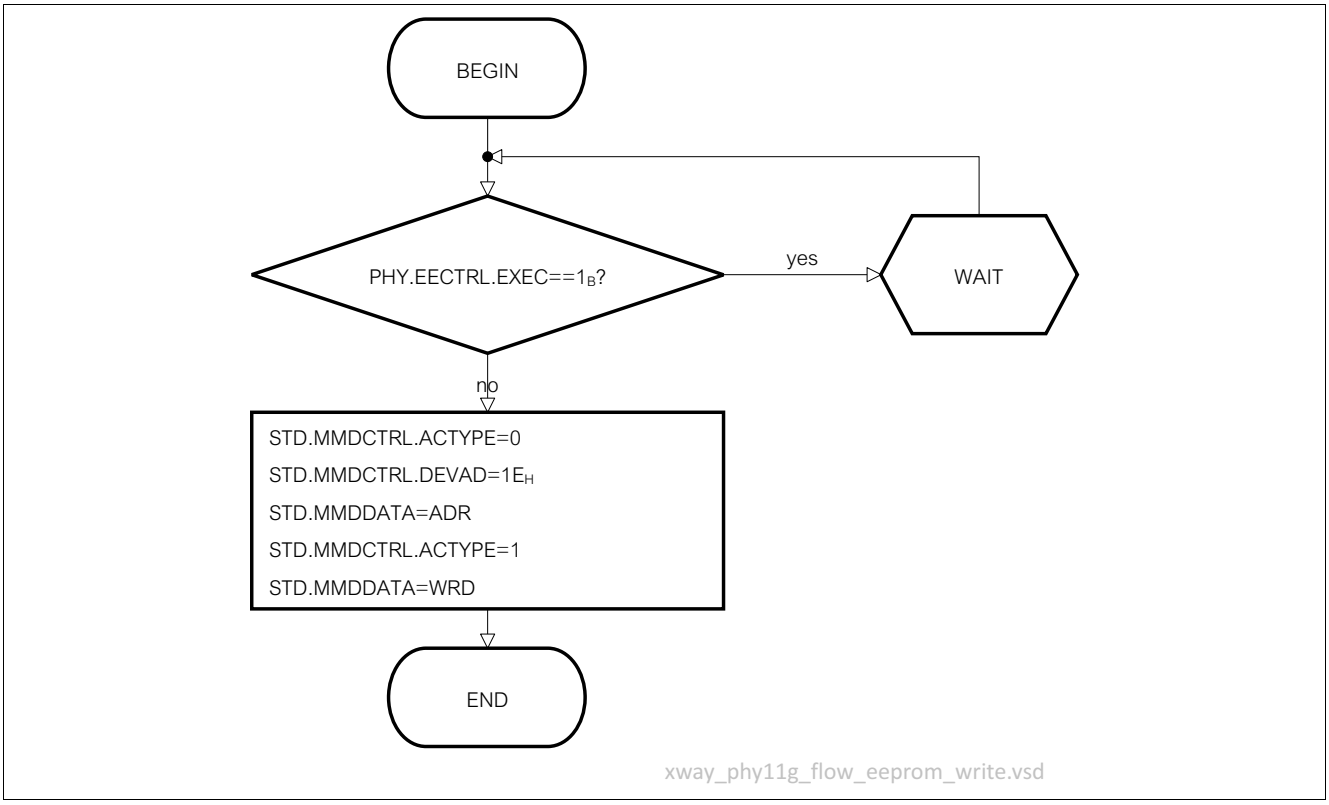


Figure 20 Flow-Chart for an Indirect EEPROM Write Cycle Via MDIO-MMD Access

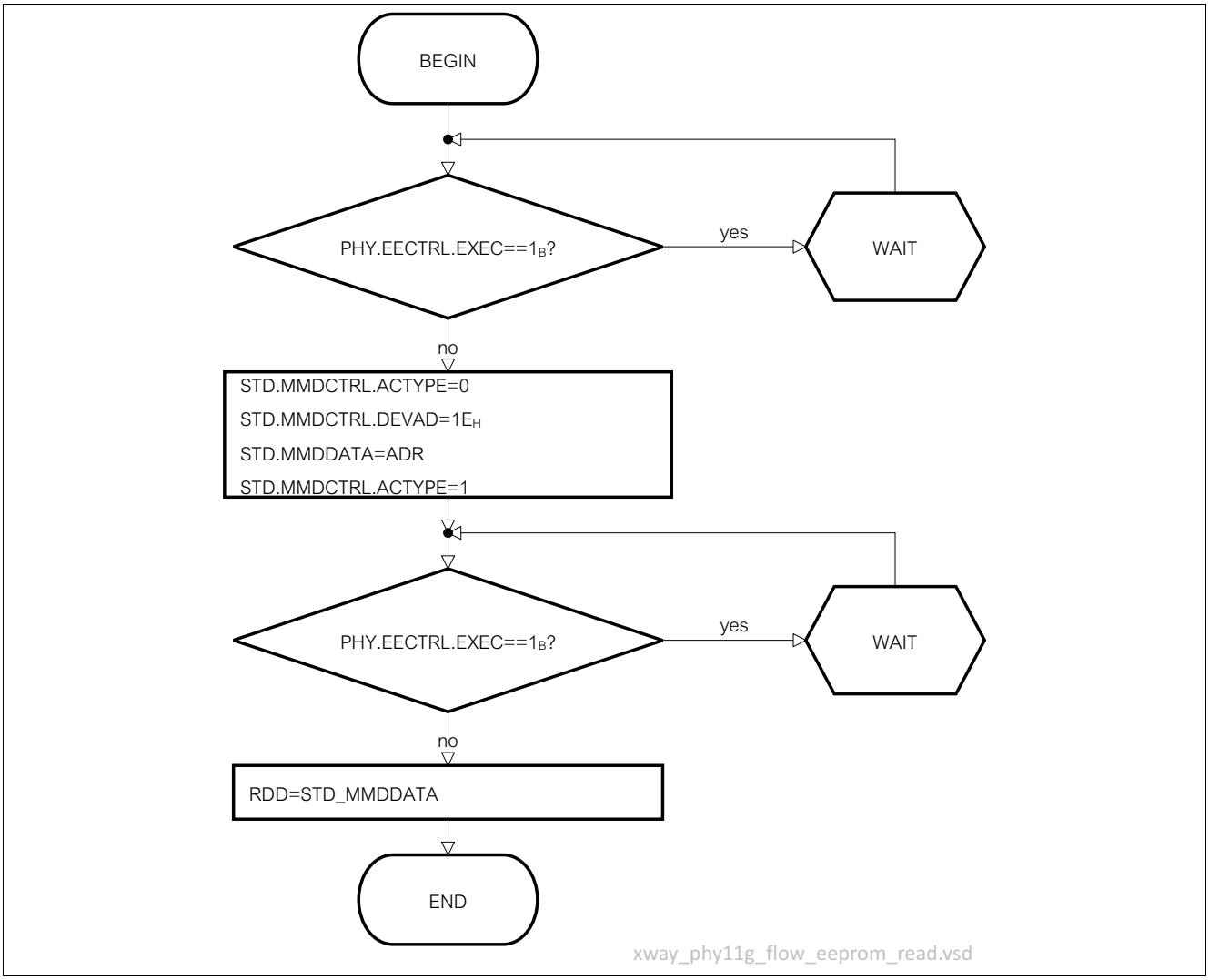


Figure 21 Flow-Chart for an Indirect EEPROM Read Cycle Via MDIO-MMD Access

3.4.3 Configuration and Control Via MDIO

If a higher-level management entity exists in the system, this can configure and control the XWAY™ PHY11G completely by means of the MDIO interface, according to IEEE 802.3 [1].

3.4.3.1 MDIO Interface

The XWAY™ PHY11G supports an MDIO interface according to IEEE 802.3 [1], giving a higher-level management entity control over internal functions. This control is provided by means of MDIO registers. The XWAY™ PHY11G provides the set of IEEE standard registers according to [1]. Additionally, extended register pages are supported. All registers are described in Chapter 4.

The MDIO interface is a serial interface using only 2 pins, which are named MDC and MDIO. See Chapter 2.2.5 for more information. The clock pin (MDC) is always driven by the higher-level management entity. The bi-directional signal (MDIO) carries the control information and is driven by both the higher-level management entity and the PHY, depending on whether a write or a read operation is being executed.

The MDIO communication between the higher-level management entity and PHY is organized in frames that are defined by IEEE 802.3 [1]. Figure 22 and Figure 23 illustrate the write and read frames respectively.

Chapter 6.6.5 defines the AC characteristics of this interface.

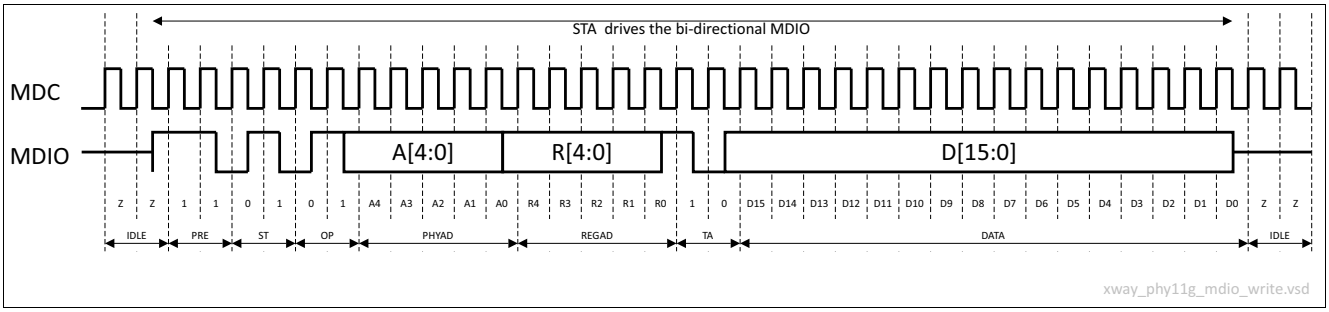


Figure 22 MDIO Write Frame

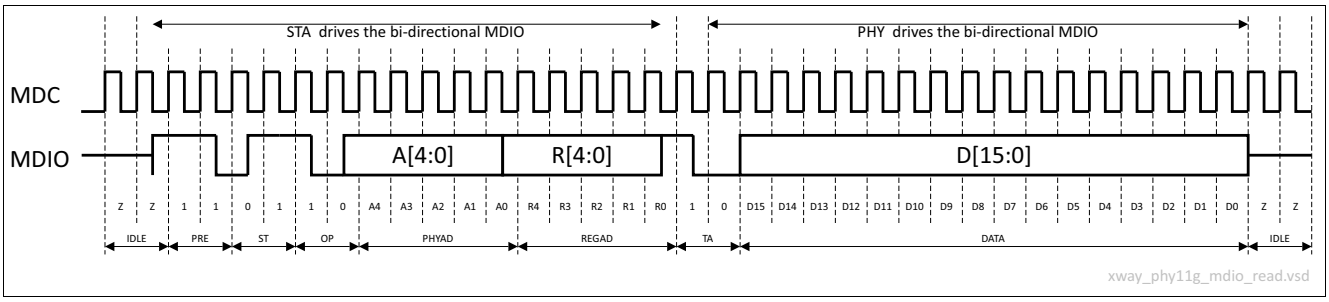


Figure 23 MDIO Read Frame

Note that the read operation requires the PHY to return the read data to the higher-level management entity. This implies that the driver of the MDIO signal is changed from being the higher-level management entity to being the PHY. In order to take this driving condition transition into account, a turn-around time is defined. The only period of time over which the PHY drives the MDIO signal is when returning the 16-bit read data value to the higher-level management entity.

Both frames consist of several fields which are explained in more detail in Table 24.

Table 24 Definition of MDIO Frame Components

Field	Field Long Name	Definition
IDLE	Idle Time	This state is entered by both the higher-level management entity and PHY when no transaction happens. In this state, all tristate drivers are inactive. The internal pull-up resistor of the MDIO pin on the XWAY™ PHY11G pulls the MDIO signal to logic one.
PRE	Preamble	The preamble is defined as a sequence of logic ones. Since this field of the frame is optional, the XWAY™ PHY11G does not require a preamble to be inserted. If inserted it can be of arbitrary length.
ST	Start of Frame	The ST field is required to determine a new frame start by means of a two-bit logic $<01_B>$ pattern.
OP	Operation Code	The operation code field indicates a read or write operation to the PHY by means of a two-bit logic $<10_B>$ or $<01_B>$ pattern respectively.
PHYAD	Physical Layer Address	The physical layer address field is used by the higher-level management entity to select one out of a maximum of 32 PHY devices. Each PHY needs to have a priori knowledge about its address. **Chapter 3.4.1** describes how this address can be configured to an XWAY™ PHY11G device.
REGAD	Register Address	This field represents a vector of five bits which define the register address for one out of 32 registers in the MDIO address space. In the XWAY™ PHY11G, this address space covers the standard IEEE 802.3 **[1]** registers plus extended and custom registers. **Chapter 4** describes all register configurations.
TA	Turnaround	The turnaround is a two-bit time field that separates the DATA field from the others to avoid contention during read operations. During read transactions, the time of the first bit is used to ensure that both the higher-level management entity and the PHY disable their tristate drivers and that MDIO is in high impedance. The times of the second bit is used by the XWAY™ PHY11G to drive a logic zero.
DATA	Read/Write Data	The data field is 16 bits wide. The MSB is sent first and the LSB is sent last in both read and write transactions.

3.4.3.2 MDIO Address Space

Configuration and control operations, as well as extraction of status information, can be handled via the MDIO interface. This interface allows for registers located in the MDIO address space to be read from and written to. The MDIO interface can only address up to 32 addresses. The first 16 addresses (from 00_H to $0F_H$) are mostly defined by the IEEE 802.3 standard **[1]**, and cannot be used for device-specific configuration. Only the last 16 addresses (from 10_H to $1F_H$) are to be used. Since a range of 16 addresses is not sufficient to manage the XWAY™ PHY11G, an indirect addressing scheme is used.

This scheme is depicted in **Figure 24**, which shows the layout of the MDIO address space looking from the higher-level management entity via the MDIO interface towards the PHY. As shown in the figure, the direct address region from 00_H to $0F_H$ holds all IEEE 802.3 standard **[1]** registers. The address range from 10_H to $1F_H$ spans an address range for PHY-specific registers that can be accessed directly via MDIO as well. The XWAY™ PHY11G address space is extended by means of an indirect memory access based on MMD registers. Note that this method is defined in the IEEE 802.3 standard **[1]**, in clause 22 and Annex 22D. It is used to access EEE registers as well as provide seamless access to a potentially externally-connected EEPROM and to all XWAY™ PHY11G internal registers. Note that access to internal registers is prohibited, except for the special addresses defined in **Chapter 5**.

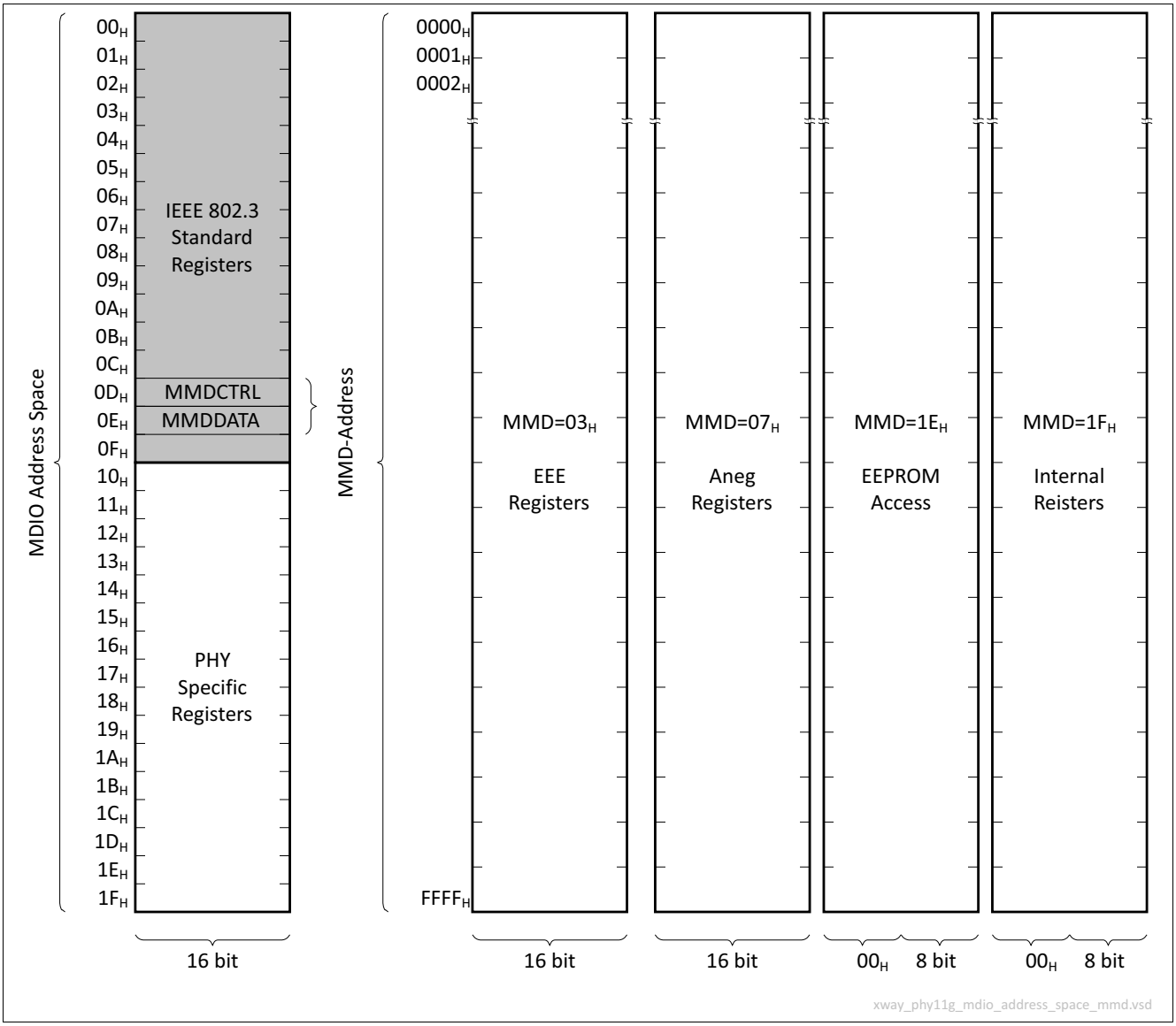


Figure 24 Layout of the MDIO Address Space

In order to simplify the software design, the most frequently used status and control registers are placed directly in the MDIO address range using the PHY-specific registers. Part of the functionality, for example EEE, is located in the MMD address range by standard definition. Some PHY-specific registers are located in the user-defined MMD addresses $1E_H$ and $1F_H$. An overview of all pages is listed in **Table 25**.

Table 25 MDIO Indirect MMD Device Address Overview

MMD	MMD Name	Description
00_H-02_H	Unused	
03_H	**EEE**	Contains some standard registers required for EEE operation
04_H-06_H	Unused	
07_H	**ANEG**	Contains some standard registers required for EEE auto-negotiation operation
04_H-06_H	Unused	
$1E_H$	**EEPROM**	Allows seamless indirect access to externally connected (if present) EEPROM
$1F_H$	**Internal**	Allows seamless indirect access to PHY internal registers

3.4.3.3 MDIO Interrupt

The XWAY™ PHY11G allows for an interrupt to be driven to the management device. This interrupt is named MDINT, and can be used by the management device to get notification of pre-configured events. These events can be configured in the MDIO register `MDIO.PHY.IMASK` (see also **Chapter 4**), which allows for a mask to be set onto the event vector that can cause the MDIO interrupt to be asserted. The actual interrupt status is reported in the MDIO register `MDIO.PHY.ISTAT`. Note that, without any active mask bit in `MDIO.PHY.IMASK`, the PHY will issue an interrupt after reset when it is ready to receive MDIO transfers.

Since there are many types of management devices, the interrupt polarity is not standardized. In order to be flexible and inter-operable with all types of management device IC, the MDINT pin of the XWAY™ PHY11G is in tristate when inactive. The active level of the MDINT pin can be customized by means of an external pull-up or pull-down resistor. If the MDINT polarity is active high, an external pull-down resistor must be connected to ground. Otherwise, if the MDINT polarity is active low, an external pull-up resistor must be connected to VDDP. After reset of the XWAY™ PHY11G, the MDINT is tristated by default. During this time period, the XWAY™ PHY11G detects the target polarity of the MDINT by reading out the pull-up/down resistor. The external circuitry for the MDINT pin in an active-high and active-low state is depicted in **Figure 25** and **Figure 26** respectively.

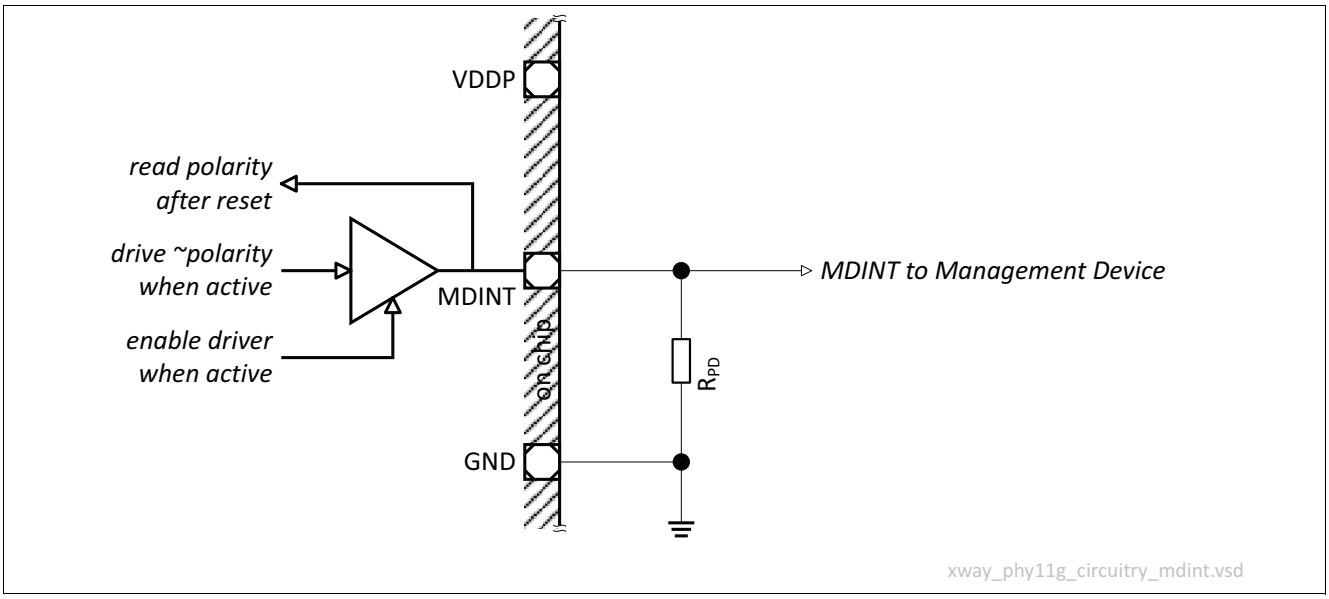


Figure 25 External Circuitry for an Active-High MDINT

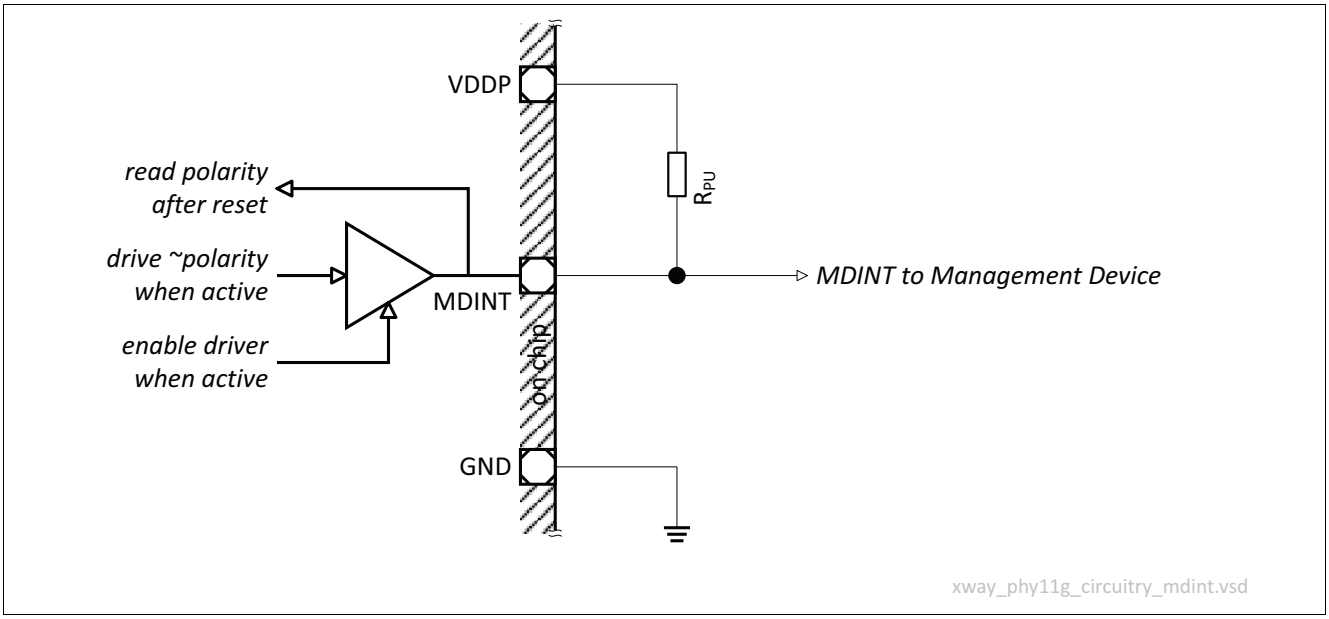


Figure 26 External Circuitry for an Active-Low MDINT

3.4.4 LED Interface

The XWAY™ PHY11G supports up to three LED outputs. These outputs are active high and drive LEDs directly with V_{DDP} = 2.5 V...3.3 V (see **Chapter 6.2**). It is possible to connect one single-color LED per interface pin, as well as bi-color LEDs. The latter is achieved by combining two LED interface pins. Both modes of operation are introduced in **Chapter 3.4.4.1** and **Chapter 3.4.4.2** respectively. The behavior and event-sensitivity of each LED can be configured individually, as described in **Chapter 3.4.4.3**. The individual MDIO registers referred to in **Chapter 3.4.4.3** are described in more detail in **Chapter 4**.

3.4.4.1 Single Color LED Mode

The external circuitry for a single-color LED is depicted in **Figure 27**. The LEDx pin represents one of the available LED interface pins at the device. The GND signal represents the common ground EPAD. The LED pins are designed to source a certain amount of current out of the pad-supply V_{DDP} when becoming active high. Besides the LED, two individual resistors are depicted in the figure. R_{LED} denotes an optional series resistor which could be used depending on the selected LED type and PAD supply voltage V_{DDP}. R_{CFGx} and C_{CFGx} denote external passive components required for the soft pin-strapping configuration of the device. The component values are selected such that the brightness of the LED is not affected. More details on this type of pin-strapping configuration can be found in **Chapter 3.4.1**.

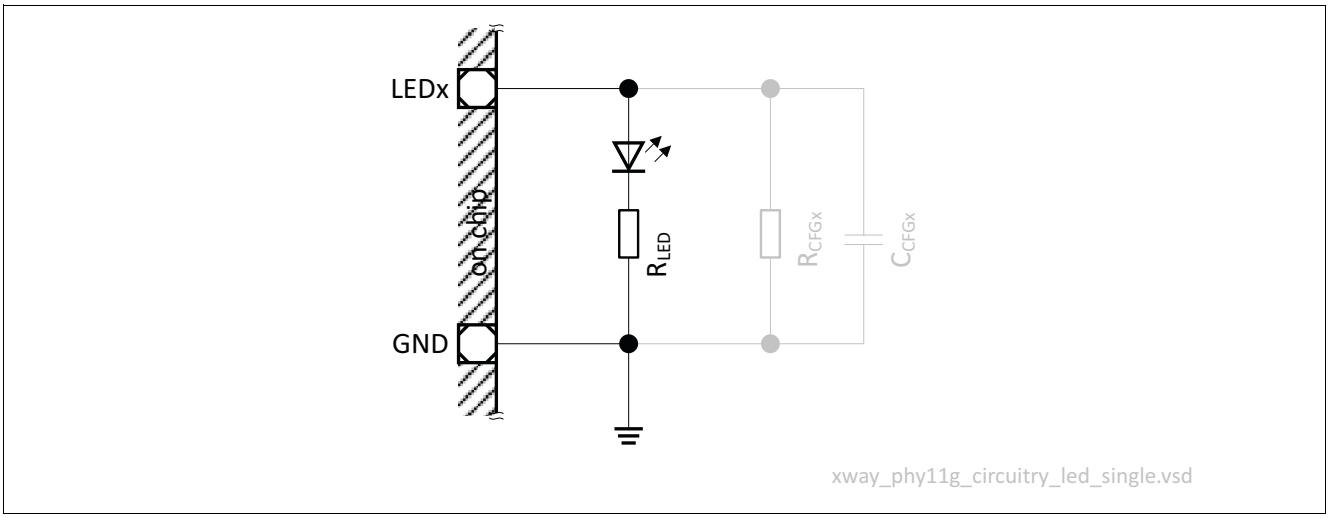


Figure 27 Single Color LED External Circuitry

3.4.4.2 Bi-Color LED Mode

The external circuitry for a bi-color LED is depicted in **Figure 28**. The LEDx and LEDy pins represent any two of the available LED interface pins at the device. The GND signal represents the common ground EPAD. The LEDx and LEDy pins are designed to source a certain amount of current out of the pad-supply V_{DDP} when becoming active high. Besides the LEDs[1)], three individual resistors are depicted in the figure. R_{LED} denotes an optional series resistor which might be used, depending on the selected LED type and PAD supply voltage V_{DDP}. R_{CFGx}/R_{CFGy} and C_{CFGx}/C_{CFGy} denote external passive components required for the soft pin-strapping configuration of the device. The component values are selected such that the brightness of the LED is not affected. More details on this type of pin-strapping configuration can be found in **Chapter 3.4.1**.

1) Bi-color LEDs are also available as monolithic 2-pin devices as indicated in **Figure 28**.

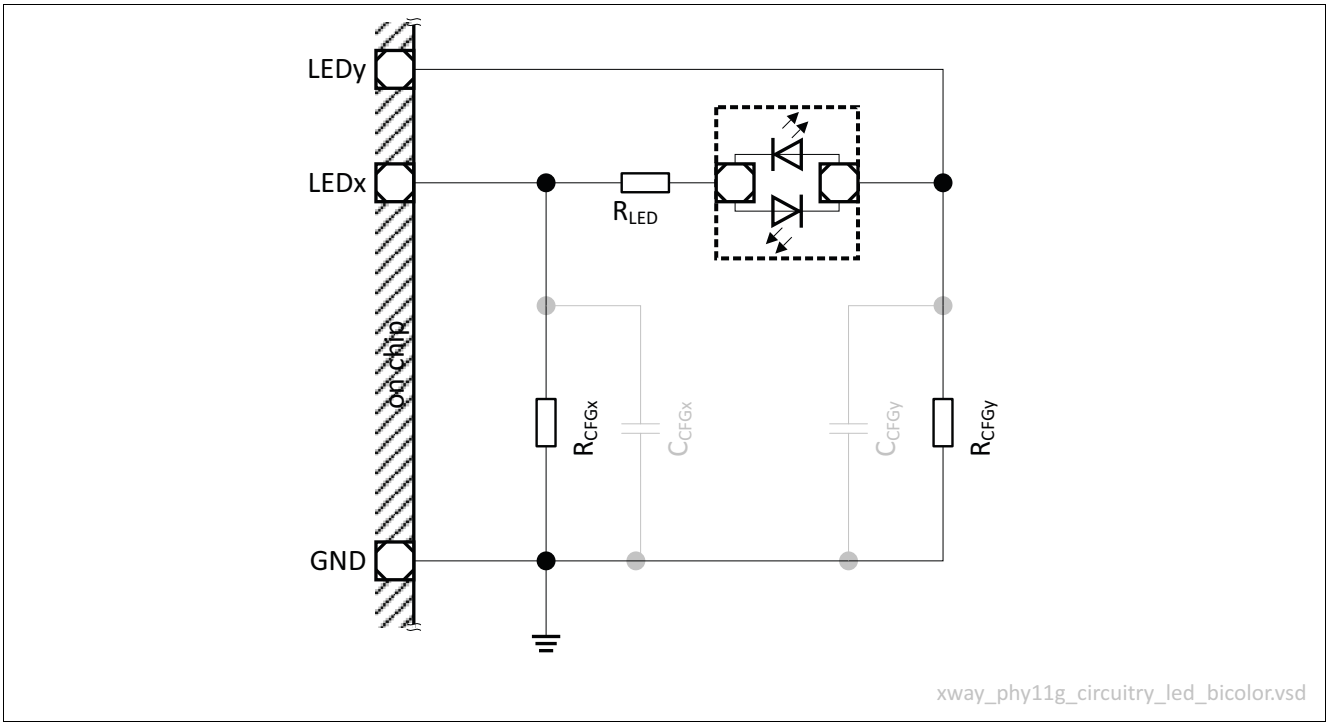


Figure 28 Bi-Color LED External Circuitry

3.4.4.3 LED Operations

Irrespective of the LED type used (single-color or bi-color), the LED pins can be operated in various modes. Basically, two major modes can be distinguished: Internally Controlled Mode (ICM) and Externally Controlled Mode (ECM). In ECM, the higher-level management entity is able to control the LEDs via register access in the MDIO register space. In ICM, the XWAY™ PHY11G itself controls the functions of the LEDs. These functions are introduced in **Chapter 3.4.4.3.2**, and can be configured by the higher-level management entity via MDIO configuration registers as described in **Chapter 3.4.4.3.3**. The configuration scheme is defined such that combined and direct-drive LED functionality can be set up.

3.4.4.3.1 LED Externally Controlled Mode (ECM)

In ECM, the LEDs can be directly driven by register bits mapped onto the MDIO address space. The higher-level management entity is able to directly change the LED outputs. This feature enables the higher-level management entity to control the LED pins itself, and the XWAY™ PHY11G only acts as the LED driver. This mode also acts as a simple testing feature for the LEDs. Note that ECM is not enabled by default, and needs to be enabled in advance. To enable the ECM, the higher-level management entity needs to set the register `MDIO.PHY.LED.LED[2:0]EN` = 0_B.

The LED can be illuminated by setting `MDIO.PHY.LED.LED[2:0]DA` = 1_B.

3.4.4.3.2 LED Functions in Internally Controlled Mode (ICM)

LED functions are activities to be applied to the LED pins according to a given configuration. These activities are applied in a given priority. It is possible to map multiple activities to the same LED pin, in order to be able to multiplex different types information. The configuration of these LED functions is described in **Chapter 3.4.4.3.3**. There are two types of LED function: direct and complex LED functions. Direct LED functions can be applied to a single LED, whereas complex LED functions use the context of all LEDs. **Table 26** lists all the supported direct LED functions and their associated priorities when compared with each other. **Table 27** lists all the supported

complex LED functions and their priorities when compared to each other. The complex LED functions have a higher priority than that of the direct LED functions.

Table 26 Direct LED Functions

Function	Priority	Description
PULSE	1 (high)	The LED is switched on/off shortly in reaction to a certain event or state transition. The corresponding ON and OFF time is determined by the pulse-stretching[1)] configuration. Note that each new event will cause an ON-OFF sequence unless if this event happens during a running PULSE function. The ON-OFF sequence is necessary to make the PULSE function visible on LEDs which already indicate another function, e.g. ON or BLINK slow. The length of the pulse stretching depends on the global setting used for the fast-blinking frequency.
BLINKF	2	LED blinks with a globally configured fast frequency.
BLINKS	3	LED blinks with a globally configured slow frequency.
CON	4	LED is constantly ON; can be configured to indicate link speed, EEE mode, ANEG, analog self-test / cable diagnostics, or the currently active interface (copper, fiber or other)
NONE	5 (low)	No direct function is applied to the LED; the LED is OFF (might be over-ruled by a concurrently running complex function).

1) Pulse-stretching is used to make short events visible by extending the lighting time of the LED following this event.

Table 27 Complex LED Functions

Function	Priority	Description
CBLINK	1 (high)	All LEDs blink simultaneously with the globally configured fast frequency. In particular, in order to distinguish this mode properly from concurrently running direct functions, all even-numbered LEDs have their blinking phase shifted by 180° with respect to the odd-numbered LEDs.
SCAN	2	Scan sequence; this is a walking light running fast between LED0 to LED2 backwards and forwards. The speed is selected for the fast-blink frequency.
NACS	3	Reversed scan sequence; similar to the SCAN function but all LED outputs are inverted.
NONE	4 (low)	No complex function is applied to the LEDs.

The speed or frequency of any of the BLINK or SCAN/ISCAN LED functions can be selected by means of a global setting in the `MMD.INTERNAL.LEDCH.FBF` register (fast-blinking frequency) as well as in the `MMD.INTERNAL.LEDCH.SBF` register (slow-blinking frequency). Refer to **LED Configuration** for more information.

3.4.4.3.3 LED Configuration in ICM

The configuration of LEDs for ICM can be managed with the LED configuration registers. Apart from the complex function registers `MMD.INTERNAL.LEDCH` and `MMD.INTERNAL.LEDCL`, there is one such register for each LED port: registers `MMD.INTERNAL.LED0H` / `MMD.INTERNAL.LED0L` through `MMD.INTERNAL.LED2H` / `MMD.INTERNAL.LED2L`. The layout of this type of configuration register is defined in **Chapter 4**. Each supported direct function owns a field in the respective LED-specific configuration registers. The setup of the direct functions is independent for each LED. The fields of the `MMD.INTERNAL.LEDxx` register allow several states/events of the XWAY™ PHY11G to be mapped to the supported direct functions. If a direct function is not desired, a NONE must

be mapped. Note that multiple events/states can occur simultaneously. The direct functions apply according to the priority as specified in **Table 26**. Also note that a direct function always has a lower priority than any supported complex function.

As an example the following mapping can be configured for LED0, LED1 and LED2:

- LED0:
  - PULSE = NONE
  - BLINKS = LINK10
  - BLINKF = LINK100
  - CON = LINK1000
- LED1
  - PULSE = ACTIVITY (TXACT | RXACT)
  - BLINKS = NONE
  - BLINKF = NONE
  - CON = NONE
- LED2
  - PULSE = COL
  - BLINKS = NONE
  - BLINKF = NONE
  - CON = NONE

In this example, the LED0 indicates the speed of the PHY, whereas LED1 indicates the transmit and receive activity. LED2 reflects any collision in case of half-duplex mode settings.

If any supported complex function (CBLINK, SCAN, NACS) is desired in cable diagnostics mode, this can be set up using the registers `MMD.INTERNAL.LEDCL.{CBLINK, SCAN}` and `MMD.INTERNAL.LEDCH.{NACS}`.

3.5 Power Management

This chapter introduces the power management and power supply functions of the XWAY™ PHY11G.

3.5.1 Power Supply

Because of its integrated DC/DC switching regulator, the XWAY™ PHY11G can be powered using a single power supply, as described in **Chapter 3.5.1.1**. However, the device can also be powered without the integrated DC/DC switching regulator, as described in **Chapter 3.5.1.2**.

If the integrated DC/DC switching regulator is used, then a clock signal is required at XTAL1 during both normal mode and boundary scan mode.

3.5.1.1 Power Supply Using Integrated Switching Regulator

By using the integrated DC/DC switching regulator, the XWAY™ PHY11G can be powered using a single power supply. This power supply can range from 2.5 V to 3.3 V. As long as the applied nominal voltage remains in this range, the device operates automatically and without the need for additional settings to be applied. Only minor external circuitry is required to enable this feature. An example schematic is shown in **Figure 29**. The electrical characteristics of the power supply are defined in **Chapter 6.2**.

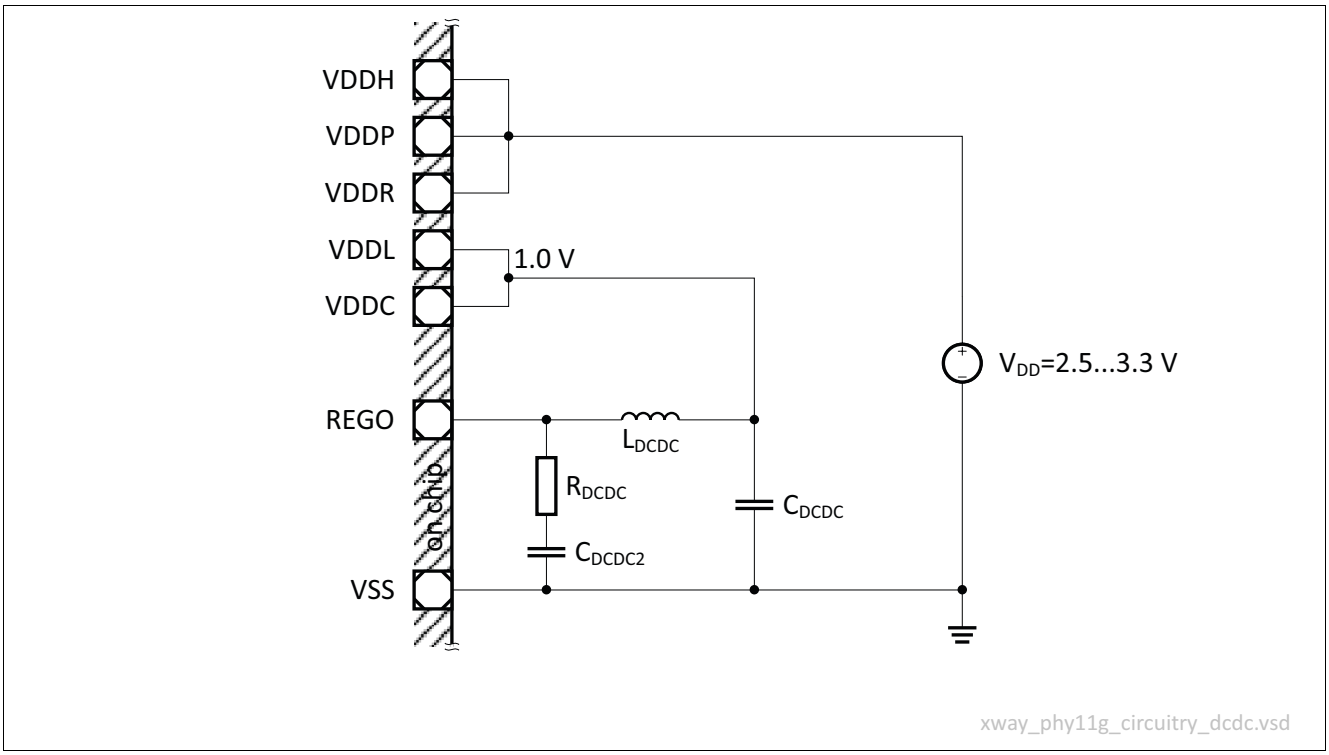


Figure 29 External Circuitry using the Integrated Switching Regulator

The required values for external components are listed in **Table 28**.

Table 28 Switching Regulator External Component Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC/DC buck inductance	L_{DCDC}		4.7		µH	I_{max} = 450 mA
DC/DC smoothing capacitance	C_{DCDC}		22.0		µF	

Table 28 Switching Regulator External Component Values (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC/DC spike filter resistance	R_{DCDC}		5.0		Ω	
DC/DC spike filter capacitance	C_{DCDC2}		333.0		pF	

3.5.1.2 Power Supply Without Using Integrated Switching Regulator

When the integrated DC/DC switching regulator is not used, for example when both power supply voltages are already available in the system, the XWAY™ PHY11G can be powered by a dual power supply, as shown in **Figure 30**. The electrical characteristics of the power supply are defined in **Chapter 6.2**.

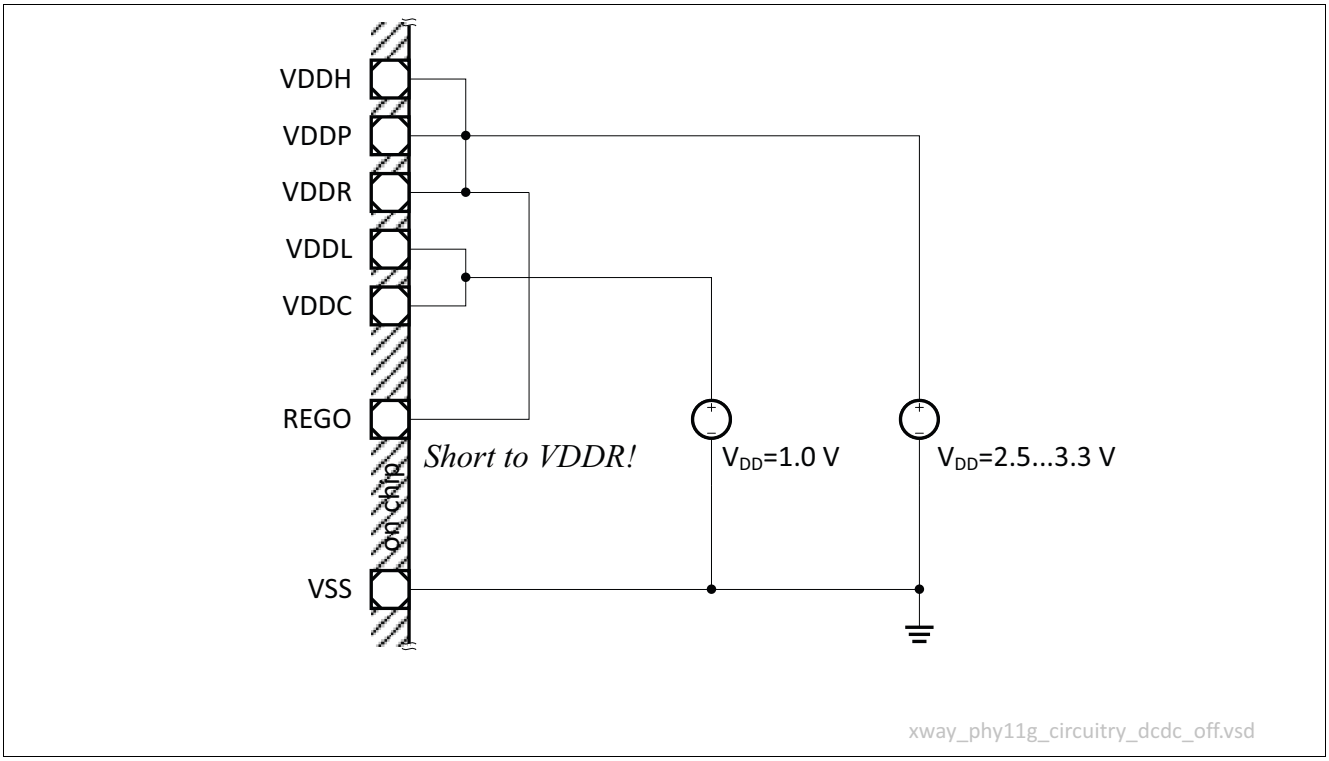


Figure 30 External Circuitry without using the Integrated Switching Regulator

In external supply mode, the integrated DC/DC is internally switched off, as the XWAY™ PHY11G automatically detects whenever the switching regulator output pin is shorted to VDDR. In this case, neither additional pin-strappings nor register settings are required. Note that **Figure 30** is only a generic schematic, and does not show power supply blocking for reasons of simplicity.

3.5.2 Power Over Ethernet (PoE)

Power Over Ethernet (PoE) is a standardized method (described in IEEE 802.3af, and in particular in IEEE 802.3, clause 33 **[1]**) for remotely powering devices via the MDI. The remotely powered device does not require a power supply, thereby mainly saving on installation costs, since only the Ethernet connection (CAT5 cable or better) needs to be equipped. One example of such an application is for WLAN routers or NAS devices. According to the standard, such devices can be remotely powered if they consume less than 15.4 W. As there is a strong demand for higher-power applications, an enhancement of the PoE standard has been developed (IEEE 802.3at, **[3]**) that is able to provide up to 50 W via remote powering. The increase in power level is practically the only difference between the two standard versions.

The IEEE 802.3at standard defines two kinds of devices, the Powered Device (PD) and the Power-Sourcing Equipment (PSE). The former extracts electrical power from the common mode of some of the twisted pairs inside the CAT5 (or better) cable, whereas the latter acts as a source of electrical power. The two types of devices and their application together with the XWAY™ PHY11G are illustrated in **Chapter 3.5.2.1** and **Chapter 3.5.2.2**, respectively.

3.5.2.1 Powered Device (PD)

Figure 31 shows a generic schematic diagram of a system using a PD.

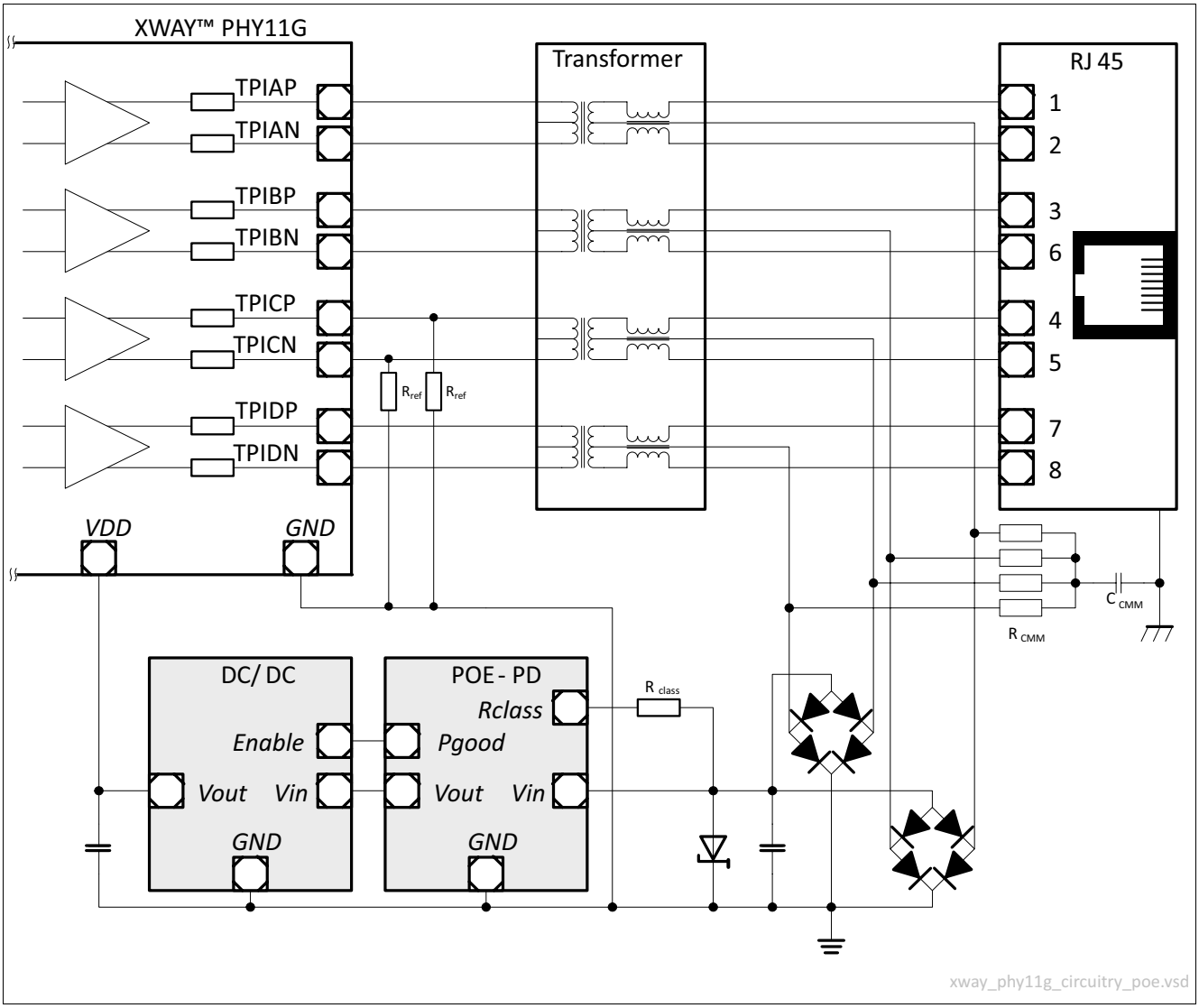


Figure 31 Generic Schematic of the PoE/PD Application

As shown in the diagram, additional external circuitry is required to extract power from the twisted pair. This includes a PD circuit and a DC/DC converter, together with various external components that are usually not integrated. The PD and DC/DC devices could be integrated on one IC.

According to IEEE 802.3, clause 33 (**[1]**), there are two alternative methods for supplying a PD. The first involves supplying power via the common mode of the pairs (1, 2) and (3, 6), whereas the second involves the pairs (4, 5) and (6, 7). The PD is required to accept power from both alternatives, but only one in parallel. The polarity of the power injection is not specified. Accordingly, each PD must have a diode-bridge rectifier to extract the power from both twisted-pair combinations alternatively but independent of the driver polarity.

In turn, the PD must signal to the PSE which type of power is required, as several power classes are defined. More details can be found in IEEE 802.3, clause 33 (**[1]**). This signaling is done by means of a resistive value which is sensed by the PSE. Each PD IC provides a pin to which this classification resistor can be connected. After the initial classification, done by the PSE with low voltages to prevent damage of non PoE-compliant PDs, the PSE drives the required power to the line. The PD indicates the availability of power to the DC/DC converter by means of the Pgood (power good) signal. The DC/DC converter is required to transform the line voltage (>20 V) to the

chip power supply voltages required by the system. Since the DC/DC can only start once the power is stable, the Pgood indication is usually a necessary requirement. Note that the DC/DC converter must implement soft-start functionality to prevent the start current from becoming exhaustively large. Once the DC/DC provides the nominal voltage to the system, the remotely powered devices (ICs) power up just as they would if a power source is applied in normal operating conditions.

In the simplified generic schematic of **Figure 31**, the board voltage provided by the DC/DC of the PD is fed to the XWAY™ PHY11G to supply the 2.5 V...3.3 V voltage domain, and in particular VDDP, VDDH and VDDR. All these domains must be properly blocked with adequate capacitance and filtering techniques. The integrated DC/DC switching regulator (see also **Chapter 3.5.1.1**) of the XWAY™ PHY11G can in turn be used to supply the 1.0 V voltage domains, for example VDDL and VDDL. Note that the integrated DC/DC switching regulator supports soft-starting such that PoE is enabled.

The power class advertised by the PD to the PSE depends largely on the power consumption of the whole system. The XWAY™ PHY11G itself must also be taken into account. Regardless of the current power consumption of the XWAY™ PHY11G, it is recommended that a figure of 1 W is assigned to the PHY.

3.5.2.2 Power Sourcing Equipment (PSE)

The generic PSE circuit diagram is similar to that of the PD, except that the PSE must only inject the supply into one of the two twisted-pair alternatives: pairs (1, 2) and (3, 6) or (4, 5) and (6, 7). The PSE also does not require polarity invariance measures, since it defines the supply polarity. However, the PSE must be supplied properly to guarantee proper operation, regardless of which type of PD is connected. Otherwise, the PSE has to switch itself off if it detects a PD of too high a power class.

There are 2 types of PSE system: in-band and mid-span. A mid-span device does not include a PHY. The pairs that are not used for PoE are routed straight through, whereas the pairs that are used are routed through another transformer into which the PSE device can inject power. The disadvantage of a mid-span device is that additional magnetics are required. Besides, the mid-span application is beyond the scope of this specification, as a mid-span device does not require any interaction whatsoever with a PHY.

Although not a likely application, the XWAY™ PHY11G can be used in PSE systems of the in-band PoE type. A generic example of such an application is shown in **Figure 32**.

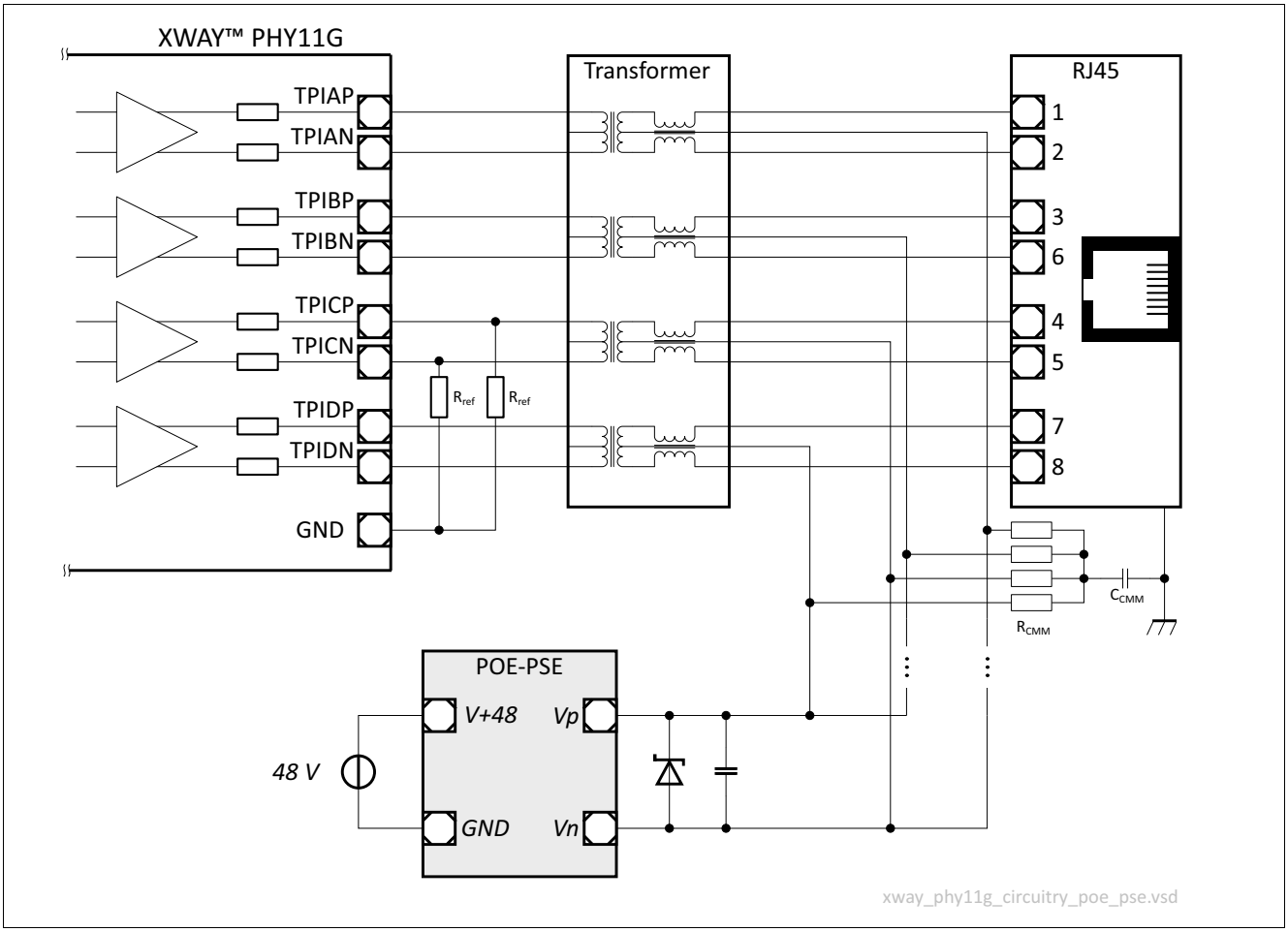


Figure 32 Generic Schematic of the PoE/PSE Application

Note that the PSE adds complexity to the design, because of the high-voltage supply of the PoE. Typically, 48 V are used to supply the remote PD. It is recommended to avoid cross-connecting any of the PSE signals with any of the XWAY™ PHY11G signals, unless these are galvanically de-coupled. This applies to the common-mode supply injection at the center taps of the transformers, which is only done on the line side of the transformer. Some PSE devices support an I^2C interface for management interaction. This interface can only be connected to the XWAY™ PHY11G when using an opto-coupler.

3.5.3 Energy-Efficient Ethernet

The IEEE 802.3az standard ([2]), describing Energy-Efficient Ethernet (EEE) operation, is also implemented in the XWAY™ PHY11G. Since the method used for saving energy depends on the PHY speed, this section is divided into 3 subsections corresponding to the various speeds of 10BASE-Te, 100BASE-TX and 1000BASE-T. Except for 10BASE-Te, the general idea of EEE is to save power during periods of low link utilization. Instead of sending an active idle, the transmitters are switched off for a short period of time (20 ms). The link is kept active by means of a frequent refresh cycle initiated by the PHY itself during low power mode. This sequence is repeated until a wake request is generated by one of the link-partners MACs. An EEE-compliant MAC must grant the PHY a time budget of wake time before the first packet is transmitted. The basic principle is shown in **Figure 33**.

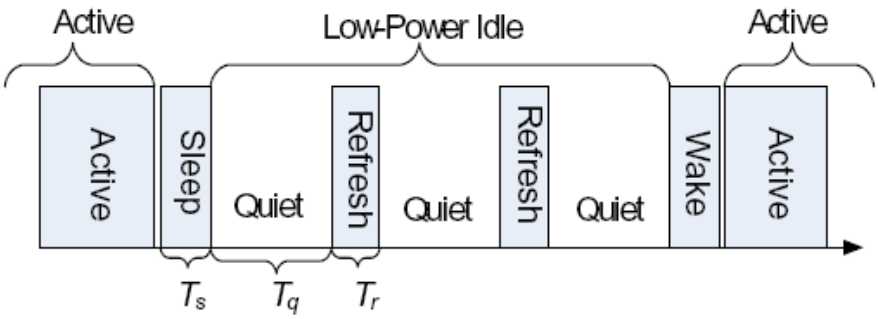


Figure 33 EEE Low-Power Idle Sequence

3.5.3.1 EEE for 10BASE-Te

10BASE-Te is a fully inter-operable version of the legacy 10BASE-T. It is optimized for CAT5 and better cabling infrastructure. Since these cables have better insertion loss properties, the amplitude of 10BASE-T can be reduced, thus saving on energy. Specifically, the 10BASE-Te transmission amplitude has been reduced to the range of 1.54 V...1.92 V, instead of 2.2 V...2.8 V for 10BASE-T. The 10BASE-Te mode can be activated using the `MDIO.PHY.PHYCTL1.TXEEE10` bit. In order to maintain maximal inter-operability, the XWAY™ PHY11G detects links with marginal characteristics and automatically switches back to the 10BASE-T mode. Thus the legacy performance requirements are also supported, even though the transmitter is set up for 10BASE-Te.

3.5.3.2 EEE for 100BASE-TX

During periods of low link utilization, an EEE-compliant MAC can assert Low Power Idle (LPI). It does so by asserting TX_EN = 0_B, TX_ER = 1_B and TXD = 0001_B at the MII or an equivalent interface. The XWAY™ PHY11G initiates LPI signaling and enters a low-power mode. Similarly, the XWAY™ PHY11G senses LPI signaling on its receive side and switches off the receive path. Any wake attempt will cause the XWAY™ PHY11G to return to the normal mode of operation in transmit or receive. Note that the XWAY™ PHY11G indicates a receive LPI by asserting RX_DV = 0_B, RX_ER = 1_B and RXD = 0001_B at the MII or equivalent interface. The wake-time for 100BASE-TX is of 30 µs.

3.5.3.3 EEE for 1000BASE-T

During periods of low link utilization, an EEE-compliant MAC can assert Low Power Idle (LPI). It does so by asserting TX_EN = 0_B, TX_ER = 1_B and TXD = 01_H at the Gigabit MII or an equivalent interface. In 1000BASE-T LPI mode, the transmit function of the XWAY™ PHY11G enters a quiet mode only after the XWAY™ PHY11G transmits “sleep” and receives “sleep” from the link partner. If the link partner chooses not to signal LPI, then the PHY can also not become quiet. However, LPI requests are passed from one end of the link to the other regardlessly, and system energy savings can be achieved even if the PHY link does not become quiet. The 1000BASE-T LPI is symmetric on the PHY layer but remains asymmetric (transmit and receive independently) at xMII level and above. Note that the XWAY™ PHY11G indicates a receive LPI by asserting RX_DV = 0_B, RX_ER = 1_B and RXD = 01_H at the GMII or an equivalent interface. The wake-time for 1000BASE-T is of 16.5 µs.

3.5.3.4 Auto-Negotiation for EEE Modes

It is imperative that EEE capability is advertised, since, except for 10BASE-Te, a compliant link partner is required. Similarly to 1000BASE-T auto-negotiation, the XWAY™ PHY11G automatically advertises EEE capability if this is enabled using next pages. EEE capability is stored in the MMD.ANEG.EEE_AN_ADV registers (refer to **EEE Auto-Negotiation Advertisement Register**). Setting this register to zero disables EEE. After a successful negotiation the link partners' capabilities are stored in the MMD.ANEG.EEE_AN_LPADV register (refer to **EEE Auto-Negotiation Link-Partner Advertisement Register**). After a successful auto-negotiation, the XWAY™ PHY11G performs an auto-resolution on the exchanged capabilities. The result is combined with the speed resolution. Whether or not a link is able to operate EEE is reported in the MDIO.PHY.MIISTAT.EEE register (refer to **Media-Independent Interface Status**).

3.5.3.5 Support of Legacy MACs

An EEE-aware MAC should be able to assert LPI as described in Table 22-1 of the IEEE 802.3az standard (**[2]**). In contrast, a legacy MAC is incapable of this and simply indicates a 'normal inter frame' when it does not have frames to send, as described in Table 22-1 of the IEEE 802.3 standard (**[1]**). However, the XWAY™ PHY11G allows for low-power operation to be achieved even when a legacy MAC is used. This is done by observing the continuous presence of normal inter-frame signal combinations at its xMII input, and by switching to LPI mode.

Therefore, the LPI mode operates in the same way as required by the IEEE 802.3az standard (**[2]**), except for the way in which the mode is triggered. The LPI mode operation in the XWAY™ PHY11G is shown in **Figure 34**. The LPI-unaware MAC can resume transmission of frames without any early warning, and it is necessary for the XWAY™ PHY11G to wake up and send these incoming frames without losing any of the data contained. To temporarily hold the bytes arriving immediately after LPI, an internal buffer is employed. This buffer is emptied gradually over the MDI after LPI mode is left. This is achieved by shortening the IPG, without which the buffer might not be properly emptied within a reasonable amount of time. To achieve this, not all incoming IPG bytes are transmitted over the MDI, and some are discarded.

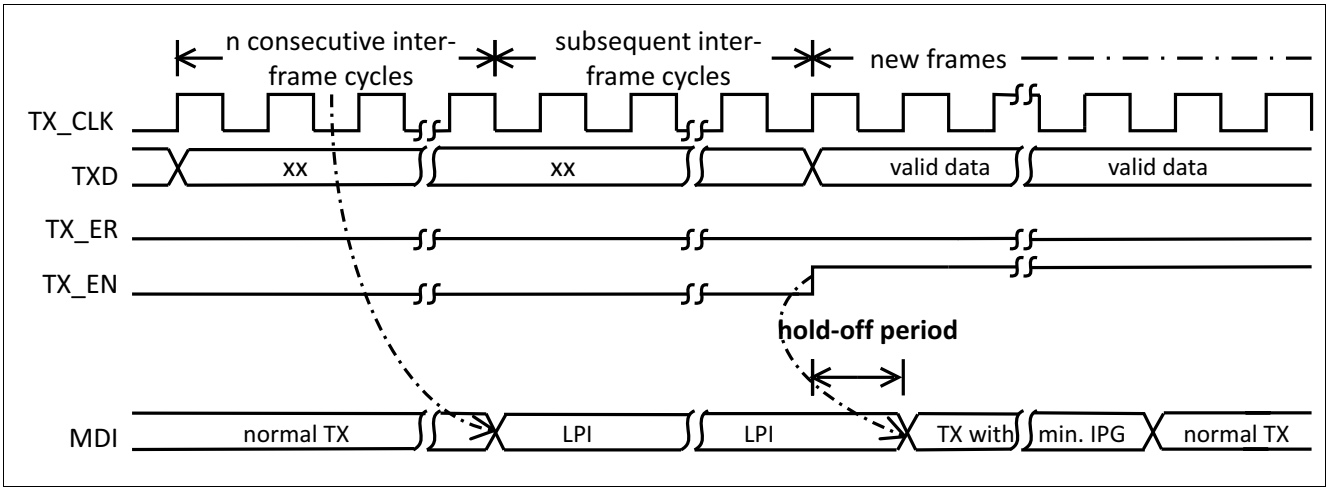


Figure 34 LPI Mode Operation in XWAY™ PHY11G

To activate this feature, the LPI bit in the MDIO.PHY.PHYCTL2 register needs to be set to 1 (refer to **Physical Layer Control 2**). In addition, the IDLE value in the MMD.INTERNAL.LEG_LPI_CFG3 register should be programmed to indicate the number of inter-frame bytes that should arrive at the MII input before the LPI is activated (refer to **Legacy LPI Configuration Register 3**). The Tw_phy value in the IEEE 802.3az standard (Table 78-4) defines a minimum time between when a new frame is received from the MAC (terminating the LPI mode) until when MDU transmission can start. This value is reflected in the HOLDOFF_100BT and HOLDOFF_1000BT values in the MMD.INTERNAL.LEG_LPI_CFG0 and MMD.INTERNAL.LEG_LPI_CFG1 registers for the 100 Mbit/s and 1000 Mbit/s modes respectively (refer to **Legacy LPI Configuration Register 0**

and **Legacy LPI Configuration Register 1**). The default value of this register ensures compliance with the IEEE 802.3az value.

In the LPI mode, the MDI alternates between quiet and refresh signals. LPI is terminated when any new valid frame from the xMII interface arrives or a wake-up signal is received from the link partner.

The maximum number of IPG bytes that may be transmitted via MDI, in the phase where the buffer is being emptied of the bytes that triggered LPI termination, is determined by the IPG value in the `MMD.INTERNAL.LEG_LPI_CFG2` register (refer to **Legacy LPI Configuration Register 2**). If the incoming data includes more IPG bytes, these will not be stored in thisbuffer, and are subsequently not transmitted over the MDI.

3.5.4 Wake-on-LAN (WoL)

Wake-on-LAN (WoL) is an essential feature of the XWAY™ PHY11G. By means of an integrated packet trace engine that is capable of monitoring and detecting WoL packets, the PHY is able to wake a larger SoC from its power-down state. This is done by indicating such an event via the external interrupt sourced by the XWAY™ PHY11G. This scenario is shown in **Figure 35**. Consequently, the SoC can switch off everything except the interrupt controller, in order to save the maximum amount of power. The XWAY™ PHY11G can trace WoL packets in any of its supported speed modes:10/100/1000 Mbit/s. Since WoL is a standby system feature, it can happen that the residual power consumption of the XWAY™ PHY11G is critical. Therefore, it is recommended to put the PHY into a lower power state, for example 10BASE-T or 100BASE-T, before the SoC enters its power-down state. If the link supports EEE (see also **Chapter 3.5.3**), this is not required since the PHY can be put into low-power mode by means of an LPI assert signal. Once a WoL packet is detected, the XWAY™ PHY11G issues a wake-up indication to the SoC by activating the MDINT signal (see also **Chapter 3.4.3.3**).

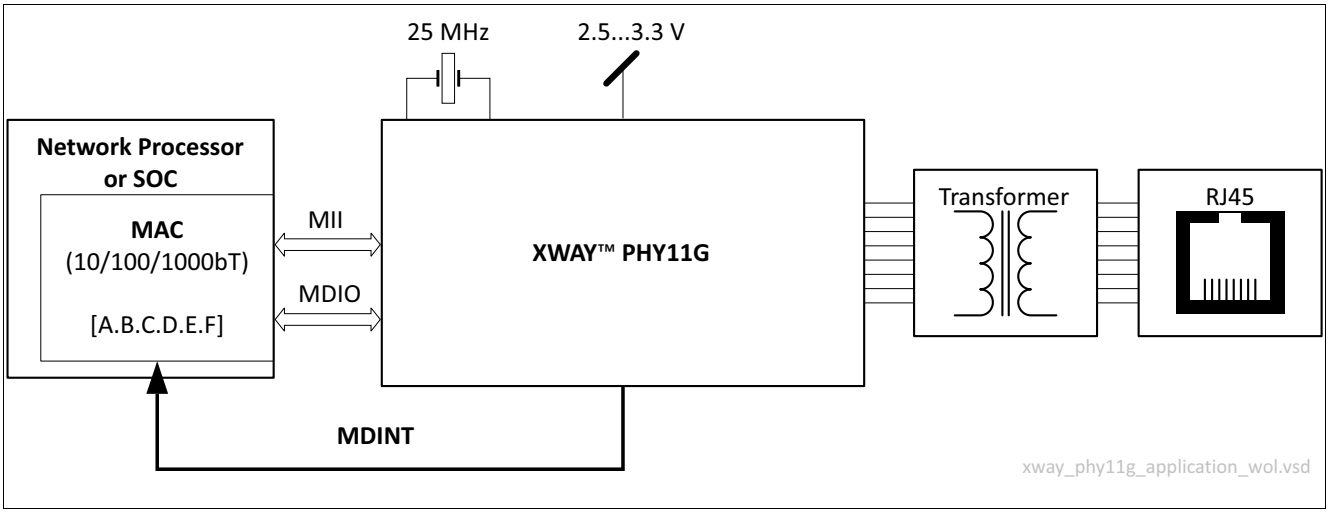


Figure 35 Block Diagram of a WoL Application

The most commonly used WoL packet is a magic packet **[14]**. A magic packet is a deterministic packet that contains the MAC address of the device that is to bewoken up. A magic packet can be encapsulated into any type of higher-layer protocol, for example TPC/IP or UDP. Regardless of the higher-layer protocol used, the setup of the core magic packet is always the same.

The format of a magic packet is shown in **Figure 36** for an example with a MAC address of $AA_H.BB_H.CC_H.DD_H.EE_H.FF_H$ and an optional password of $00_H.11_H.22_H.33_H.44_H.55_H$. The example magic packet is shown encapsulated in the content of a conventional Ethernet MAC frame structure. The magic packet itself contains of a header which is a sequence of 6 consecutive FF_H Bytes. Following this header is a repetition for 16 times of the target MAC address of the device to be woken up. Note that this address can also be any standard broadcast address. An optional field containing a 6 Byte wake-up password follows. The XWAY™ PHY11G scans for this password if it is configured. Otherwise, this field is ignored.

The XWAY™ PHY11G is a pure PHY and does not include a MAC or have a MAC address. The SoC must configure its own MAC address, for example $AA_H.BB_H.CC_H.DD_H.EE_H.FF_H$, into the WoL packet monitoring engine of the XWAY™ PHY11G, using the MDIO interface. The same applies in case the optional password is intended to be used.

The configuration of the MAC address and the optional SecureOn password relevant for the WoL logic inside the XWAY™ PHY11G is performed via MDIO registers. For the given example, programming is done according to the steps illustrated in **Table 29**. Note that, by definition, a SecureOn password of $00_H.00_H.00_H.00_H.00_H.00_H$ means that no SecureOn password is defined and therefore none is checked.

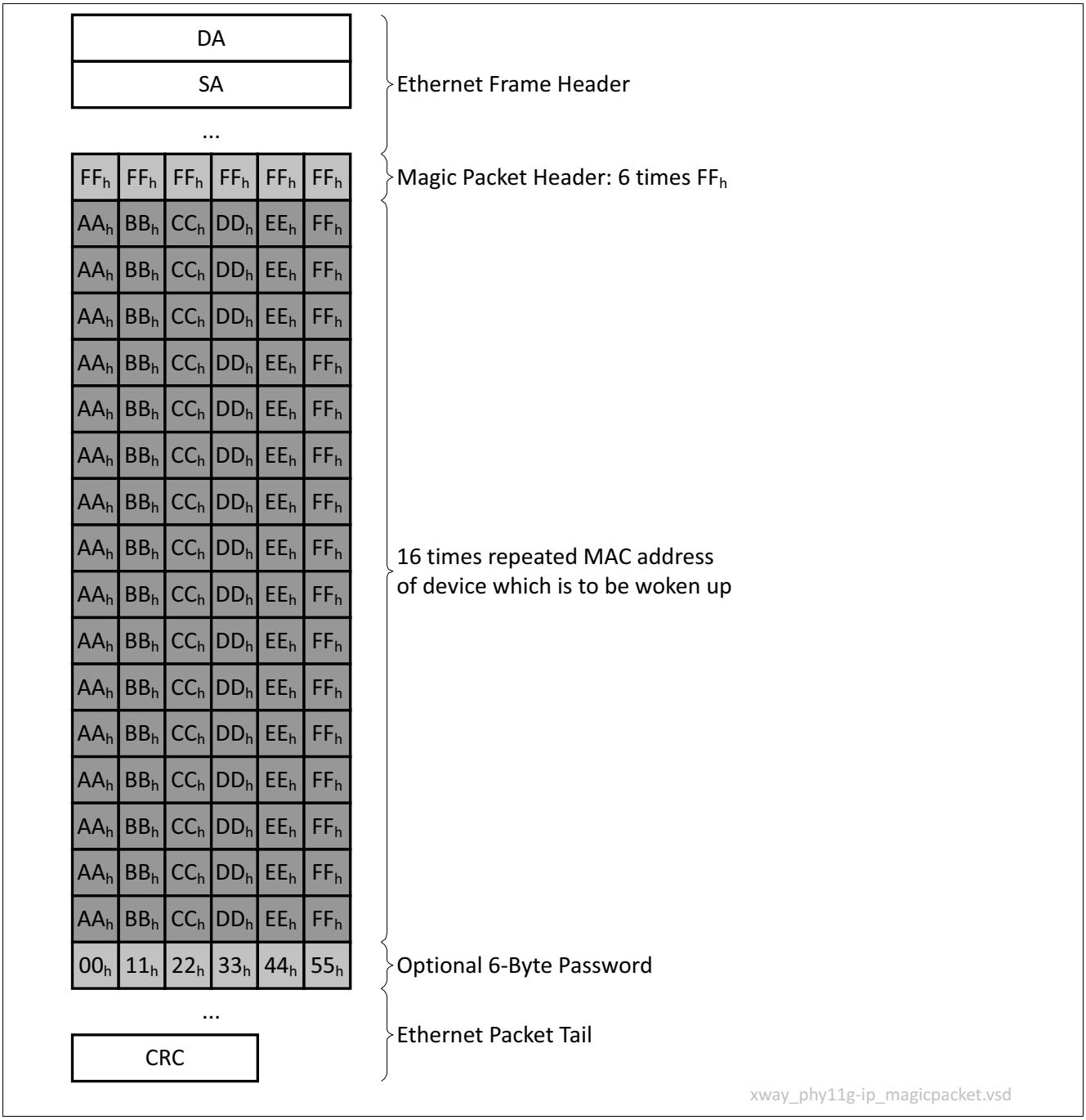


Figure 36 The Magic Packet Format

Table 29 Programming Sequence for the Wake-On-LAN Functionality

Step	Register Access	Remark
1	MDIO.MMD.WOLAD0 = AA_H	Program the first MAC address byte
2	MDIO.MMD.WOLAD1 = BB_H	Program the second MAC address byte
3	MDIO.MMD.WOLAD2 = CC_H	Program the third MAC address byte
4	MDIO.MMD.WOLAD3 = DD_H	Program the fourth MAC address byte
5	MDIO.MMD.WOLAD4 = EE_H	Program the fifth MAC address byte
6	MDIO.MMD.WOLAD5 = FF_H	Program the sixth MAC address byte
7	MDIO.MMD.WOLPW0 = 00_H	Program the first SecureON password byte
8	MDIO.MMD.WOLPW1 = 11_H	Program the second SecureON password byte
9	MDIO.MMD.WOLPW2 = 22_H	Program the third SecureON password byte
10	MDIO.MMD.WOLPW3 = 33_H	Program the fourth SecureON password byte
11	MDIO.MMD.WOLPW4 = 44_H	Program the fifth SecureON password byte
12	MDIO.MMD.WOLPW5 = 55_H	Program the sixth SecureON password byte
13	MDIO.PHY.IMASK.WOL = 1_B	Enable the Wake-On-LAN interrupt mask
14	MDIO.MMD.WOLCTRL.WOL.EN = 1_B	Enable Wake-On-LAN functionality

3.5.5 Power Down Modes

This section introduces the power-down modes that are supported by the XWAY™ PHY11G. These modes can be associated to states as shown in **Figure 37**. The functionality of each mode and the state transitions are discussed in detail in the subsequent sections.

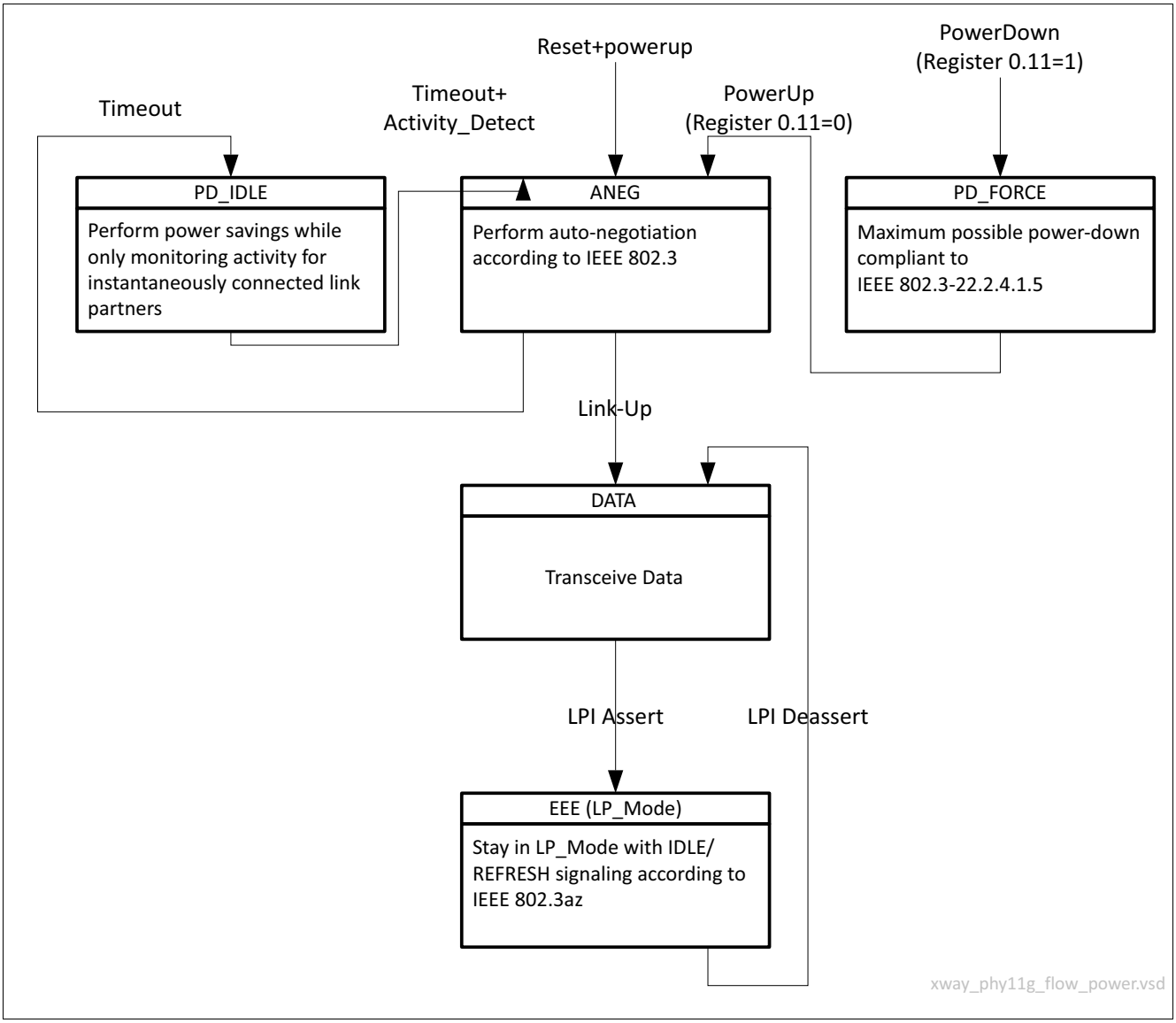


Figure 37 State Diagram for Power-Down Mode Management

3.5.5.1 PD_FORCE Mode

The PD_FORCE mode is entered by setting the register `MDIO.STD.CTRL.PD` to logic 1, regardless of the current state of the device. Active links are dropped when the PHY is leaving the DATA mode. The sleep mode corresponds to power down as specified in IEEE 802.3 **[1]**, clause 22.2.4.1.5. The device still reacts to MDIO management transactions. The interface clocks to the MAC are switched off. No signal is transmitted on the MDI.

Since this mode is entered manually, the device will wake neither itself nor any link partner. Leaving the PD_FORCE mode is only possible by setting the register `MDIO.STD.CTRL.PD` = 0_B.

3.5.5.2 ANEG Mode

In the Auto-Negotiation (ANEG) mode, the PHY tries to establish a connection to a potential link partner. The PHY remains in this state for a reasonably long time until a successful link partner has been detected, either through parallel detection or by an auto-negotiation process itself. After a successful link partner detection, the PHY enters the DATA mode by performing a link-up. However, since in most Ethernet systems the default mode is still an open port (no link-partner is connected), the idle power consumption during ANEG mode contributes significantly to the power budget. The XWAY™ PHY11G supports an optimized power-down mode during auto-negotiation. Whenever no link partner is detected for a certain amount of time, the PHY moves into the PD_IDLE mode (**Chapter 3.5.5.3**). It only comes back from the PD_IDLE mode into the ANEG mode after a time-out, or whenever a signal is detected coming from the link partner. Returning to ANEG mode after a time-out is required to wake up link partners that use similar power-saving schemes, for example another XWAY™ PHY11G.

3.5.5.3 PD_IDLE Mode

This is a sub-state supporting power-saving methodologies during auto-negotiation (see also **Chapter 3.5.5.2**).

3.5.5.4 DATA Mode

The DATA mode is used to establish and maintain a link connection. Once this connection is dropped, the PHY moves back into ANEG mode. During DATA mode, the PHY is linked up and data can be transmitted and received. If the EEE mode (**Chapter 3.5.5.5**) of operation has been negotiated during the ANEG mode, the PHY moves into and out of the EEE mode whenever instructed to by the MAC's LPI agent.

3.5.5.5 EEE Mode

This is the Energy-Efficient Ethernet (EEE) low-power mode which is entered after an LPI assert command from the MAC's LPI agent. More details can be found in **Chapter 3.5.3**.

3.6 Testing Functions

This section describes the test and verification features supported for the XWAY™ PHY11G.

3.6.1 JTAG Interface

The XWAY™ PHY11G integrates a JTAG port according to IEEE 1149.1 [8], which defines a test access port and a boundary scan architecture. The JTAG interface of the XWAY™ PHY11G consists of a 4-pin Test Access Port (TAP) as specified in Chapter 2.2.6. It includes the mandatory signals TMS, TCK, TDI and TDO.

When using JTAG mode with the internal DC/DC switching regulator, a clock signal needs to be applied at XTAL.

The integrated TAP controller of the XWAY™ PHY11G supports the op-codes as shown in Table 30.

Table 30 JTAG TAP Controller Op-Codes

Instruction	Instruction Code	JTAG Register	Register Width	Comment
EXTEST	$0000\ 0000_B$	Boundary scan		Allows for testing of external circuitry connected between XWAY™ PHY11G and other components on the same PCB. The XWAY™ PHY11G drives a previously loaded (using the PRELOAD instruction) pattern to all its outputs and samples all its inputs.
SAMPLE/PRELOAD	$0000\ 0001_B$	Boundary scan		Allows a snapshot to be taken of all pins within the boundary scan during normal mode of operation, as well as for the values to be read out. This instruction also allows for patterns to be loaded into the boundary scan test cells in advance of other JTAG test instructions.
IDCODE	$0001\ 0001_B$	Device ID	32	Returns the JTAG boundary scan ID according to Table 31 on TDO
CLAMP	$0000\ 0010_B$	Bypass	1	Allows the state of the signals driven from all XWAY™ PHY11G pins within the boundary scan to be determined from the boundary scan register. Simultaneously, the bypass register is selected as the serial path between TDI and TDO. The signals determined from the boundary scan register remain unchanged while the CLAMP instruction is selected.
HIGHZ	$0000\ 0011_B$	Bypass	1	Forces all outputs of the XWAY™ PHY11G into a high-impedance state. This prevents damage of components when testing according to IEEE1149.1 with components not following this standard.
BYPASS	$1111\ 1111_B$	Bypass	1	Bypasses the integrated TAP controller by connecting TDI to TDO via a single register, i.e. with one TCK period delay
RESERVED	Remaining			

As specified in Table 30, the IDCODE instruction returns the device ID on the TDO pin. The encoding of this device ID is given in Table 31.

Table 31 JTAG Boundary Scan ID

Description	Device Version [31:28]	Device Code [27:12]	Manufacture Code [11:1]	Mandatory LSB
Value 00	01_B	$0000\ 0001\ 1100\ 1100_B$	$0000\ 1000\ 001_B$	1_B

3.6.2 Payload Data Tests

This chapter specifies several payload-data test features that are integrated in the XWAY™ PHY11G.

3.6.2.1 Test Packet Generator (TPG)

The integrated Test Packet Generator (TPG) allows for test packets to be sent even when no MAC is connected to the MII, or when the connected MAC is inactive. This is done by multiplexing the TPG output into the transmit data path of the MAC interface. The TPG is controlled by `MDIO.PHY.TPGCTRL` and `MDIO.PHY.TPGDATA` (refer to **Test-Packet Generator Control** and **Test-Packet Generator Data**). It can be effectively used in the following applications:

- Electrical-characteristics test for 10BASE-T and 100BASE-TX
- BER measurements

The test packet is limited to layer-2 functionality with restricted configuration possibilities determined by `MDIO.PHY.TPGCTRL`. The basic test packet structure is shown in **Figure 38**.

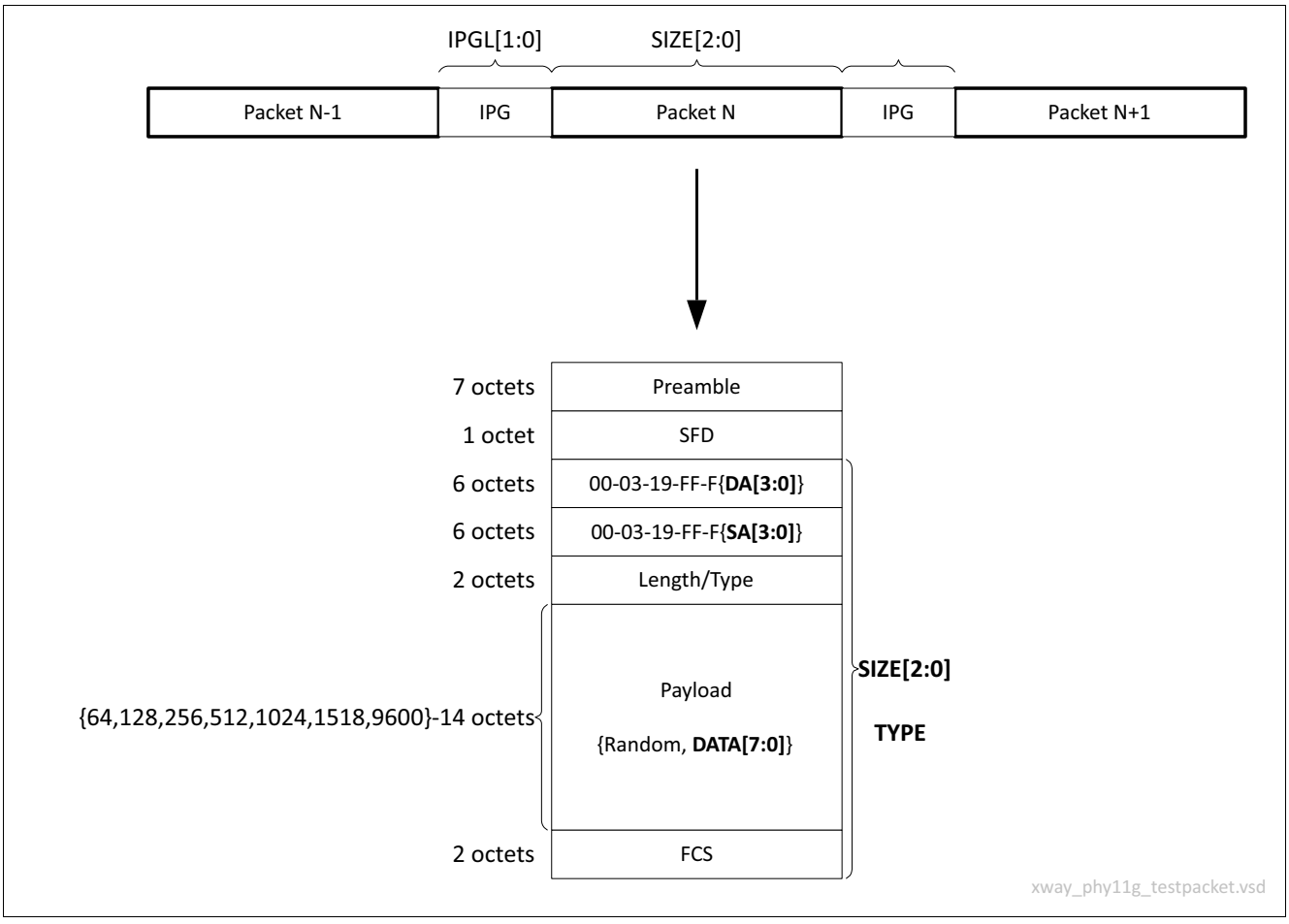


Figure 38 Test Packet Format

3.6.2.2 Error Counters

The XWAY™ PHY11G incorporates a general-purpose error counter, accessible via the `MDIO.PHY.ERRCNT.*` MDIO management registers. `MDIO.PHY.ERRCNT.SEL` allows an error source to be selected. The number of errors are counted and written to `MDIO.PHY.ERRCNT.COUNT`. This counter is cleared upon read access, and saturates at the value `MDIO.PHY.ERRCNT.COUNT` = FF_H. This prevents ambiguous monitoring results created by an overflow. The error counter is only applicable to the twisted-pair PHY modes.

3.6.3 Test Loops

The XWAY™ PHY11G supports several test loops to support system integration. The individual loop-back functions are covered in the following sections, as well as how to enable and disable them.

3.6.3.1 Near-End Test Loops

The near-end test loops are used to verify system integration of an XWAY™ PHY11G device. They allow for closed loop-backs of data and signals at different OSI reference layers. The following sections describe these loop-backs in descending order of OSI abstraction layer.

3.6.3.1.1 MAC Interface Test Loop

The MAC interface test loop allows raw xMII transmit data to be looped back to the xMII receive port. In the high-level block diagram in **Figure 39**, the test loop data-path is marked by the area shaded in gray. This test loop can be applied to all the supported MAC interfaces described in **Chapter 3.2**. If required, the conversion of data and control information is handled internally.

There are two methods for setting up this test loop. The first uses the IEEE loop-back setting: `MDIO.STD.CTRL.LB` = 1_B. In this mode, the MII speed must be configured manually using the `MDIO.STD.CTRL.SS*` speed selection bits. Also, the PHY is not operable towards the MDI.

The second method uses the `MDIO.PHY.PHYCTL1.TLOOP = NETL` XWAY™ PHY11G proprietary test-loop setting. The test loop is activated at the next link-up.

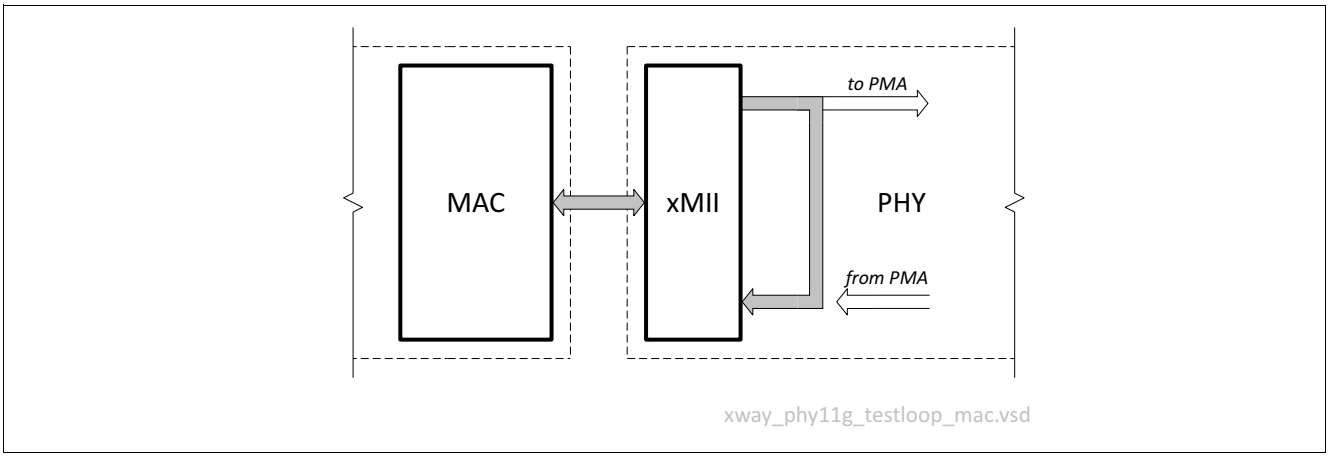


Figure 39 MAC Interface Near-End Test Loop

3.6.3.1.2 MDI Test Loop

The MDI test loop allows for loop-back of the signal at the MDI connector, for example RJ45 or SMB. Referring to the four available twisted pairs in a CAT5 or equivalent cable type, pair A is connected to pair B, and pair C to D. This shorting of near-end twisted pairs must be enabled using specialized termination circuitry. Note that no additional resistors are required, since the ports of the XWAY™ PHY11G are already inherently terminated. **Figure 40** shows a high-level block diagram, where the test loop data-path is marked by the area shaded in gray. This test loop can be applied to all the supported MAC interfaces described in **Chapter 3.2**. The test-loop mode is activated by setting `MDIO.PHY.PHYCTL1.TLOOP = RJ45`. The test loop is activated at the next link-up.

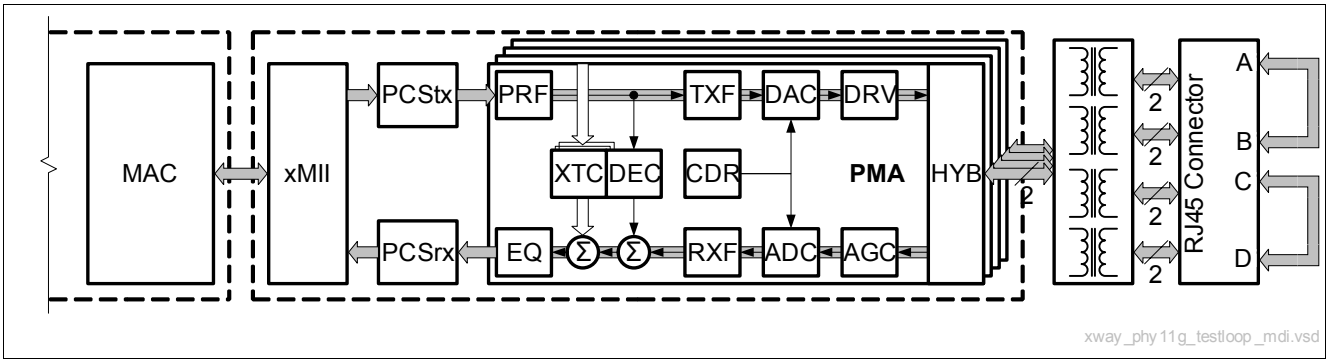


Figure 40 MDI connector Near-End Test Loop

3.6.3.1.3 Echo Test Loop

The DEC (Digital Echo Canceler) test loop allows for the transmit signal to be looped back via the Digital Echo Canceler (DEC). This loop-back is similar to the functionality of the MDI test loop as described in **Chapter 3.6.3.1.2**, except that it does not require a special termination circuitry at the MDI connector. The user of this test loop has the option to terminate each twisted pair with a 100 Ω resistor. When executing this test, the PMA trains the DEC to the echo that is inherently present because of non-ideal line terminations. Since there is no far-end signal, and the echo is canceled out at the summation point, the synthesized echo replica signal at the output of the DEC is used as a receive signal. This setup allows for the complete transceiver to be tested in 1000BASE-T mode, without the need for additional hardware to be attached. **Figure 41** shows a high-level block diagram, where the test loop data-path is marked by the area shaded in gray. This test loop can be applied to all the supported MAC interfaces described in **Chapter 3.2**, but is only applicable to 1000BASE-T. The test loop is activated by setting `MDIO.PHY.PHYCTL1.TLOOP = ECHO`, and by activating the 1000BASE-T forced mode using `MDIO.STD.CTRL.SSM` = 1_B and `MDIO.STD.CTRL.SSL` = 0_B.

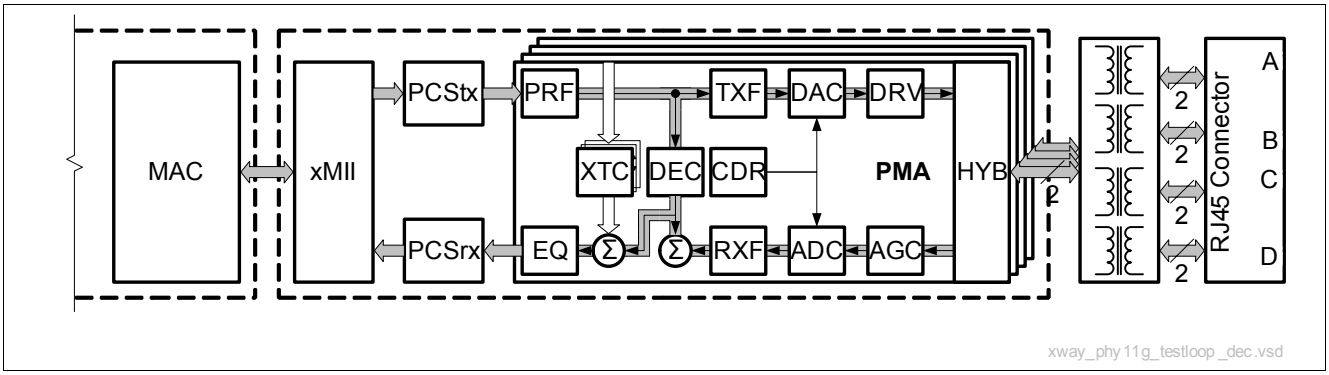


Figure 41 Echo Near-End Test Loop

3.6.3.2 Far-End Test Loop

The PCS far-end test loop allows for the receive data at the output of the receive PCS to be fed back into the transmit path, that is, the input of the transmit PCS. The received data is also available at the xMII interface output, however all xMII transmit data is ignored in this test mode. **Figure 42** shows a high-level block diagram, where the test loop data-path is marked by the area shaded in gray. This test loop can be applied to all the supported MAC interfaces described in **Chapter 3.2**. The test is also applicable to all supported types of MDI physical-layer standards as described in **Chapter 3.3**. This test loop is activated by setting the bit `MDIO.PHY.PHYCTL1.TLOOP = FETL`. Note that the test-loop is only operable when the link is operational. It is activated at the next link-up.

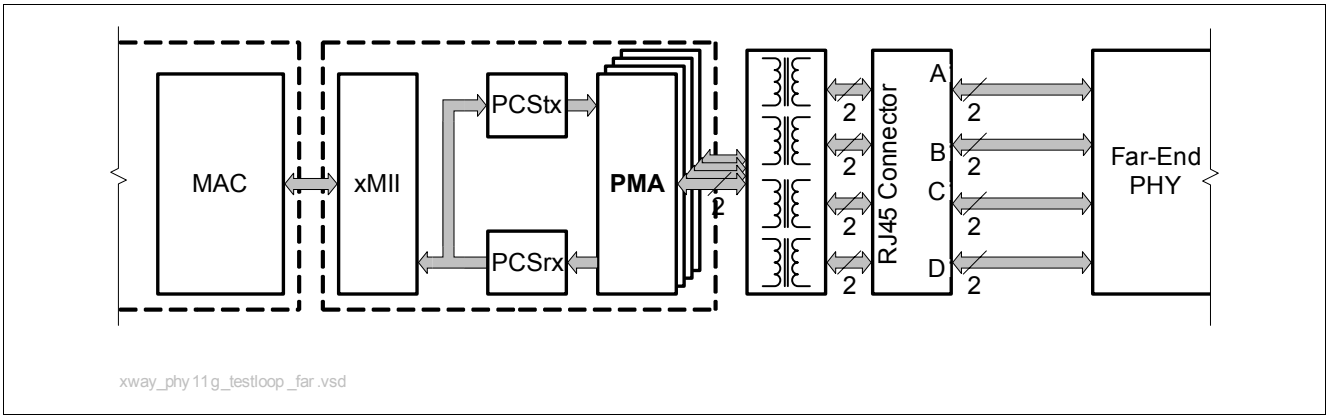


Figure 42 PCS Far-End Test Loop

4 MDIO Registers

This chapter defines all the MDIO registers needed to operate the XWAY™ PHY11G.

Table 32 Registers Address Space

Module	Base Address	End Address	Note
MDIO Registers	00_H	$1F_H$	Addresses are word-aligned

Table 33 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
STD			
CTRL	Control	00_H	**86**
STAT	Status Register	01_H	**89**
PHYID1	PHY Identifier 1	02_H	**92**
PHYID2	PHY Identifier 2	03_H	**92**
AN_ADV	Auto-Negotiation Advertisement	04_H	**93**
AN_LPA	Auto-Negotiation Link-Partner Ability	05_H	**95**
AN_EXP	Auto-Negotiation Expansion	06_H	**97**
AN_NPTX	Auto-Negotiation Next-Page Transmit Register	07_H	**98**
AN_NPRX	Auto-Negotiation Link-Partner Received Next-Page Register	08_H	**99**
GCTRL	Gigabit Control Register	09_H	**100**
GSTAT	Gigabit Status Register	$0A_H$	**102**
RES11	Reserved	$0B_H$	**104**
RES12	Reserved	$0C_H$	**104**
MMDCTRL	MMD Access Control Register	$0D_H$	**105**
MMDDATA	MMD Access Data Register	$0E_H$	**106**
XSTAT	Extended Status Register	$0F_H$	**107**
PHY			
PHYPERF	Physical Layer Performance Status	10_H	**108**
PHYSTAT1	Physical Layer Status 1	11_H	**109**
PHYSTAT2	Physical Layer Status 2	12_H	**111**
PHYCTL1	Physical Layer Control 1	13_H	**112**
PHYCTL2	Physical Layer Control 2	14_H	**114**
ERRCNT	Error Counter	15_H	**116**
EECTRL	EEPROM Control Register	16_H	**117**
MIICTRL	Media-Independent Interface Control	17_H	**119**
MIISTAT	Media-Independent Interface Status	18_H	**121**
IMASK	Interrupt Mask Register	19_H	**122**
ISTAT	Interrupt Status Register	$1A_H$	**124**
LED	LED Control Register	$1B_H$	**126**

Table 33 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TPGCTRL	Test-Packet Generator Control	$1C_H$	128
TPGDATA	Test-Packet Generator Data	$1D_H$	130
FWV	Firmware Version Register	$1E_H$	131
RES1F	Reserved	$1F_H$	131

The registers are addressed wordwise.

4.1 STD: Standard Management Registers

This section describes the IEEE 802.3 standard management registers.

Control

This register controls the main functions of the PHY. See also IEEE 802.3-2008 22.2.4.1 ([1]).

CTRL	Offset	Reset Value
Control	00_H	9040_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	LB	SSL	ANEN	PD	ISOL	ANRS	DPLX	COL	SSM	RES					
RWSC	RW	RW	RW	RW	RW	RWSC	RW	RW	RW	RO					

Field	Bits	Type	Description
RST	15	RWSC	**Reset** Resets the PHY to its default state. Active links are terminated. Note that this is a self-clearing bit which is set to zero by the hardware after reset has been done. See also IEEE 802.3-2008 22.2.4.1.1 ([1]). **Constants** 0_B **NORMAL** Normal operational mode 1_B **RESET** Resets the device
LB	14	RW	**Loop-Back** This mode enables looping back of MII data from the transmit to the receive direction. No data is transmitted to the medium via MDI. The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test. See also IEEE 802.8-2008 22.2.4.1.2 ([1]). **Constants** 0_B **NORMAL** Normal operational mode 1_B **ENABLE** Closes the loop-back from TX to RX at xMII
SSL	13	RW	**Forced Speed-Selection LSB** Note that this bit only takes effect when the auto-negotiation process is disabled, that is, bit CTRL.ANEN is set to zero. This is the LSB (CTRL.SSL) of the forced speed-selection register SS. In conjunction with the MSB (CTRL.SSM), the following encoding is valid: SS=0: 10 Mbit/s SS=1: 100 Mbit/s SS=2: 1000 Mbit/s SS=3: Reserved

Field	Bits	Type	Description
ANEN	12	RW	**Auto-Negotiation Enable** Allows enabling and disabling of the auto-negotiation process capability of the PHY. If enabled, the force bits for duplex mode (CTRL.DPLX) and the speed selection (CTRL.SSM, CTRL.SSL) become inactive. Otherwise, the force bits define the PHY operation. See also IEEE 802.3-2008 22.2.4.1.4 ([1]). **Constants** 0_B **DISABLE** Disable the auto-negotiation protocol 1_B **ENABLE** Enable the auto-negotiation protocol
PD	11	RW	**Power Down** Forces the device into a power-down state where power consumption is the bare minimum requiredto still maintain theMII managementinterface communication. When activating the power-down functionality, the PHY terminates active data links. None of the xMII interfaces work in power-down mode. See also IEEE 802.3-2008 22.2.4.1.5 ([1]). **Constants** 0_B **NORMAL** Normal operational mode 1_B **POWERDOWN** Forces the device into power-down mode
ISOL	10	RW	**Isolate** The isolation mode isolates the PHY from the MAC. MAC interface inputs are ignored, whereas MAC interface outputs are set to tristate (high-impedance). See also IEEE 802.3-2008 22.2.4.1.6 ([1]). **Constants** 0_B **NORMAL** Normal operational mode 1_B **ISOLATE** Isolates the PHY from the MAC
ANRS	9	RWSC	**Restart Auto-Negotiation** Restarts the auto-negotiation process on the MDI. This bit does not take any effect when auto-negotiation is disabled using (CTRL.ANEN). Note that this bit is self-clearing after the auto-negotiation process is initiated. See also IEEE 802.3-2008 22.2.4.1.7 ([1]). **Constants** 0_B **NORMAL** Stay in current mode 1_B **RESTART** Restart auto-negotiation
DPLX	8	RW	**Forced Duplex Mode** Note that this bit only takes effect when the auto-negotiation process is disabled, that is, bit CTRL.ANEN is set to zero. This bit controls the forced duplex mode. It allows forcing of the PHY into full or half-duplex mode. Note that this bit does not take effect in loop-back mode, that is, when bit CTRL.LB is set to one. See also IEEE 802.3-2008 22.2.4.1.8 ([1]). **Constants** 0_B **HD** Half duplex 1_B **FD** Full duplex

Field	Bits	Type	Description
COL	7	RW	**Collision Test** Allows testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency time. See also IEEE 802.3-2008 22.2.4.1.9 ([1]). **Constants** 0_B **DISABLE** Normal operational mode 1_B **ENABLE** Activates the collision test
SSM	6	RW	**Forced Speed-Selection MSB** See the description of SSL. See also IEEE 802.3-2008 22.2.4.1.3 ([1]).
RES	5:0	RO	**Reserved** Write as zero, ignore on read.

Status Register

This register contains status and capability information about the device. Note that all bits are read-only. A write access by the MAC does not have any effect. See also IEEE 802.3-2008 22.2.4.2 ([1]).

STAT	Offset	Reset Value
Status Register	01_H	7949_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CBT4	CBTXF	CBTXH	XBTF	XBTH	CBT2F	CBT2H	EXT	RES	MFPS	ANOK	RF	ANAB	LS	JD	XCAP
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	ROLH	RO	ROLL	ROLH	RO

Field	Bits	Type	Description
CBT4	15	RO	**IEEE 100BASE-T4** Specifies the 100BASE-T4 ability. See also IEEE 802.3-2008 22.2.4.2.1 ([1]). **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBTXF	14	RO	**IEEE 100BASE-TX Full-Duplex** Specifies the 100BASE-TX full-duplex ability. See also IEEE 802.3-2008 22.2.4.2.2 ([1]). **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBTXH	13	RO	**IEEE 100BASE-TX Half-Duplex** Specifies the 100BASE-TX half-duplex ability. See also IEEE 802.3-2008 22.2.4.2.3 ([1]). **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
XBTF	12	RO	**IEEE 10BASE-T Full-Duplex** Specifies the 10 BASE-T full-duplex ability. See also IEEE 802.3-2008 22.2.4.2.4 ([1]). **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
XBTH	11	RO	**IEEE 10BASE-T Half-Duplex** Specifies the 10BASE-T half-duplex ability. See also IEEE 802.3-2008 22.2.4.2.5 ([1]). **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode

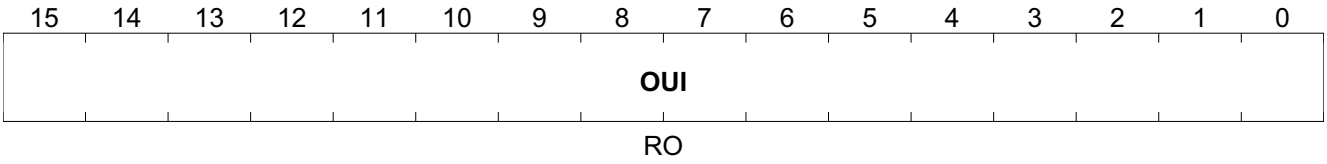
Field	Bits	Type	Description
CBT2F	10	RO	**IEEE 100BASE-T2 Full-Duplex** Specifies the 100BASE-T2 full-duplex ability. See also IEEE 802.3-2008 22.2.4.2.6 ([1]). **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
CBT2H	9	RO	**IEEE 100BASE-T2 Half-Duplex** Specifies the 100BASE-T2 half-duplex ability. See also IEEE 802.3-2008 22.2.4.2.7 ([1]). **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
EXT	8	RO	**Extended Status** The extended status registers are used to specify 1000 Mbit/s speed capabilities in the register XSTAT. See also IEEE 802.3-2008 clause 22.2.4.2.16 ([1]). **Constants** 0_B **DISABLED** No extended status information available in register 15 1_B **ENABLED** Extended status information available in register 15
RES	7	RO	**Reserved** Ignore when read.
MFPS	6	RO	**Management Preamble Suppression** Specifies the MF preamble suppression ability. See also IEEE 802.3-2008 22.2.4.2.9 ([1]). **Constants** 0_B **DISABLED** PHY requires management frames with preamble 1_B **ENABLED** PHY accepts management frames without preamble
ANOK	5	RO	**Auto-Negotiation Completed** Indicates whether the auto-negotiation process is completed or in progress. See also IEEE 802.3-2008 22.2.4.2.10 ([1]). **Constants** 0_B **RUNNING** Auto-negotiation process is in progress 1_B **COMPLETED** Auto-negotiation process is completed
RF	4	ROLH	**Remote Fault** Indicates the detection of a remote fault event. See also IEEE 802.3-2008 22.2.4.2.11 ([1]). **Constants** 0_B **INACTIVE** No remote fault condition detected 1_B **ACTIVE** Remote fault condition detected
ANAB	3	RO	**Auto-Negotiation Ability** Specifies the auto-negotiation ability. See also IEEE 802.3-2008 22.2.4.2.12 ([1]). **Constants** 0_B **DISABLED** PHY is not able to perform auto-negotiation 1_B **ENABLED** PHY is able to perform auto-negotiation

Field	Bits	Type	Description
LS	2	ROLL	**Link Status** Indicates the link status of the PHY to the link partner. See also IEEE 802.3-2008 22.2.4.2.13 ([1]). **Constants** 0_B **INACTIVE** The link is down. No communication with link partner possible. 1_B **ACTIVE** The link is up. Data communication with link partner is possible.
JD	1	ROLH	**Jabber Detect** Indicates that a jabber event has been detected. See also IEEE 802.3-2008 22.2.4.2.14 ([1]). **Constants** 0_B **NONE** No jabber condition detected 1_B **DETECTED** Jabber condition detected
XCAP	0	RO	**Extended Capability** Indicates the availabilityand support ofextended capability registers. See also IEEE 802.3-2008 22.2.4.2.15 ([1]). **Constants** 0_B **DISABLED** Only base registers are supported 1_B **ENABLED** Extended capability registers are supported

PHY Identifier 1

This is the first of two PHY identification registers containing the MSBs of a 32-bit code. This code specifies the Organizationally Unique Identifier (OUI), and the vendor's model and revision number.

PHYID1	Offset	Reset Value
PHY Identifier 1	02_H	$D565_H$

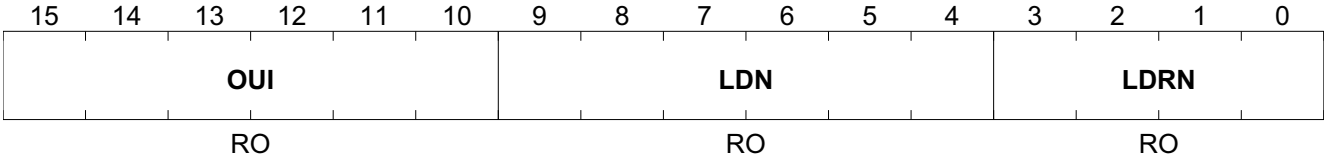


Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier Bits 3:18** This register holds the bits 3:18 of the OUI code for Lantiq Deutschland GmbH, which is specified to be OUI=AC-9A-96. See also IEEE 802.3-2008 22.2.4.3.1 ([1]).

PHY Identifier 2

This is the second of 2 PHY identification registers containing the LSBs of a 32-bit code. This code specifies the Organizationally Unique Identifier (OUI), and the vendor's model and revision number. See also IEEE 802.3-2008 22.2.4.3.1 ([1]).

PHYID2	Offset	Reset Value
PHY Identifier 2	03_H	$A401_H$

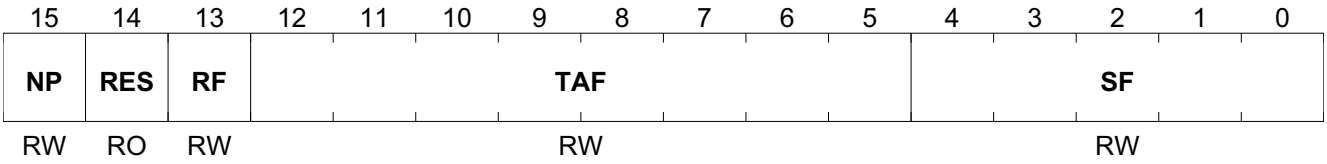


Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24** This register holds the bits 19:24 of the OUI code for Lantiq Deutschland GmbH, which is specified to be OUI=AC-9A-96.
LDN	9:4	RO	**Lantiq Device Number** Specifies the device number, in order to distinguish between several Lantiq products.
LDRN	3:0	RO	**Lantiq Device Revision Number** Specifies the device revision number, in order to distinguish between several versions of this device.

Auto-Negotiation Advertisement

This register contains th e advertised abiliti es of the PHY during au to-negotiation. See also IEEE 802.3-2008 28.2.4.1.3 ([1]), as well as IEEE 802.3-2008 Table 28-2([1]).

AN_ADV	Offset	Reset Value
Auto-Negotiation Advertisement	04_H	$01E1_H$



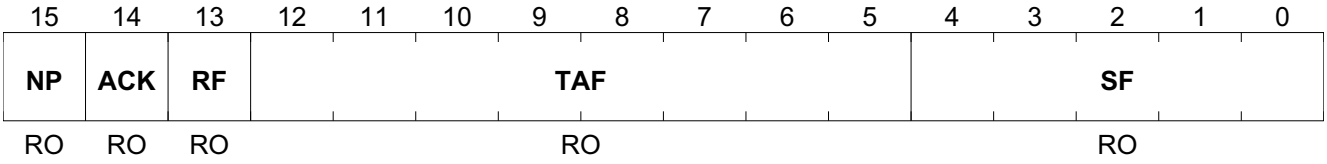
Field	Bits	Type	Description
NP	15	RW	**Next Page** Next-page indication is encoded in bit AN_ADV.NP regardless of the selector field value or link code word encoding. The PHY always advertises NP if a 1000BASE-T mode is advertised during auto-negotiation. See also IEEE 802.3-2008 28.2.1.2.6 ([1]). **Constants** 0_B **INACTIVE** No next page(s) will follow 1_B **ACTIVE** Additional next page(s) will follow
RES	14	RO	**Reserved** Write as zero, ignore on read.
RF	13	RW	**Remote Fault** The remote fault bit allows indication of a fault to the link partner. See also IEEE 802.3-2008 28.2.1.2.4 ([1]). **Constants** 0_B **NONE** No remote fault is indicated 1_B **FAULT** A remote fault is indicated
TAF	12:5	RW	**Technology Ability Field** The technology ability field is an eight-bit wide field containing information indicating supported technologies as defined by the following constants specific to the selector field value. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. In converter mode, the field is always forced to value 0x60. The TAF encoding for the IEEE 802.3 selector (AN_ADV.SF=0x1) is described in IEEE 802.3-2008 Annex 28B.2 and in Annex 28D ([1]). See also IEEE 802.3-2008 28.2.1.2.2 ([1]). **Constants** 00000001_B**XBT_HDX** Advertise 10BASE-T half duplex 00000010_B**XBT_FDX** Advertise 10BASE-T full duplex 00000100_B**DBT_HDX** Advertise 100BASE-TX half duplex 00001000_B**DBT_FDX** Advertise 100BASE-TX full duplex 00010000_B**DBT4** Advertise 100BASE-T4 00100000_B**PS_SYM** Advertise symmetric pause 01000000_B**PS_ASYM** Advertise asymmetric pause 10000000_B**RES** Reserved for future technologies

Field	Bits	Type	Description
SF	4:0	RW	**Selector Field** The selector field is a five-bit wide field for encoding 32 possible messages. Selector field encoding definitions are shown in IEEE 802.3-2008 Annex 28A ([1]). Combinations not specified are reserved for future use. Reserved combinations of the selector field are not to be transmitted. See also IEEE 802.3-2008 28.2.1.2.1 ([1]). **Constants** 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Link-Partner Ability

All of the bits in the auto-negotiation link-partner ability register are read-only. A write to the auto-negotiation link-partner ability register has no effect. This register contains the advertised ability of the link partner (see also IEEE 802.3-2008 Tables 28-3 and 28-4, [1]). The bit definitions are a direct representation of the received link-code word (see also IEEE 802.3-2008 Figure 28-7, [1]). See also IEEE 802.3-2008 22.2.4.3.3 ([1]).

AN_LPA	Offset	Reset Value
Auto-Negotiation Link-Partner Ability	**05_H**	**0000_H**



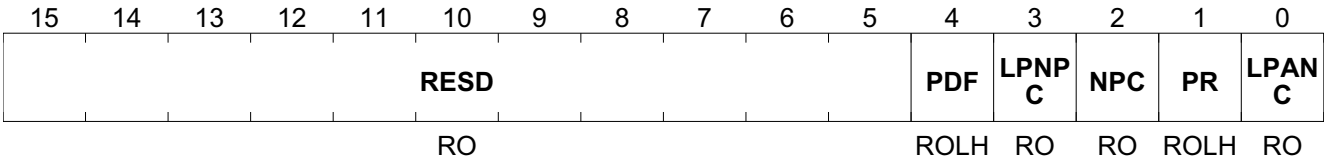
Field	Bits	Type	Description
NP	15	RO	**Next Page** Next-page request indication from the link partner. See also IEEE 802.3-2008 28.2.1.2.6. **Constants** 0_B **INACTIVE** No next page(s) will follow 1_B **ACTIVE** Additional next pages will follow
ACK	14	RO	**Acknowledge** Acknowledgement indication from the link partner's link-code word. See also IEEE 802.3-2008 28.2.1.2.5 ([1]). **Constants** 0_B **INACTIVE** The device did not successfully receive its link partner's link code word 1_B **ACTIVE** The device has successfully received its link partner's link-code word
RF	13	RO	**Remote Fault** Remote fault indication from the link partner. See also IEEE 802.3-2008 28.2.1.2.4 ([1]). **Constants** 0_B **NONE** Remote fault is not indicated by the link partner 1_B **FAULT** Remote fault is indicated by the link partner
TAF	12:5	RO	**Technology Ability Field** Indicates the link-partner capabilities as received from the link partner's link-code word. See also IEEE 802.3-2008 28.2.1.2.2 ([1]). **Constants** 00000001_B**XBT_HDX** Link partner advertised 10BASE-T half duplex 00000010_B**XBT_FDX** Link partner advertised 10BASE-T full duplex. 00000100_B**DBT_HDX** Link partner advertised 100BASE-TX half duplex 00001000_B**DBT_FDX** Link partner advertised 100BASE-TX full duplex 00010000_B**DBT4** Link partner advertised 100BASE-T4 00100000_B**PS_SYM** Link partner advertised symmetric pause 01000000_B**PS_ASYM** Link partner advertised asymmetric pause 10000000_B**RES** Reserved for future technologies; should be zero

Field	Bits	Type	Description
SF	4:0	RO	**Selector Field** The selector field represents one of the 32 possible messages. Note that it must fit to the advertised selector field in AN_ADV.SF. Selector field encoding definitions are shown in IEEE 802.3-2008 Annex 28A ([1]). **Constants** 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Expansion

This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. See also IEEE 802.3-2008 28.2.4.1.5.

AN_EXP	Offset	Reset Value
Auto-Negotiation Expansion	06_H	0004_H



Field	Bits	Type	Description
RESD	15:5	RO	**Reserved** Write as zero, ignore on read.
PDF	4	ROLH	**Parallel Detection Fault** Note that this bit latches high. It is set to zero upon read of AN_EXP. See also IEEE 802.3-2008 28.2.4.1.5 ([1]). **Constants** 0_B **NONE** A fault has not been detected via the parallel detection function 1_B **FAULT** A fault has been detected via the parallel detection function
LPNPC	3	RO	**Link Partner Next-Page Capable** See also IEEE 802.3-2008 28.2.4.1.5 ([1]). **Constants** 0_B **UNABLE** Link partner is unable to exchange next pages 1_B **CAPABLE** Link partner is capable of exchanging next pages
NPC	2	RO	**Next-Page Capable** See also IEEE 802.3-2008 28.2.4.1.5 ([1]). **Constants** 0_B **UNABLE** Local Device is unable to exchange next pages 1_B **CAPABLE** Local device is capable of exchanging next pages
PR	1	ROLH	**Page Received** Note that this bit latches high. It is set to zero upon read of AN_EXP. See also IEEE 802.3-2008 28.2.4.1.5 ([1]). **Constants** 0_B **NONE** A new page has not been received 1_B **RECEIVED** A new page has been received
LPANC	0	RO	**Link Partner Auto-Negotiation Capable** See also IEEE 802.3-2008 28.2.4.1.5 ([1]). **Constants** 0_B **UNABLE** Link partner is unable to auto-negotiate 1_B **CAPABLE** Link partner is auto-negotiation capable

Auto-Negotiation Next-Page Transmit Register

The auto-negotiation next-page transmit register contains the next-page link-code word to be transmitted when next-page ability is supported. On power-up, this register contains the default value of 0x2001, which represents a message page with the message code set to the null message. See also IEEE 802.3-2008 28.2.4.1.6 ([1]).

AN_NPTX	Offset	Reset Value
Auto-Negotiation Next-Page Transmit Register	07_H	2001_H

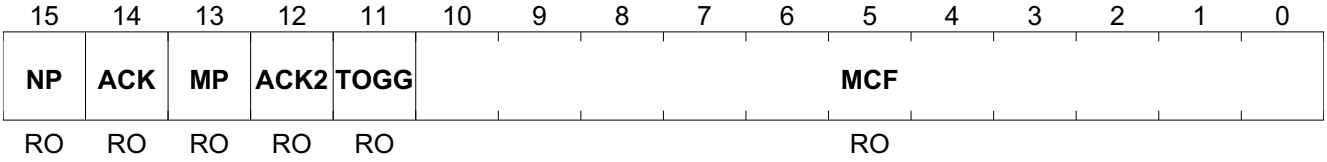
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	RES	MP	ACK2	TOGG	MCF										
RW	RO	RW	RW	RO	RW										

Field	Bits	Type	Description
NP	15	RW	**Next Page** See IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **INACTIVE** Last page 1_B **ACTIVE** Additional next page(s) will follow
RES	14	RO	**Reserved** Write as zeroes, ignore on read.
MP	13	RW	**Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. See IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RW	**Acknowledge 2** See also IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **INACTIVE** Device cannot comply with message 1_B **ACTIVE** Device will comply with message
TOGG	11	RO	**Toggle** See also IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **ZERO** Previous value of the transmitted link-code word was equal to logic ONE 1_B **ONE** Previous value of the transmitted link-code word was equal to logic ZERO
MCF	10:0	RW	**Message or Unformatted Code Field** See also IEEE 802.3-2008 28.2.3.4 ([1]).

Auto-Negotiation Link-Partner Received Next-Page Register

The auto-negotiation link-partner received next-page register contains the next-page link-code word received from the link partner. See also IEEE 802.3-2008 28.2.4.1.7 ([1]).

AN_NPRX	Offset	Reset Value
Auto-Negotiation Link-Partner Received Next-Page Register	08_H	2001_H

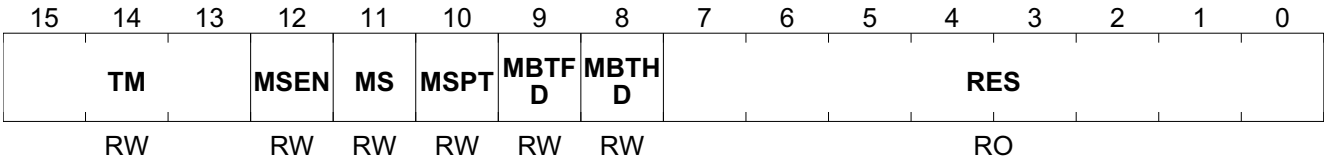


Field	Bits	Type	Description
NP	15	RO	**Next Page** See IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **INACTIVE** No next pages to follow 1_B **ACTIVE** Additional next page(s) will follow
ACK	14	RO	**Acknowledge** See also IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **INACTIVE** The device did not successfully receive its link partner's link-code word 1_B **ACTIVE** The device has successfully received its link partner's link-code word
MP	13	RO	**Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. See also IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RO	**Acknowledge 2** See also IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **INACTIVE** Device cannot comply with message 1_B **ACTIVE** Device will comply with message
TOGG	11	RO	**Toggle** See also IEEE 802.3-2008 28.2.3.4 ([1]). **Constants** 0_B **ZERO** Previous value of the transmitted link-code word was equal to logic ONE 1_B **ONE** Previous value of the transmitted link-code word was equal to logic ZERO
MCF	10:0	RO	**Message or Unformatted Code Field** See also IEEE 802.3-2008 28.2.3.4 ([1]).

Gigabit Control Register

This is the control register used to configure the Gigabit Ethernet behavior of the PHY. See also IEEE 802.3-2008 40.5.1.1 ([1]).

GCTRL	Offset	Reset Value
Gigabit Control Register	09_H	0300_H



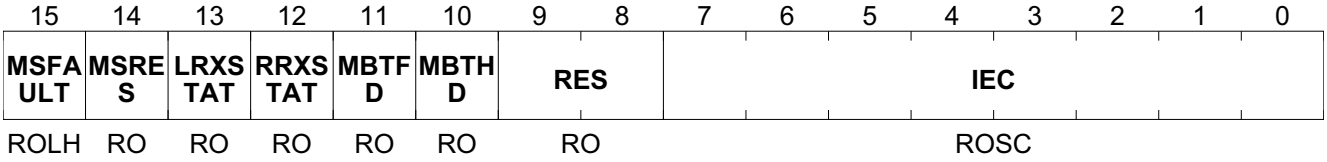
Field	Bits	Type	Description
TM	15:13	RW	**Transmitter Test Mode** This register field allows enabling of the standard transmitter test modes. See also IEEE 802.3-2008 Table 40-7 ([1]). **Constants** 000_B **NOP** Normal operation 001_B **WAV** Test mode 1 transmit waveform test 010_B **JITM** Test mode 2 transmit jitter test in MASTER mode 011_B **JITS** Test mode 3 transmit jitter test in SLAVE mode 100_B **DIST** Test mode 4 transmitter distortion test 101_B **RESD0** Reserved, operations not identified. 110_B **CDIAG** Cable diagnostics. 111_B **ABIST** Analog build in self-test
MSEN	12	RW	**Master/Slave Manual Configuration Enable** See also IEEE 802.3-2008 40.5.1.1 ([1]). **Constants** 0_B **DISABLED** Disable master/slave manual configuration value 1_B **ENABLED** Enable master/slave manual configuration value
MS	11	RW	**Master/Slave Config Value** Allows forcing of master or slave mode manually when AN_GCTRL.MSEN is set to logical one. See also IEEE 802.3-2008 40.5.1.1 ([1]). **Constants** 0_B **SLAVE** Configure PHY as SLAVE during master/slave negotiation, only when AN_GCTRL.MSEN is set to logical one 1_B **MASTER** Configure PHY as MASTER during master/slave negotiation, only when AN_GCTRL.MSEN is set to logical one
MSPT	10	RW	**Master/Slave Port Type** Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function. See also IEEE 802.3-2008 40.5.1.1 ([1]). **Constants** 0_B **SPD** Single-port device 1_B **MPD** Multi-port device

Field	Bits	Type	Description
MBTFD	9	RW	**1000BASE-T Full-Duplex** Advertises the 1000BASE-T full-duplex capability; always forced to 1 in converter mode. See also IEEE 802.3-2008 40.5.1.1 ([1]). **Constants** 0_B **DISABLED** Advertise PHY as not 1000BASE-T full-duplex capable 1_B **ENABLED** Advertise PHY as 1000BASE-T full-duplex capable
MBTHD	8	RW	**1000BASE-T Half-Duplex** Advertises the 1000BASE-T half-duplex capability; always forced to 1 in converter mode. See also IEEE 802.3-2008 40.5.1.1 ([1]). **Constants** 0_B **DISABLED** Advertise PHY as not 1000BASE-T half-duplex capable 1_B **ENABLED** Advertise PHY as 1000BASE-T half-duplex capable
RES	7:0	RO	**Reserved** Write as zero, ignore on read.

Gigabit Status Register

This is the status register used to reflect the Gigabit Ethernet status of the PHY. See also IEEE 802.3-2008 40.5.1.1 ([1]).

GSTAT	Offset	Reset Value
Gigabit Status Register	$0A_H$	0000_H



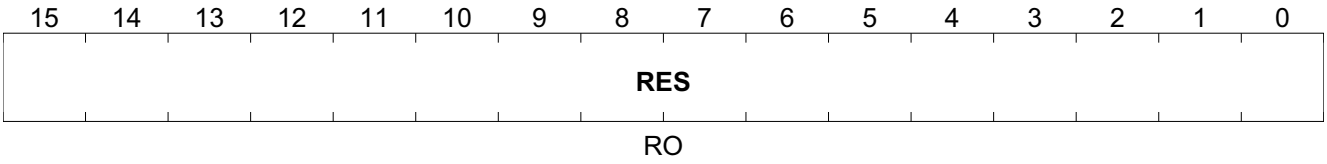
Field	Bits	Type	Description
MSFAULT	15	ROLH	**Master/Slave Manual Configuration Fault** This is a latching high bit. It is cleared upon each read of GSTAT. This bit will self clear on auto-negotiation enable or auto-negotiation complete. This bit will be set to active high if the number of failed master/slave resolutions reaches 7. See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3 ([1]). **Constants** 0_B **OK** Master/slave manual configuration resolved successfully 1_B **NOK** Master/slave manual configuration resolved with a fault
MSRES	14	RO	**Master/Slave Configuration Resolution** See IEEE 802.3 40.5.1.1 register 10 in Table 40-3 ([1]). **Constants** 0_B **SLAVE** Local PHY configuration resolved to SLAVE 1_B **MASTER** Local PHY configuration resolved to MASTER
LRXSTAT	13	RO	**Local Receiver Status** Indicates the status of the local receiver. See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3 ([1]). **Constants** 0_B **NOK** Local receiver not OK 1_B **OK** Local receiver OK
RRXSTAT	12	RO	**Remote Receiver Status** Indicates the status of the remote receiver. See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3 ([1]). **Constants** 0_B **NOK** Remote receiver not OK 1_B **OK** Remote receiver OK
MBTFD	11	RO	**Link-Partner Capable of Operating 1000BASE-T Full-Duplex** See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3 ([1]). **Constants** 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T full-duplex 1_B **ENABLED** Link partner is capable of operating 1000BASE-T full-duplex

Field	Bits	Type	Description
MBTHD	10	RO	**Link-Partner Capable of Operating 1000BASE-T Half-Duplex** See also IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3 ([1]). **Constants** 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T half-duplex 1_B **ENABLED** Link partner is capable of operating 1000BASE-T half-duplex
RES	9:8	RO	**Reserved** Write as zero, ignore on read.
IEC	7:0	ROSC	**Idle Error Count** Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rxerror_status is equal to ERROR. These bits are reset to all zeroes when the GSTAT register is read by the management function or upon execution of the PCS reset function, and are to be held at all ones in case of overflow.

Reserved

Reserved. In IEEE 802.3-2008, this register is used for Power-Sourcing-Equipment (PSE) control functions (see IEEE 802.3-2008 33.6.1.1, [1]), which are not supported by this PHY.

RES11	Offset	Reset Value
Reserved	$0B_H$	0000_H

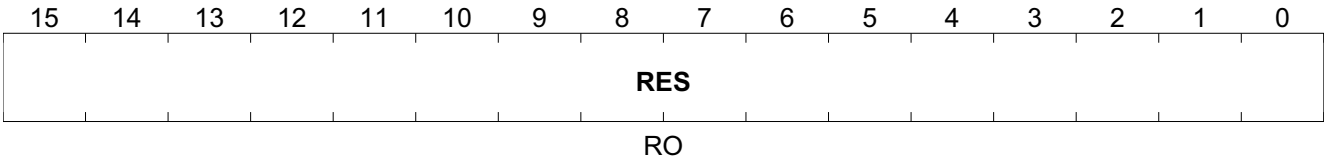


Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

Reserved

Reserved. In IEEE 802.3-2008, this register is used for Power-Sourcing-Equipment (PSE) status functions (see IEEE 802.3-2008 33.6.1.2, [1]), which are not supported by this PHY.

RES12	Offset	Reset Value
Reserved	$0C_H$	0000_H

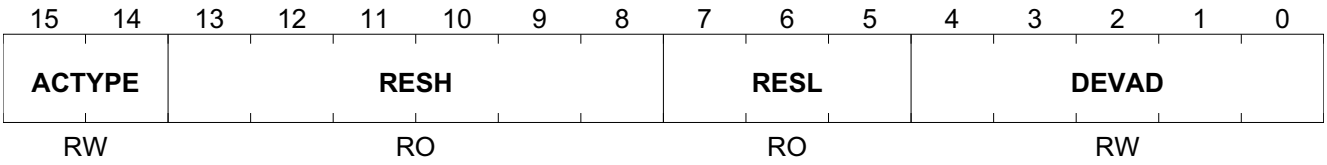


Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

MMD Access Control Register

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. Each MMD maintains its own individual address register, as described in IEEE 802.3-2008 clause 45.2.8 ([1]). The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 clause 45.2. For additional insight into the operation and use of the MMD registers, see IEEE 802.3-2008 clause 22.2.4.3.11, Annex 22D and clause 45.2 ([1]).

MMDCTRL	Offset	Reset Value
MMD Access Control Register	$0D_H$	0000_H

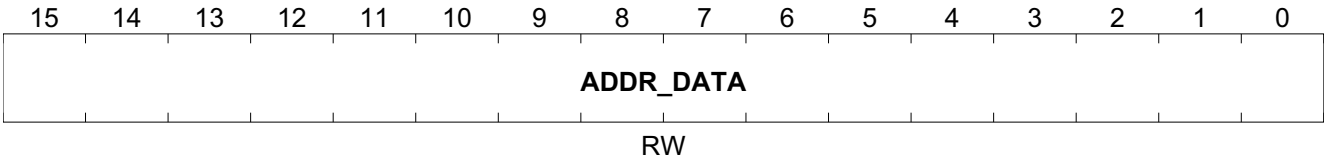


Field	Bits	Type	Description
ACTYPE	15:14	RW	**Access Type Function** If the access of register MMDDATA is an address access (ACTYPE=0) then it is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD's address register direct the register MMDDATA data accesses to the appropriate registers within that MMD. The function field can be set to any of the constants defined (ADDRESS, DATA, DATA_PI, DATA_PIWR). **Constants** 00_B **ADDRESS** Accesses to register MMDDATA access the MMD individual address register 01_B **DATA** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD's address register 10_B **DATA_PI** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD's address register. After this access is complete, for both read and write accesses, the value in the MMD address field is incremented. 11_B **DATA_PIWR** Accesses to register MMDDATA access the register within the MMD selected by the value in the MMD's address register. After this access is complete, for write accesses only, the value in the MMDs address field is incremented. For read accesses, the value in the MMDs address field is not modified.
RESH	13:8	RO	**Reserved** Write as zero, ignored on read.
RESL	7:5	RO	**Reserved** Write as zero, ignored on read.
DEVAD	4:0	RW	**Device Address** The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 clause 45.2 ([1]).

MMD Access Data Register

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space. For more information on MMD access, refer to IEEE 802.3-2008 clause 22.2.4.3.12, clause 45.2 and Annex 22D ([1]).

MMDDATA	Offset	Reset Value
MMD Access Data Register	$0E_H$	0000_H

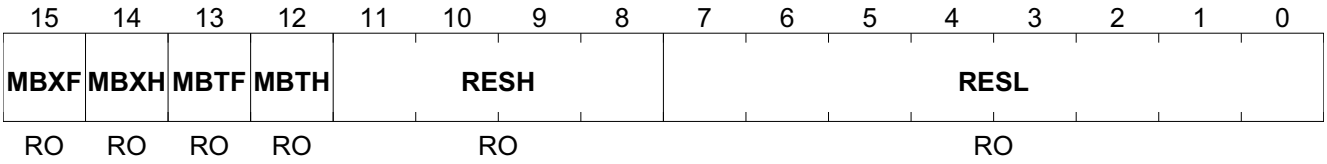


Field	Bits	Type	Description
ADDR_DATA	15:0	RW	**Address or Data Register** This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. Which of the functions is currently valid is defined by the MMDCTRL register.

Extended Status Register

This register contains extended status and capability information about the PHY. Note that all bits are read-only. A write access does not have any effect.

XSTAT	Offset	Reset Value
Extended Status Register	$0F_H$	3000_H



Field	Bits	Type	Description
MBXF	15	RO	**1000BASE-X Full-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X full-duplex. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBXH	14	RO	**1000BASE-X Half-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X half-duplex. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBTF	13	RO	**1000BASE-T Full-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-T full-duplex. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
MBTH	12	RO	**1000BASE-T Half-Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-T full-duplex. **Constants** 0_B **DISABLED** PHY does not support this mode 1_B **ENABLED** PHY supports this mode
RESH	11:8	RO	**Reserved** Ignore when read.
RESL	7:0	RO	**Reserved** Ignore when read.

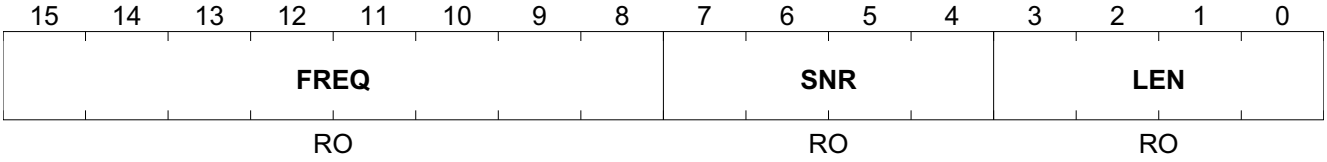
4.2 PHY: PHY-Specific Management Registers

This chapter describes the PHY-specific management registers.

Physical Layer Performance Status

This register reports the PHY performance in the current mode of operation. The content of this register is only valid when the link is up.

PHYPERF	Offset	Reset Value
Physical Layer Performance Status	10_H	$80FF_H$

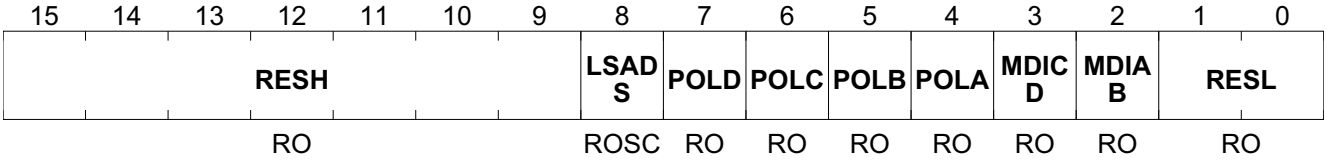


Field	Bits	Type	Description
FREQ	15:8	RO	**Frequency Offset of Link-Partner [ppm]** This register fields reports the measured frequency offset of the receiver in ppm as a signed 2's complement number. Note that a value of -128 (0x80) indicates an invalid number.
SNR	7:4	RO	**Receive SNR Margin [dB]** This register field reports the measured SNR margin of the receiver in dB. The value saturates at a 14-dB SNR margin for very short links and 0 dB for very long links. A value of 15 indicates an invalid number.
LEN	3:0	RO	**Estimated Loop Length (Valid During Link-Up)** This register field reports the estimated loop length compared to a virtually ideal CAT5e straight cable. A value of 15 indicates an invalid number. **Constants** 0000_B**L0** 0 - 10 m 0001_B**L1** 10 - 20 m 0010_B**L2** 20 - 30 m 0011_B**L3** 30 - 40 m 0100_B**L4** 40 - 50 m 0101_B**L5** 50 - 60 m 0110_B**L6** 60 - 70 m 0111_B**L7** 70 - 80 m 1000_B**L8** 80 - 90 m 1001_B**L9** 90 - 100 m 1010_B**L10** 100 - 110 m 1011_B**L11** 110 - 120 m 1100_B**L12** 120 - 130 m 1101_B**L13** 130 - 140 m 1110_B**L14** 140 - ...m 1111_B**INVALID** Invalid number, for example when link is down

Physical Layer Status 1

This register reports PHY lock information, for example link-up, polarity reversals and port mapping. The content of this register is only valid when the link is up.

PHYSTAT1	Offset	Reset Value
Physical Layer Status 1	11_H	0000_H



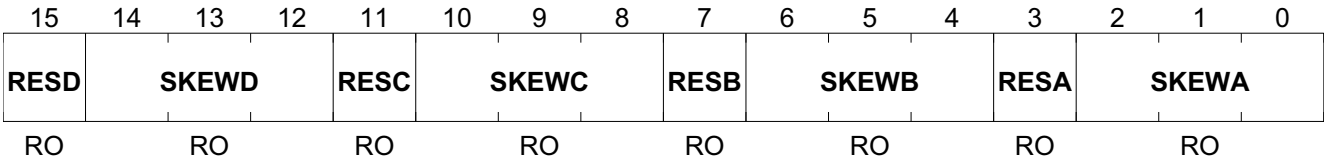
Field	Bits	Type	Description
RESH	15:9	RO	**Reserved** Write as zero, ignored on read.
LSADS	8	ROSC	**Link-Speed Auto-Downspeed Status** Monitors the status of the link speed auto-downspeed controlled in PHYCTL1.LDADS **Constants** 0_B **NORMAL** Did not perform any link speed auto-downspeed 1_B **DETECTED** Detected an auto-downspeed
POLD	7	RO	**Receive Polarity Inversion Status on Port D** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLC	6	RO	**Receive Polarity Inversion Status on Port C** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLB	5	RO	**Receive Polarity Inversion Status on Port B** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
POLA	4	RO	**Receive Polarity Inversion Status on Port A** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion detected
MDICD	3	RO	**Mapping of MDI ports C and D** **Constants** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
MDIAB	2	RO	**Mapping of MDI ports A and B** **Constants** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode

Field	Bits	Type	Description
RESL	1:0	RO	**Reserved** Write as zero, ignored on read.

Physical Layer Status 2

This register reports PHY lock information, for example, pair skews in the GbE mode. The content of this register is only valid when the link is up.

PHYSTAT2	Offset	Reset Value
Physical Layer Status 2	12_H	0000_H



Field	Bits	Type	Description
RESD	15	RO	**Reserved** Write as zero, ignored on read.
SKEWD	14:12	RO	**Receive Skew on Port D** The skew is reported as an unsigned number of symbol periods.
RESC	11	RO	**Reserved** Write as zero, ignored on read.
SKEWC	10:8	RO	**Receive Skew on Port C** The skew is reported as an unsigned number of symbol periods.
RESB	7	RO	**Reserved** Write as zero, ignored on read.
SKEWB	6:4	RO	**Receive Skew on Port B** The skew is reported as an unsigned number of symbol periods.
RESA	3	RO	**Reserved** Write as zero, ignored on read.
SKEWA	2:0	RO	**Receive Skew on Port A** The skew is reported as an unsigned number of symbol periods.

Physical Layer Control 1

This register controls the PHY functions.

PHYCTL1	Offset	Reset Value
Physical Layer Control 1	13_H	0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLOOP			TXOFF	TXADJ				POLD	POLC	POLB	POLA	MDICD	MDIAB	TXEEE10	AMDIX
RW			RW	RW				RW	RW	RW	RW	RW	RW	RW	RW

Field	Bits	Type	Description
TLOOP	15:13	RW	**Test Loop** Configures predefined test loops. **Constants** 000_B **OFF** Test loops are switched off - normal operation. 001_B **NETL** Near-end test loop 010_B **FETL** Far-end test loop 011_B **ECHO** Echo test loop 100_B **RJTL** RL45 connector test loop
TXOFF	12	RW	**Transmitter Off** This register bit allows turning off of the transmitter. This feature might be useful for return loss measurements. **Constants** 0_B **ON** Transmitter is on 1_B **OFF** Transmitter is off
TXADJ	11:8	RW	**Transmit Level Adjustment** Transmit-level adjustment can be used to fine tune the transmit amplitude of the PHY. The amplitude adjustment is valid for all supported speed modes. The adjustment is performed in digits. One digit represents 3.125 percent of the nominal amplitude. The scaling factor is gain = 1 + signed(TXADJ)*2^-7.
POLD	7	RW	**Transmit Polarity Inversion Status on Port D** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
POLC	6	RW	**Transmit Polarity Inversion Status on Port C** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
POLB	5	RW	**Transmit Polarity Inversion Control on Port B** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion

Field	Bits	Type	Description
POLA	4	RW	**Transmit Polarity Inversion Control on Port A** **Constants** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
MDICD	3	RW	**Mapping of MDI Ports C and D** **Constants** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
MDIAB	2	RW	**Mapping of MDI Ports A and B** **Constants** 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
TXEEE10	1	RW	**Transmit Energy-Efficient Ethernet 10BASE-Te Amplitude** This register bit allows enabling of the 10BASE-Teenergy-efficient mode transmitting only with a 1.75 V nominal amplitude. **Constants** 0_B **DISABLED** Transmit the 10BASE-T amplitude, that is, 2.3+ V 1_B **ENABLED** Transmit the 10BASE-Te amplitude, that is, 1.75 V
AMDIX	0	RW	**PHY Performs Auto-MDI/MDI-X or Uses Manual MDI/MDI-X** **Constants** 0_B **MANUAL** PHY uses manual MDI/MDI-X 1_B **AUTO** PHY performs Auto-MDI/MDI-X

Physical Layer Control 2

This register controls the PHY functions.

PHYCTL2	Offset	Reset Value
Physical Layer Control 2	14_H	8006_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LSADS		RESH			CLKSEL	SDETP	STICKY	RESL				ADCR	PSCL	ANPD	LPI
RW		RO			RW	RW	RW	RO				RW	RW	RW	RW

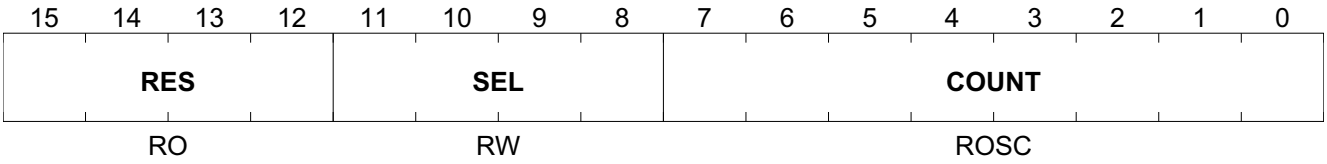
Field	Bits	Type	Description
LSADS	15:14	RW	**Link Speed Auto-Downspeed Control Register** Link speed auto-downspeed is a functionality which allows an Ethernet link to be established even in non-standard harsh cable environments. **Constants** 00_B **OFF** Do not perform link speed auto-downspeed 01_B **ADS2** Perform auto-downspeed of link speed after 2 consecutive failed link-ups 10_B **ADS3** Perform auto-downspeed of link speed after 3 consecutive failed link-ups 11_B **ADS4** Perform auto-downspeed of link speed after 4 consecutive failed link-ups
RESH	13:11	RO	**Reserved** Write as zero, ignored on read.
CLKSEL	10	RW	**Clock-Out Frequency Selection.** Allows specification of the frequency of the clock-out pin. **Constants** 0_B **CLK25M** CLKOUT frequency is 25 MHz 1_B **CLK125M** CLKOUT frequency is 125 MHz
SDETP	9	RW	**Signal Detection Polarity for the 1000BASE-X PHY** Allows specification of the signal detection polarity of the SIGDET input. Although this bit is reset to 0, its actual value depends on the soft pin-strapping configuration if no EEPROM is detected. **Constants** 0_B **LOWACTIVE** SIGDET input is low active 1_B **HIGHACTIVE** SIGDET input is high active
STICKY	8	RW	**Sticky-Bit Handling** Allows enabling/disabling of the sticky-bit handling for all PHY-specific MDIO register bits of type RW, except for the TPGCTRL register. This means that the current content of these registers is left untouched during a software reset if sticky-bit handling is enabled. **Constants** 0_B **OFF** Sticky-bit handling is disabled 1_B **ON** Sticky-bit handling is enabled

Field	Bits	Type	Description
RESL	7:4	RO	**Reserved** Write as zero, ignored on read.
ADCR	3	RW	**ADC Resolution Boost** Allows for the ADC resolution to be increased. **Constants** 0_B **DEFAULT** Default ADC resolution. 1_B **BOOST** ADC resolution boost.
PSCL	2	RW	**Power-Consumption Scaling Depending on Link Quality** Allows enabling/disabling of the power-consumption scaling dependent on the link quality. **Constants** 0_B **OFF** PSCL is disabled 1_B **ON** PSCL is enabled
ANPD	1	RW	**Auto-Negotiation Power Down** Allows enabling/disabling of the power-down modes during auto-negotiation looking for a link partner. **Constants** 0_B **OFF** ANPD is disabled 1_B **ON** ANPD is enabled
LPI	0	RW	**Enable EEE Activation with Legacy MACs** Enables activation of EEE when connected to a legacy MAC. **Constants** 0_B **DISABLE** EEE is disabled 1_B **ENABLE** EEE is enabled

Error Counter

This register controls the error counter. It allows the number of errors detected in the PHY to be counted for monitoring purposes.

ERRCNT	Offset	Reset Value
Error Counter	15_H	0000_H



Field	Bits	Type	Description
RES	15:12	RO	**Reserved** Write as zero, ignored on read.
SEL	11:8	RW	**Select Error Event** Configures the error/event to which the error counter is sensitive. **Constants** 0000_B**RXERR** Receive errors are counted 0001_B**RXACT** Receive frames are counted 0010_B**ESDERR** ESD errors are counted 0011_B**SSDERR** SSD errors are counted 0100_B**TXERR** Transmit errors are counted 0101_B**TXACT** Transmit frames events get counted 0110_B**COL** Collision events get counted
COUNT	7:0	ROSC	**Counter State** This counter state is updated each time the selected error event has been detected. The counter state is reset every time a read operation on this register is performed or the error event is changed. The counter saturates at value 0xFF.

EEPROM Control Register

This register controls the external EEPROM via indirect accesses in the MDIO address space. It can be used to perform read and write accesses to the external EEPROM connected to the PHY. The actual reset value of this register depends on the soft pin-strapping settings.

EECTRL	Offset	Reset Value
EEPROM Control Register	16_H	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EESCAN	EEAF	CSRDET	EEDET	SIZE				ADRMODE	DADR			SPEED		RDWR	EXEC
RW	ROLH	ROLH	ROLH	RW				RW	RW			RW		RO	RO

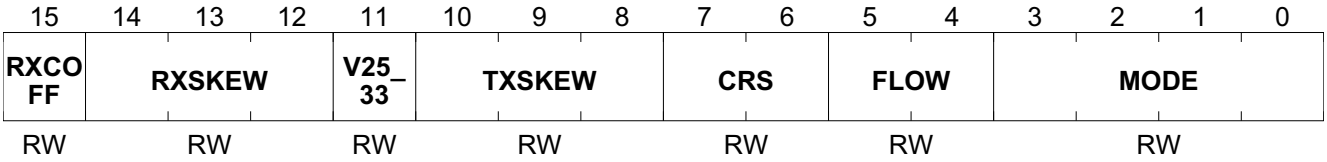
Field	Bits	Type	Description
EESCAN	15	RW	**Enable/Disable EEPROM Configuration Scan Also After SW Reset.** **Constants** 0_B **DISABLE** EEPROM configuration scan is done only after hardware reset 1_B **ENABLE** EEPROM configuration scan is also done after software reset
EEAF	14	ROLH	**EEPROM Access Failure Indication** **Constants** 0_B **UNDETECTED** No EEPROM access error (read or write) has been detected 1_B **DETECTED** An EEPROM access error (read or write) has been detected
CSRDET	13	ROLH	**Configuration Signature Record Detect Indication** **Constants** 0_B **UNDETECTED** CSR has not been found 1_B **DETECTED** CSR has been detected
EEDET	12	ROLH	**EEPROM Detect Indication** **Constants** 0_B **UNDETECTED** No EEPROM is has been detected 1_B **DETECTED** An EEPROM is has been detected

Field	Bits	Type	Description
SIZE	11:8	RW	**EEPROM Size** Defines the size of the connected EEPROM. After reset, this register contains the size extracted from the soft pin-strapping. **Constants** 0000_B**SIZE1K** SIZE1K 0001_B**SIZE2K** SIZE2K 0010_B**SIZE4K** SIZE4K 0011_B**SIZE8K** SIZE8K 0100_B**SIZE16K** SIZE16K 0101_B**SIZE32K** SIZE32K 0110_B**SIZE64K** SIZE64K 0111_B**SIZE128K** SIZE128K 1000_B**SIZE256K** SIZE256K 1001_B**SIZE512K** SIZE512K 1010_B**SIZE1024K** SIZE1024K
ADRMODE	7	RW	**EEPROM Addressing Mode** Defines the device addressing mode of the connected EEPROM. After reset, this register contains the size extracted from the soft pin-strapping. **Constants** 0_B **MODE11** 11-bit addressing mode 1_B **MODE16** 16-bit addressing mode
DADR	6:4	RW	**EEPROM Device Address** Defines the device address of the connected EEPROM. After reset, this register contains the size extracted from the soft pin-strapping.
SPEED	3:2	RW	**EEPROM Speed** Defines the device address of the connected EEPROM. After reset, this register contains the size extracted from the soft pin-strapping. **Constants** 00_B **FRQ_100KHZ** EEPROM is accessed at 100 kHz 01_B **FRQ_400KHZ** EEPROM is accessed at 400 kHz 10_B **FRQ_1_0MHZ** EEPROM is accessed at 1 MHz 11_B **FRQ_3_4MHZ** EEPROM is accesses at 3.4 MHz
RDWR	1	RO	**EEPROM Read/Write Control** **Constants** 0_B **READ** Read access to the external EEPROM 1_B **WRITE** Write access to the external EEPROM
EXEC	0	RO	**Execute EEPROM Read/Write Control** This register is used to initiate an external EEPROM access. The bit remains set until the access is completed. **Constants** 0_B **IDLE** No access to the external EEPROM is currently pending 1_B **EXECUTE** Access to the external EEPROM is currently pending

Media-Independent Interface Control

This register controls the MII interface in its various operational modes.

MIICTRL	Offset	Reset Value
Media-Independent Interface Control	17_H	8000_H



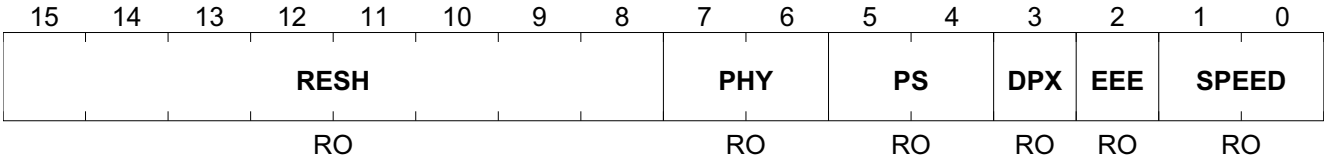
Field	Bits	Type	Description
RXCOFF	15	RW	**Receive Clock Control** Allows disabling of the RXCLK. **Constants** 0_B **OFF** RXCLK is inactive when link is down 1_B **ON** RXCLK is active also then link is down
RXSKEW	14:12	RW	**Receive Timing Skew (RGMII)** Defines the receive timing skew in the RGMII mode using the integrated delay generation on RX_CLK. Note that this register is subject to default reset values which depend on soft pin-strappings. **Constants** 000_B **SKEW_0N0** 0.0 ns timing skew 001_B **SKEW_0N5** 0.5 ns timing skew 010_B **SKEW_1N0** 1.0 ns timing skew 011_B **SKEW_1N5** 1.5 ns timing skew 100_B **SKEW_2N0** 2.0 ns timing skew 101_B **SKEW_2N5** 2.5 ns timing skew 110_B **SKEW_3N0** 3.0 ns timing skew 111_B **SKEW_3N5** 3.5 ns timing skew
V25_33	11	RW	**Power Supply Control for MII Pins** Required for standard compliant operation of RGMII. **Constants** 0_B **V33** MII is operated at 3.3 V 1_B **V25** MII is operated at 2.5 V

Field	Bits	Type	Description
TXSKEW	10:8	RW	**Transmit Timing Skew (RGMII)** Defines the transmit timing skew in the RGMII mode using the integrated delay generation on TX_CLK. Note that this register is subject to default reset values which depend on soft pin-strappings. **Constants** 000_B **SKEW_0N0** 0.0 ns timing skew 001_B **SKEW_0N5** 0.5 ns timing skew 010_B **SKEW_1N0** 1.0 ns timing skew 011_B **SKEW_1N5** 1.5 ns timing skew 100_B **SKEW_2N0** 2.0 ns timing skew 101_B **SKEW_2N5** 2.5 ns timing skew 110_B **SKEW_3N0** 3.0 ns timing skew 111_B **SKEW_3N5** 3.5 ns timing skew
CRS	7:6	RW	**CRS Sensitivity Configuration** **Constants** 00_B **TXRX_RX** HDX:TX+RX, FDX:RX 01_B **TXRX_0** HDX:TX+RX, FDX:0 10_B **RX_RX** HDX:RX, FDX:RX 11_B **RX_0** HDX:RX, FDX:0
FLOW	5:4	RW	**Data Flow Configuration** This register field controls the data flow of the Ethernet frames in the PHY. The MAC interface type is selected by MODE. **Constants** 00_B **COPPER** MAC interface to twisted-pair 11_B **CONVERTER** Media converter: fiber to twisted-pair
MODE	3:0	RW	**MII Interface Mode** This register field controls the operation of the MII interface depending on the FLOW configuration. **Constants** (FLOW = COPPER) 0000_B**RGMII** RGMII mode 0001_B**SGMII** SGMII mode 0010_B**RMII** RMII mode, that is, link speed is forced to 10/100 Mbit/s only 0011_B**RTBI** RTBI mode, that is, link speed is forced to 1000 Mbit/s only 0100_B**GMII** (G)MII mode, that is, MII in 10/100 Mbit/s and GMII in 1000 Mbit/s speed modes 0101_B**TBI** TBI mode, that is, link speed is forced to 1000 Mbit/s only 0110_B**SGMIINC** SGMII mode (without serial clock) 1111_B**TEST** Test mode for SGMII (FLOW = CONVERTER) 0000_B**CONV_X2T1000** Convert 1000BASE-X (without ANEG) to 1000BASE-T. Continuous signal detection is needed to start ANEG on the 1000BASE-T interface. 0001_B**CONV_X2T1000A** Convert 1000BASE-X (with ANEG) to 1000BASE-T. Successful 1000BASE-X negotiation is needed to start ANEG on the 1000BASE-T interface.

Media-Independent Interface Status

This register contains status information of the MII interface.

MIISTAT	Offset	Reset Value
Media-Independent Interface Status	18_H	0000_H



Field	Bits	Type	Description
RESH	15:8	RO	**Reserved** Write as zero, ignored on read.
PHY	7:6	RO	**Active PHY Interface.** **Constants** 00_B **TP** The twisted-pair interface is the active PHY interface 01_B **FIBER** The fiber interface is the active PHY interface 10_B **MII2** The second MII interface is the active PHY interface 11_B **SGMII** The SGMII interface is the active PHY interface
PS	5:4	RO	**Resolved Pause Status for Flow Control** **Constants** 00_B **NONE** No PAUSE 01_B **TX** Transmit PAUSE 10_B **RX** Receive PAUSE 11_B **TXRX** Both transmit and receive PAUSE
DPX	3	RO	**Duplex mode at which the MII currently operates.** **Constants** 0_B **HDX** Half duplex 1_B **FDX** Full duplex
EEE	2	RO	**Resolved Energy-Efficient Ethernet Mode** **Constants** 0_B **OFF** EEE is disabled after auto-negotiation resolution 1_B **ON** EEE is enabled after auto-negotiation resolution
SPEED	1:0	RO	**PHY Speed at which the MII Currently Operates.** **Constants** 00_B **TEN** 10 Mbit/s 01_B **FAST** 100 Mbit/s 10_B **GIGA** 1000 Mbit/s 11_B **RES** Reserved for future use

Interrupt Mask Register

This register defines the mask for the Interrupt Status Register (ISTAT). Each masked interrupt is able to activate the MDINT pin to the management device. The information about the interrupt source can be extracted by reading the ISTAT register. A read operation on the ISTAT register simultaneously clears the interrupts, deactivating MDINT.

IMASK	Offset	Reset Value
Interrupt Mask Register	19_H	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WOL	MSRE	NPRX	NPTX	ANE	ANC	RESH		RESL		ADSC	MDIPC	MDIXC	DXMC	LSPC	LSTC
RW	RW	RW	RW	RW	RW	RO		RO		RW	RW	RW	RW	RW	RW

Field	Bits	Type	Description
WOL	15	RW	**Wake-On-LAN Event Mask** When active and masked in IMASK, the MDINT is activated upon detection of a valid Wake-On-LAN event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MSRE	14	RW	**Master/Slave Resolution Error Mask** When active, MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPRX	13	RW	**Next Page Received Mask** When active, MDINT is activated upon reception of a next page in STD.AN_NPRX. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPTX	12	RW	**Next Page Transmitted Mask** When active, MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
ANE	11	RW	**Auto-Negotiation Error Mask** When active, MDINT is activated upon detection of an auto-negotiation error. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Field	Bits	Type	Description
ANC	10	RW	**Auto-Negotiation Complete Mask** When active, MDINT is activated upon completion of the auto-negotiation process. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
RESH	9:8	RO	**Reserved** Write as zeroes, ignore on read.
RESL	7:6	RO	**Reserved** Write as zeroes, ignore on read.
ADSC	5	RW	**Link-Speed Auto-Downspeed Detect Mask** When active, MDINT is activated upon detection of a link speed auto-downspeed event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIPC	4	RW	**MDI Polarity Change Detect Mask** When active, MDINT is activated upon detection of an MDI polarity change event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIXC	3	RW	**MDIX Change Detect Mask** When active, MDINT is activated upon detection of an MDI/MDIX cross-over change event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
DXMC	2	RW	**Duplex Mode Change Mask** When active, MDINT is activated upon detection of full- or half-duplex change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSPC	1	RW	**Link Speed Change Mask** When active, MDINT is activated upon detection of link speed change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSTC	0	RW	**Link State Change Mask** When active, MDINT is activated upon detection of link status change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Interrupt Status Register

This register defines the Interrupt Status Register (ISTAT). Each masked interrupt (IMASK) is able to activate the MDINT pin to the management device. The information about the interrupt source can be extracted by reading the ISTA register. A read operation on the ISTAT register simultaneously clears the interrupts and this deactivates MDINT.

ISTAT	Offset	Reset Value
Interrupt Status Register	$1A_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WOL	MSRE	NPRX	NPTX	ANE	ANC	RESH		RESL		ADSC	MDIPC	MDIXC	DXMC	LSPC	LSTC
ROLH	ROLH	ROLH	ROLH	ROLH	ROLH	ROLH		ROLH		ROLH	ROLH	ROLH	ROLH	ROLH	ROLH

Field	Bits	Type	Description
WOL	15	ROLH	**Wake-On-LAN Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a valid Wake-On-LAN event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MSRE	14	ROLH	**Master/Slave Resolution Error Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPRX	13	ROLH	**Next Page Received Interrupt Status** When active and masked in IMASK, the MDINT is activated upon reception of a next page in STD.AN_NPRX. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
NPTX	12	ROLH	**Next Page Transmitted Interrupt Status** When active and masked in IMASK, the MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
ANE	11	ROLH	**Auto-Negotiation Error Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an auto-negotiation error. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

Field	Bits	Type	Description
ANC	10	ROLH	**Auto-Negotiation Complete Interrupt Status** When active and masked in IMASK, the MDINT is activated upon completion of the auto-negotiation process. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
RESH	9:8	ROLH	**Reserved** Write as zeroes, ignore on read.
RESL	7:6	ROLH	**Reserved** Write as zeroes, ignore on read.
ADSC	5	ROLH	**Link Speed Auto-Downspeed Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a link speed auto-downspeed event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIPC	4	ROLH	**MDI Polarity Change Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an MDI polarity change event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
MDIXC	3	ROLH	**MDIX Change Detect Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of an MDI/MDIX cross-over change event. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
DXMC	2	ROLH	**Duplex Mode Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of a full or half-duplex change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSPC	1	ROLH	**Link Speed Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of link speed change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated
LSTC	0	ROLH	**Link State Change Interrupt Status** When active and masked in IMASK, the MDINT is activated upon detection of link status change. **Constants** 0_B **INACTIVE** Interrupt is masked out 1_B **ACTIVE** Interrupt is activated

LED Control Register

This register contains control bits to allow for direct access to the LEDs. A directly controlled LED must disable the integrated LED function as specified by the more sophisticated LED control registers in page LED.

LED	Offset	Reset Value
LED Control Register	$1B_H$	$0F00_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESH				LED3 EN	LED2 EN	LED1 EN	LED0 EN	RESL				LED3 DA	LED2 DA	LED1 DA	LED0 DA
RO				RW	RW	RW	RW	RO				RW	RW	RW	RW

Field	Bits	Type	Description
RESH	15:12	RO	**Reserved** Write as zero, ignored on read.
LED3EN	11	RW	**Enable the integrated function of LED3** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED3DA. **Constants** 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED2EN	10	RW	**Enable the integrated function of LED2** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED2DA. **Constants** 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED1EN	9	RW	**Enable the Integrated Function of LED1** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED1DA. **Constants** 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
LED0EN	8	RW	**Enable the Integrated Function of LED0** Write a logic 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED0DA. **Constants** 0_B **DISABLE** Disables the integrated LED function 1_B **ENABLE** Enables the integrated LED function
RESL	7:4	RO	**Reserved** Write as zero, ignored on read.

Field	Bits	Type	Description
LED3DA	3	RW	**Direct Access to LED3** Write a logic 1 to this bit to illuminate the LED. Note that LED3EN must be set to logic zero. **Constants** 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED2DA	2	RW	**Direct Access to LED2** Write a logic 1 to this bit to illuminate the LED. Note that LED2EN must be set to logic zero. **Constants** 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED1DA	1	RW	**Direct Access to LED1** Write a logic 1 to this bit to illuminate the LED. Note that LED1EN must be set to logic zero. **Constants** 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED
LED0DA	0	RW	**Direct Access to LED0** Write a logic 1 to this bit to illuminate the LED. Note that LED0EN must be set to logic zero. **Constants** 0_B **OFF** Switch off the LED 1_B **ON** Switch on the LED

Test-Packet Generator Control

This register controls the operation of the integrated Test-Packet Generator (TPG). Note that this module is only used for testing purposes.

TPGCTRL	Offset	Reset Value
Test-Packet Generator Control	$1C_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESH1		MODE	RESH0	IPGL		TYPE		RESL1	SIZE			RESL0		START	EN
RO		RW	RO	RW		RW		RO	RW			RO		RW	RW

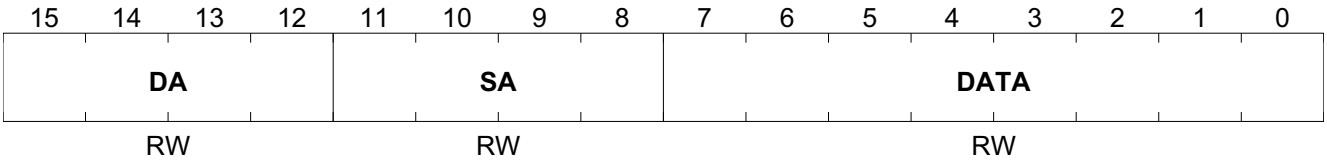
Field	Bits	Type	Description
RESH1	15:14	RO	**Reserved** Write as zero, ignore on read.
MODE	13	RW	**Mode of the TPG** Configures the packet generation mode **Constants** 0_B **BURST** Send bursts of 10,000 packets continuously 1_B **SINGLE** Send a single packet
RESH0	12	RO	**Reserved** Write as zero, ignore on read.
IPGL	11:10	RW	**Inter-Packet Gap Length** Configures the length of the inter-packet gap in bit times. **Constants** 00_B **BT48** Length is 48 bit times 01_B **BT96** Length is 96 bit times 10_B **BT960** Length is 960 bit times 11_B **BT9600** Length is 9600 bit times
TYPE	9:8	RW	**Packet Data Type** Configures the packet data type to be either predefined, byte increment or random. If pre-defined, the content of the register TPGDATA is used repetitively. **Constants** 00_B **RANDOM** Use random data as the packet content 01_B **BYTEINC** Use byte increment as the packet content 10_B **PREDEF** Use pre-defined content of the register TPGDATA
RESL1	7	RO	**Reserved.** Write as zero, ignore on read.

Field	Bits	Type	Description
SIZE	6:4	RW	**Packet Size** Configures the size of the generated Ethernet packets in bytes. The size includes DA, SA, length/type, payload and FCS. **Constants** 000_B **B64** Packet length is 64 bytes 001_B **B128** Packet length is 128 bytes 010_B **B256** Packet length is 256 bytes 011_B **B512** Packet length is 512 bytes 100_B **B1024** Packet length is 1024 bytes 101_B **B1518** Packet length is 1518 bytes 110_B **B9600** Packet length is 9600 bytes
RESL0	3:2	RO	**Reserved** Write as zero, ignore on read.
START	1	RW	**Start or Stop TPG Data Generation.** Starts the TPG data generation. Depending on the MODE, the TPG sends only 1 single packet or chunks of 10,000 packets until stopped. **Constants** 0_B **STOP** Stops the TPG data generation 1_B **START** Starts the TPG data generation
EN	0	RW	**Enable the TPG** Enables the TPG for data generation. **Constants** 0_B **DISABLE** Disables the TPG 1_B **ENABLE** Enables the TPG

Test-Packet Generator Data

Specifies the payload data to be used when sending a non-random data packet. All payload data bytes are sent with this value.

TPGDATA	Offset	Reset Value
Test-Packet Generator Data	$1D_H$	$00AA_H$

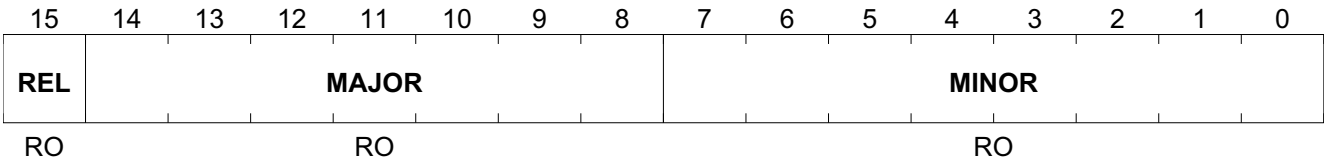


Field	Bits	Type	Description
DA	15:12	RW	**Destination Address** Configures the destination address nibble. The Source Address builds up to 00-03-19-FF-FF-F[DA].
SA	11:8	RW	**Source Address** Configures the source address nibble. The source address builds up to 00-03-19-FF-FF-F[SA].
DATA	7:0	RW	**Data Byte to be Transmitted** This is the content of the payload bytes in the frame.

Firmware Version Register

This register contains the version of the PHY firmware.

FWV	Offset	Reset Value
Firmware Version Register	**$1E_H$**	**8406_H**

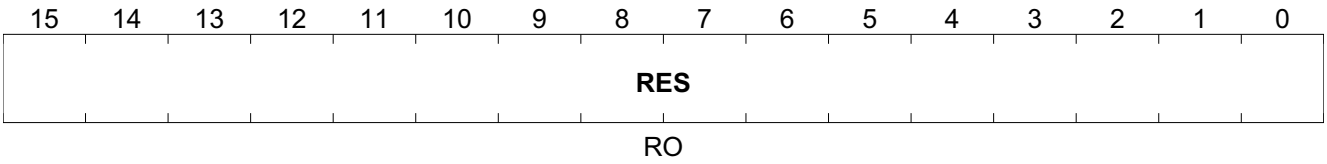


Field	Bits	Type	Description
REL	15	RO	**Release Indication** This parameter indicates either a test or a release version. **Constants** 0_B **TEST** Indicates a test version 1_B **RELEASE** Indicates a released version
MAJOR	14:8	RO	**Major Version Number** Specifies the main version release number of the firmware.
MINOR	7:0	RO	**Minor Version Number** Specifies the sub-version release number of the firmware.

Reserved

Reserved for future use.

RES1F	Offset	Reset Value
Reserved	**$1F_H$**	**0000_H**



Field	Bits	Type	Description
RES	15:0	RO	**Reserved** Write as zero, ignored on read.

5 MMD Registers

This chapter defines the MMD Registers (MDIO Manageable Device Registers). These registers are indirectly addressable using the MDIO registers MMDCTRL (Page 105) and MMDDATA (Page 106). Most of these registers are standardized registers which must be mapped to these MMD addresses for compliant operation.

Table 34 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
EEE			
EEE_CTRL1	EEE Control Register 1	03.0000_H	134
EEE_STAT1	EEE Status Register 1	03.0001_H	135
EEE_CAP	EEE Capability Register	03.0014_H	136
EEE_WAKERR	EEE Wake Time Fault Count Register	03.0016_H	137
ANEG			
EEE_AN_ADV	EEE Auto-Negotiation Advertisement Register	$07.003C_H$	138
EEE_AN_LPADV	EEE Auto-Negotiation Link-Partner Advertisement Register	$07.003D_H$	139
EEPROM			
EEPROM	EEPROM Content [Memory]	$1E.0000_H$	140
INTERNAL			
LEDCH	LED Configuration	$1F.01E0_H$	141
LEDCL	LED Configuration	$1F.01E1_H$	143
LED0H	Configuration for LED Pin 0	$1F.01E2_H$	144
LED0L	Configuration for LED Pin 0	$1F.01E3_H$	146
LED1H	Configuration for LED Pin 1	$1F.01E4_H$	144
LED1L	Configuration for LED Pin 1	$1F.01E5_H$	146
LED2H	Configuration for LED Pin 2	$1F.01E6_H$	144
LED2L	Configuration for LED Pin 2	$1F.01E7_H$	146
EEE_RXERR_LINK_FAIL_H	High Byte of the EEE Link-Fail Counter	$1F.01EA_H$	148
EEE_RXERR_LINK_FAIL_L	Low Byte of the EEE Link-Fail Counter	$1F.01EB_H$	148
MII2CTRL	MII2 Control	$1F.01EC_H$	149
LEG_LPI_CFG0	Legacy LPI Configuration Register 0	$1F.01ED_H$	150
LEG_LPI_CFG1	Legacy LPI Configuration Register 1	$1F.01EE_H$	150
WOLCTRL	Wake-On-LAN Control Register	$1F.0781_H$	151
WOLAD0	Wake-On-LAN Address Byte 0	$1F.0783_H$	152
WOLAD1	Wake-On-LAN Address Byte 1	$1F.0784_H$	152
WOLAD2	Wake-On-LAN Address Byte 2	$1F.0785_H$	152
WOLAD3	Wake-On-LAN Address Byte 3	$1F.0786_H$	152
WOLAD4	Wake-On-LAN Address Byte 4	$1F.0787_H$	152

Table 34 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
WOLAD5	Wake-On-LAN Address Byte 5	$1F.0788_H$	152
WOLPW0	Wake-On-LAN SecureON Password Byte 0	$1F.0789_H$	153
WOLPW1	Wake-On-LAN SecureON Password Byte 1	$1F.078A_H$	153
WOLPW2	Wake-On-LAN SecureON Password Byte 2	$1F.078B_H$	153
WOLPW3	Wake-On-LAN SecureON Password Byte 3	$1F.078C_H$	153
WOLPW4	Wake-On-LAN SecureON Password Byte 4	$1F.078D_H$	153
WOLPW5	Wake-On-LAN SecureON Password Byte 5	$1F.078E_H$	153
LEG_LPI_CFG2	Legacy LPI Configuration Register 2	$1F.0EB5_H$	154
LEG_LPI_CFG3	Legacy LPI Configuration Register 3	$1F.0EB7_H$	154

The registers are addressed wordwise.

Unused registers bits are written with zeros; their values are ignored when read. These unused bits are marked by "-" in the following register diagrams.

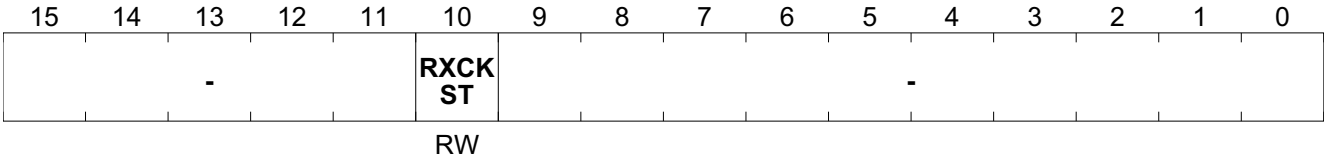
5.1 EEE: Standard EEE Registers for MMD=0x03

This section describes the EEE registers for MMD device 0x03.

EEE Control Register 1

EEE Control Register 1.

EEE_CTRL1	Offset	Reset Value
EEE Control Register 1	**03.0000_H**	**0000_H**

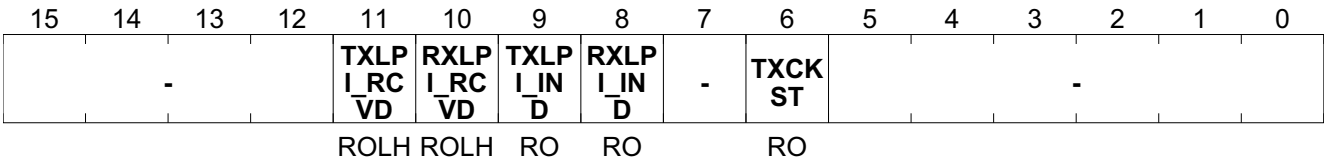


Field	Bits	Type	Description
RXCKST	10	RW	**Receive Clock Stoppable** The MAC can set this bit to active to allow the PHY to stop the clocking during the LPI_MODE. **Constants** 0_B **DISABLE** The PHY must not stop the xMII clock during LPI_MODE 1_B **ENABLE** The PHY can stop the xMII clock during LPI_MODE

EEE Status Register 1

EEE Status Register 1.

EEE_STAT1	Offset	Reset Value
EEE Status Register 1	03.0001_H	0000_H



Field	Bits	Type	Description
TXLPI_RCVD	11	ROLH	**TXLPI Has Been Received** **Constants** 0_B **INACTIVE** LPI has not been received 1_B **ACTIVE** LPI has been received
RXLPI_RCVD	10	ROLH	**RXLPI Has Been Received** **Constants** 0_B **INACTIVE** LPI has not been received 1_B **ACTIVE** LPI has been received
TXLPI_IND	9	RO	**TXLPI Indication** **Constants** 0_B **INACTIVE** LPI is currently inactive 1_B **ACTIVE** LPI is currently active
RXLPI_IND	8	RO	**RXLPI Has Been Received** **Constants** 0_B **INACTIVE** LPI is currently inactive 1_B **ACTIVE** LPI is currently active
TXCKST	6	RO	**Transmit Clock Stoppable** The PHY must set this bit to allow the MAC to stop the clocking during the LPI_MODE. The MAC may stop its clock during LPI if this bit is set to active. **Constants** 0_B **DISABLE** The PHY is not able to accept stopped transmit clocks 1_B **ENABLE** The PHY is able to accept a stopped transmit clock during LPI_MODE

EEE Capability Register

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type.

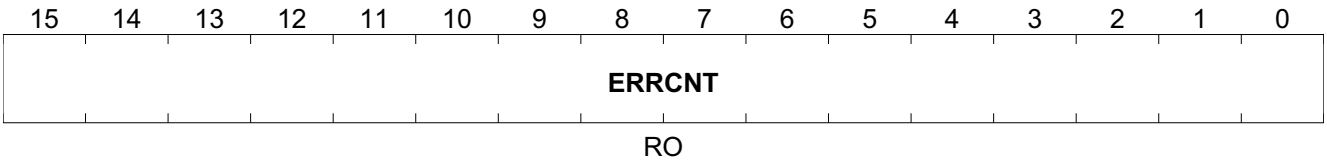
EEE_CAP	Offset	Reset Value
EEE Capability Register	03.0014_H	0006_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-									EEE_10GBKR	EEE_10GBKX4	EEE_1000BKX	EEE_10GBT	EEE_1000BT	EEE_100BTX	-
									RO	RO	RO	RO	RO	RO	

Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

EEE Wake Time Fault Count Register

EEE_WAKERR	Offset	Reset Value
EEE Wake Time Fault Count Register	03.0016_H	0000_H



Field	Bits	Type	Description
ERRCNT	15:0	RO	**TXLPI Has Been Received** This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and may occur during a refresh or a wake-up as defined by the PHY. This 16-bit counter is reset to all zeroes when the EEE wake error counter is read by the management function or upon execution of the PCS reset. It is held at all ones in case of overflow.

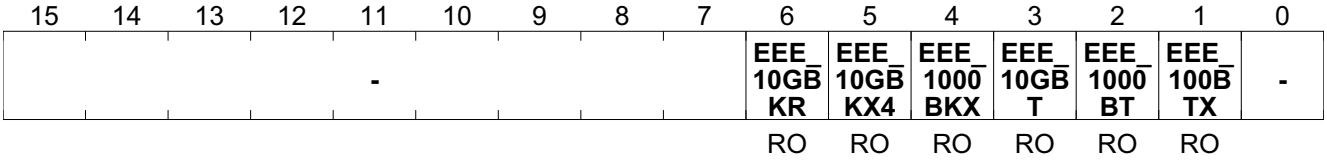
5.2 ANEG: Standard Auto-Negotiation Registers for MMD=0x07

This register file contains the auto-negotiation registers for MMD device 0x07 (only supporting EEE specifics).

EEE Auto-Negotiation Advertisement Register

This register defines the EEE advertisement that is sent in the unformatted next page following an EEE technology message code as defined in 28C.12. The 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to the bits in the unformatted next page. For PHYs that negotiate extended next-page support, the 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to bits U10 to U0 respectively of the extended next-page unformatted code field.

EEE_AN_ADV	Offset	Reset Value
EEE Auto-Negotiation Advertisement Register	$07.003C_H$	0006_H



Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

EEE Auto-Negotiation Link-Partner Advertisement Register

All of the bits in the EEE LP advertisement register are read only. A write operation to the EEE LP advertisement register has no effect. After the AN process has been completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are the same as for the EEE AN advertisement register.

EEE_AN_LPADV	Offset	Reset Value
EEE Auto-Negotiation Link-Partner Advertisement Register	$07.003D_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-									EEE_10GBKR	EEE_10GBKX4	EEE_1000BKX	EEE_10GBT	EEE_1000BT	EEE_100BTX	-
									RO	RO	RO	RO	RO	RO	

Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** **Constants** 0_B **DISABLED** This PHY mode is not supported for EEE 1_B **ENABLE** This PHY mode is supported for EEE

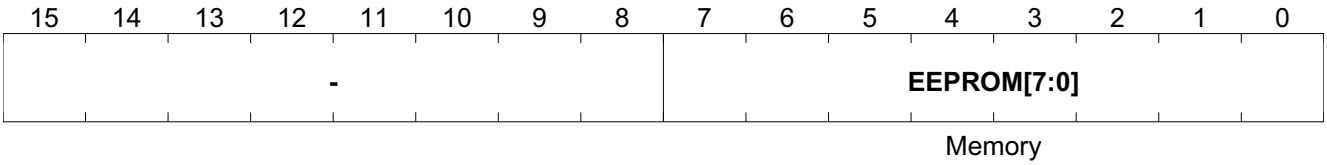
5.3 EEPROM: EEPROM Address Space (MMD=0x1E)

This register file contains the EEPROM address space (MMD=0x1E).

EEPROM Content (Memory)

The EEPROM is indirectly addressable via MMD 0x1E.

EEPROM	Offset	Reset Value
EEPROM Content	$1E.0000_H$... $1EFFFF_H$	-



Field	Bits	Type	Description
EEPROM	8:0	Memory	**EEPROM Content** The EEPROM is indirectly addressable via MMD 0x1E.

5.4 INTERNAL: Internal Address Space (MMD=0x1F)

This register file contains the PHY internal address space (MMD=0x1F).

LED Configuration

This register must be used to configure the complex functions of the LED behavior. Complex functions are of a higher priority than direct LED functions as of registers MMD.INTERNAL.LEDxH/L. When the PHY enters a state which is defined to activate complex LED functions, all LEDs are controlled according to the type of the complex function.

LEDCH	Offset	Reset Value
LED Configuration	$1F.01E0_H$	$00C5_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								FBF		SBF		-	NACS		
								RW		RW			RW		

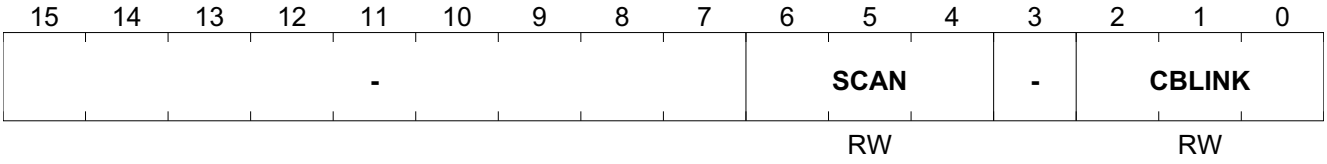
Field	Bits	Type	Description
FBF	7:6	RW	**Fast Blink Frequency** This register must be used to configure the fast-blinking frequency. Note that this setting implicitly defines the pulse-stretching width. **Constants** 00_B **F02HZ** 2 Hz blinking frequency 01_B **F04HZ** 4 Hz blinking frequency 10_B **F08HZ** 8 Hz blinking frequency 11_B **F16HZ** 16 Hz blinking frequency
SBF	5:4	RW	**Slow Blink Frequency** This register must be used to configure the slow-blinking frequency. **Constants** 00_B **F02HZ** 2 Hz blinking frequency 01_B **F04HZ** 4 Hz blinking frequency 10_B **F08HZ** 8 Hz blinking frequency 11_B **F16HZ** 16 Hz blinking frequency

Field	Bits	Type	Description
NACS	2:0	RW	**Inverse of SCAN Function** This configuration defines in which state the "complex SCAN" should be activated. The complex SCAN performs running off which turns back and forth between the first and last LED. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. **Constants** 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running

LED Configuration

The register must be used to configure the complex functions of the LED behavior. Complex functions are of a higher priority than direct LED functions as of registers MMD.INTERNAL.LEDxH/L. When the PHY enters a state which is defined to activate complex LED functions all LEDs are controlled according to the type of the complex function.

LEDCL	Offset	Reset Value
LED Configuration	$1F.01E1_H$	0067_H

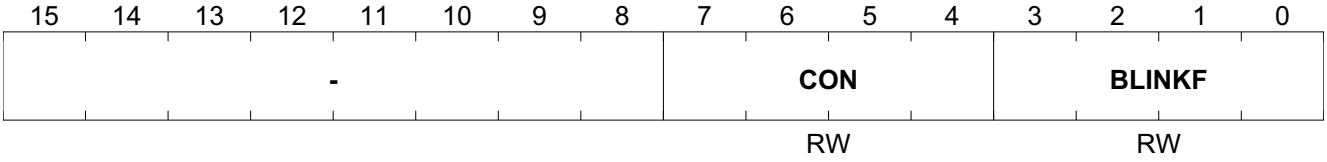


Field	Bits	Type	Description
SCAN	6:4	RW	**Complex SCAN Configuration** This configuration defines in which state the "complex SCAN" should be activated. The complex SCAN performs running on which turns back and forth between the first and last LED. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. **Constants** 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running
CBLINK	2:0	RW	**Complex Blinking Configuration** This configuration defines in which state the "complex blinking" should be activated. The complex blinking performs a blinking at the fast-blinking frequency on all LEDs simultaneously. This function can be used to indicate a special mode of the PHY such as cable-diagnostics or test. The speed is dependent on the MMD.INTERNAL.LEDCH.FBF setting. **Constants** 000_B **NONE** No Function 001_B **LINK** Complex function enabled when link is up 010_B **PDOWN** Complex function enabled when device is powered-down 011_B **EEE** Complex function enabled when device is in EEE mode 100_B **ANEG** Complex function enabled when auto-negotiation is running 101_B **ABIST** Complex function enabled when analog self-test is running 110_B **CDIAG** Complex function enabled when cable diagnostics are running 111_B **TEST** Complex function enabled when test mode is running

Configuration for LED Pin 0

This register configures the behavior of the LED depending on pre-defined states or events the PHY has entered into or raised. Since more than one event/state can be active at the same time, more than one function might apply simultaneously. The priority from highest to lowest is given by the order PULSE, BLINKS, BLINKF, CON.

LED0H	Offset	Reset Value
Configuration for LED Pin 0	$1F.01E2_H$	0070_H



Field	Bits	Type	Description
CON	7:4	RW	**Constant On Configuration** The Constant-ON field selects in which PHY states the LED is constantly on. **Constants** 0000_B**NONE** LED does not light up constantly 0001_B**LINK10** LED is on when link is 10 Mbit/s 0010_B**LINK100** LED is on when link is 100 Mbit/s 0011_B**LINK10X** LED is on when link is 10/100 Mbit/s 0100_B**LINK1000** LED is on when link is 1000 Mbit/s 0101_B**LINK10_0** LED is on when link is 10/1000 Mbit/s 0110_B**LINK100X** LED is on when link is 100/1000 Mbit/s 0111_B**LINK10XX** LED is on when link is 10/100/1000 Mbit/s 1000_B**PDOWN** LED is on when device is powered-down 1001_B**EEE** LED is on when device is in EEE mode 1010_B**ANEG** LED is on when auto-negotiation is running 1011_B**ABIST** LED is on when analog self-test is running 1100_B**CDIAG** LED is on when cable diagnostics are running 1101_B**COPPER** LED is on when the COPPER interface is selected 1110_B**FIBER** LED is on when the FIBER or an interface other than copper is selected 1111_B**RESERVED** Reserved for future use

Field	Bits	Type	Description
BLINKF	3:0	RW	**Fast Blinking Configuration** The Blink-F Field selects in which PHY states the LED blinks with the pre-defined fast frequency. **Constants** 0000_B**NONE** No Blinking 0001_B**LINK10** Blink when link is 10 Mbit/s 0010_B**LINK100** Blink when link is 100 Mbit/s 0011_B**LINK10X** Blink when link is 10/100 Mbit/s 0100_B**LINK1000** Blink when link is 1000 Mbit/s 0101_B**LINK10_0** Blink when link is 10/1000 Mbit/s 0110_B**LINK100X** Blink when link is 100/1000 Mbit/s 0111_B**LINK10XX** Blink when link is 10/100/1000 Mbit/s 1000_B**PDOWN** Blink when device is powered-down 1001_B**EEE** Blink when device is in EEE mode 1010_B**ANEG** Blink when auto-negotiation is running 1011_B**ABIST** Blink when analog self-test is running 1100_B**CDIAG** Blink when cable diagnostics are running

Similar Registers

The following registers are identical to the Register **LED0H** defined above.

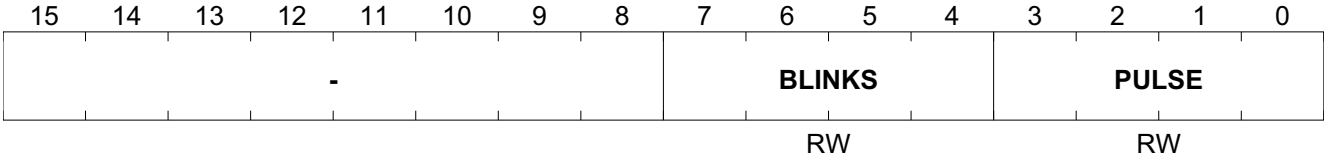
Table 35 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
LED1H	Configuration for LED Pin 1	$1F.01E4_H$	0020_H
LED2H	Configuration for LED Pin 2	$1F.01E6_H$	0040_H
LED3H	Configuration for LED Pin 3	$1F.01E8_H$	0040_H

Configuration for LED Pin 0

This register configures the behavior of the LED depending on pre-defined states or events the PHY has entered into or raised. Since more than one event or state can be active at the same time, more than one function might apply simultaneously. The priority from highest to lowest is given by the order PULSE, BLINKS, BLINKF, CON.

LED0L	Offset	Reset Value
Configuration for LED Pin 0	$1F.01E3_H$	0003_H



Field	Bits	Type	Description
BLINKS	7:4	RW	**Slow Blinking Configuration** The Blink-S field selects in which PHY states the LED blinks with the pre-defined slow frequency. **Constants** 0000_B**NONE** No Blinking 0001_B**LINK10** Blink when link is 10 Mbit/s 0010_B**LINK100** Blink when link is 100 Mbit/s 0011_B**LINK10X** Blink when link is 10/100 Mbit/s 0100_B**LINK1000** Blink when link is 1000 Mbit/s 0101_B**LINK10_0** Blink when link is 10/1000 Mbit/s 0110_B**LINK100X** Blink when link is 100/1000 Mbit/s 0111_B**LINK10XX** Blink when link is 10/100/1000 Mbit/s 1000_B**PDOWN** Blink when device is powered-down 1001_B**EEE** Blink when device is in EEE mode 1010_B**ANEG** Blink when auto-negotiation is running 1011_B**ABIST** Blink when analog self-test is running 1100_B**CDIAG** Blink when cable diagnostics are running
PULSE	3:0	RW	**Pulsing Configuration** The pulse field is a mask field by which certain events can be combined, e.g. TXACT|RXACT, to generate a pulse on the LED in case such an event has been detected. **Constants** 0000_B**NONE** No pulsing 0001_B**TXACT** Transmit activity 0010_B**RXACT** Receive activity 0100_B**COL** Collision 1000_B**RES** Reserved

Similar Registers

The following registers are identical to the Register **LED0L** defined above.

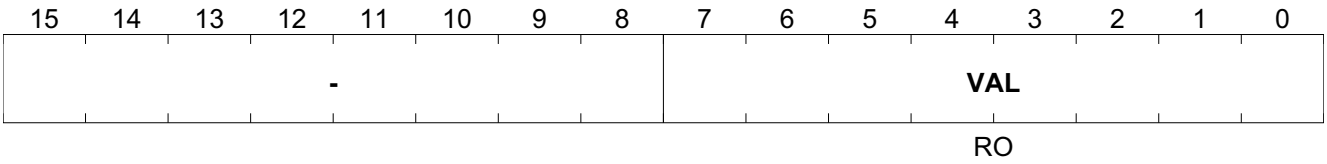
Table 36 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
LED1L	Configuration for LED Pin 1	$1F.01E5_H$	0000_H
LED2L	Configuration for LED Pin 2	$1F.01E7_H$	0000_H

High Byte of the EEE Link-Fail Counter

High Byte of the EEE Link-Fail Counter.

EEE_RXERR_LINK_FAIL_H	Offset	Reset Value
High Byte of the EEE Link-Fail Counter	$1F.01EA_H$	0000_H

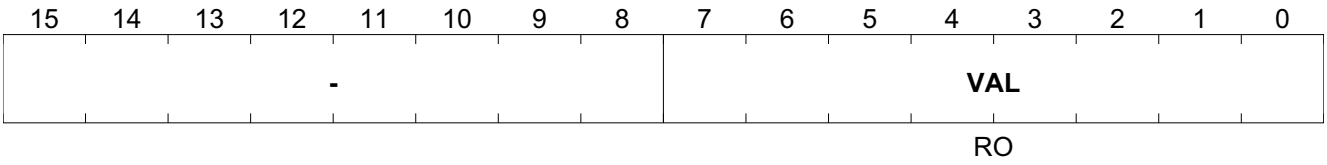


Field	Bits	Type	Description
VAL	7:0	RO	**VAL** High byte of the EEE_RXERR_LINK_FAIL counter. A read access to the low byte also clears the high byte of this counter.

Low Byte of the EEE Link-Fail Counter

Low Byte of the EEE Link-Fail Counter.

EEE_RXERR_LINK_FAIL_L	Offset	Reset Value
Low Byte of the EEE Link-Fail Counter	$1F.01EB_H$	0000_H

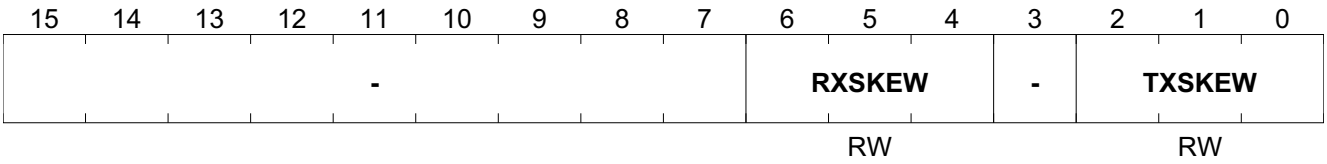


Field	Bits	Type	Description
VAL	7:0	RO	**VAL** Low byte of the EEE_RXERR_LINK_FAIL counter. A read access to this byte also clears the high byte of this counter.

MII2 Control

MII2 Control Register.

MII2CTRL	Offset	Reset Value
MII2 Control	$1F.01EC_H$	0000_H

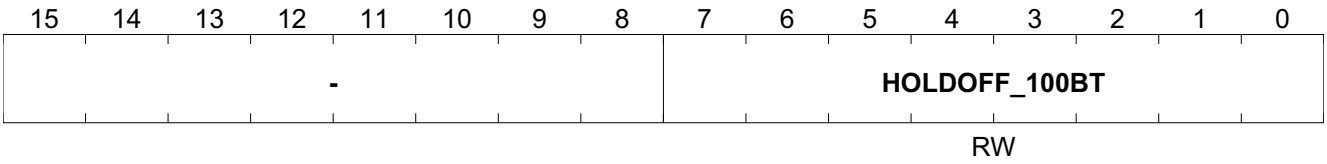


Field	Bits	Type	Description
RXSKEW	6:4	RW	**Receive Timing Skew (RGMII)** Defines the receive timing skew in the RGMII mode using the integrated delay generation on RX_CLK. Note that this register is subject to default reset values which depend on the soft pin-strappings. **Constants** 000_B **SKEW_0N0** 0.0 ns timing skew 001_B **SKEW_0N5** 0.5 ns timing skew 010_B **SKEW_1N0** 1.0 ns timing skew 011_B **SKEW_1N5** 1.5 ns timing skew 100_B **SKEW_2N0** 2.0 ns timing skew 101_B **SKEW_2N5** 2.5 ns timing skew 110_B **SKEW_3N0** 3.0 ns timing skew 111_B **SKEW_3N5** 3.5 ns timing skew
TXSKEW	2:0	RW	**Transmit Timing Skew (RGMII)** Defines the transmit timing skew in the RGMII mode using the integrated delay generation on TX_CLK. Note that this register is subject to default reset values which depend on the soft pin-strappings. **Constants** 000_B **SKEW_0N0** 0.0 ns timing skew 001_B **SKEW_0N5** 0.5 ns timing skew 010_B **SKEW_1N0** 1.0 ns timing skew 011_B **SKEW_1N5** 1.5 ns timing skew 100_B **SKEW_2N0** 2.0 ns timing skew 101_B **SKEW_2N5** 2.5 ns timing skew 110_B **SKEW_3N0** 3.0 ns timing skew 111_B **SKEW_3N5** 3.5 ns timing skew

Legacy LPI Configuration Register 0

Legacy LPI Configuration Register 0.

LEG_LPI_CFG0	Offset	Reset Value
Legacy LPI Configuration Register 0	**$1F.01ED_H$**	**0020_H**

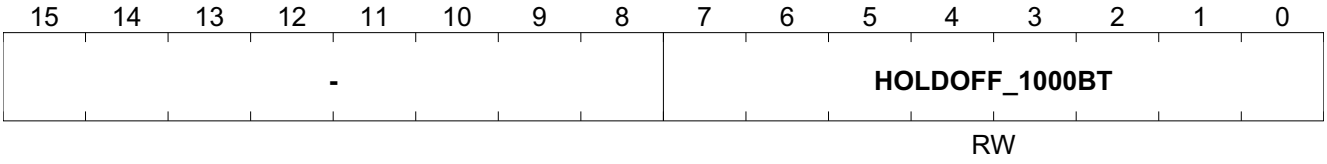


Field	Bits	Type	Description
HOLDOFF_100BT	7:0	RW	**Data Hold-Off Time 100BASE-T** Defines the time between releasing the LPI request on the MII until the first data is transmitted via MII for the 100BASE-T mode. The time is calculated as (HOLDOFF_100BT + 1) x 16 x 40 ns. **Constants** 00100000_B**DEFAULT** 21.12 us

Legacy LPI Configuration Register 1

Legacy LPI Configuration Register 1.

LEG_LPI_CFG1	Offset	Reset Value
Legacy LPI Configuration Register 1	**$1F.01EE_H$**	**0080_H**



Field	Bits	Type	Description
HOLDOFF_1000BT	7:0	RW	**Data Hold-Off Time 1000BASE-T** Defines the time between releasing the LPI request on the MII until the first data is transmitted via MII for the 1000BASE-T mode. The time is calculated as (HOLDOFF_1000BT + 1) x 16 x 8 ns. **Constants** 10000000_B**DEFAULT** 16.51 us

Wake-On-LAN Control Register

Wake-On-LAN Control Register.

WOLCTRL	Offset	Reset Value
Wake-On-LAN Control Register	$1F.0781_H$	0000_H

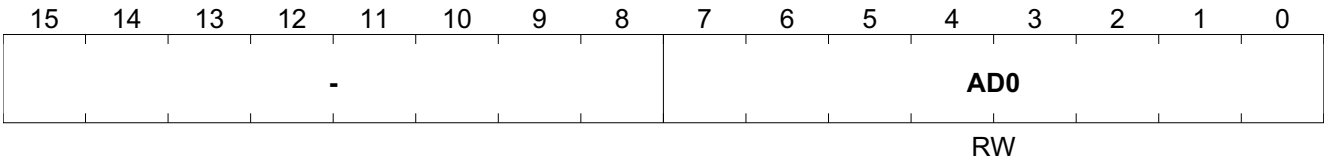
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-													SPWD_EN	RES	EN
													RW	RO	RW

Field	Bits	Type	Description
SPWD_EN	2	RW	**Secure-ON Password Enable** If enabled, checks for the Secure-ON password after the 16 MAC address repetitions. **Constants** 0_B **DISABLED** Secure-On password check is disabled 1_B **ENABLED** Secure-On password check is enabled
RES	1	RO	**Reserved** Must always be written to zero!
EN	0	RW	**Enables the Wake-On-LAN functionality** If Wake-On-LAN is enabled, the PHY scans for the configured magic packet and indicates its reception via the register bit ISTAT.WOL, and optionally also via interrupt. **Constants** 0_B **DISABLED** Wake-On-LAN functionality is disabled 1_B **ENABLED** Wake-On-LAN functionality is enabled

Wake-On-LAN Address Byte 0

Wake-On-LAN Address Byte 0.

WOLAD0	Offset	Reset Value
Wake-On-LAN Address Byte 0	$1F.0783_H$	0000_H



Field	Bits	Type	Description
AD0	7:0	RW	**Address Byte 0** Defines byte 0 of the WOL-designated MAC address to which the PHY is sensitive.

Similar Registers

The following registers are identical to the Register **WOLAD0** defined above.

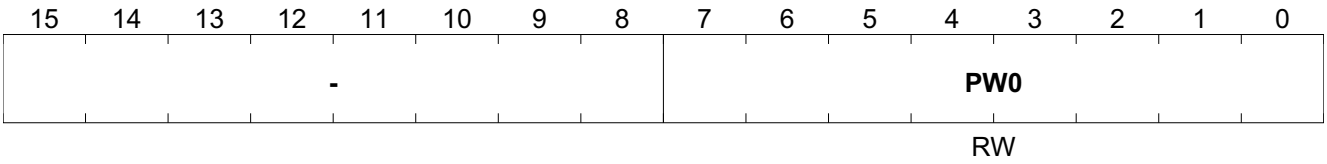
Table 37 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
WOLAD1	Wake-On-LAN Address Byte 1	$1F.0784_H$	0000_H
WOLAD2	Wake-On-LAN Address Byte 2	$1F.0785_H$	0000_H
WOLAD3	Wake-On-LAN Address Byte 3	$1F.0786_H$	0000_H
WOLAD4	Wake-On-LAN Address Byte 4	$1F.0787_H$	0000_H
WOLAD5	Wake-On-LAN Address Byte 5	$1F.0788_H$	0000_H

Wake-On-LAN SecureON Password Byte 0

Wake-On-LAN SecureON Password Byte 0.

WOLPW0	Offset	Reset Value
Wake-On-LAN SecureON Password Byte 0	**1F.0789$_H$**	**0000$_H$**



Field	Bits	Type	Description
PW0	7:0	RW	**SecureON Password Byte 0** Defines byte 0 of the WOL-designated SecureON password to which the PHY is sensitive.

Similar Registers

The following registers are identical to the Register **WOLPW0** defined above.

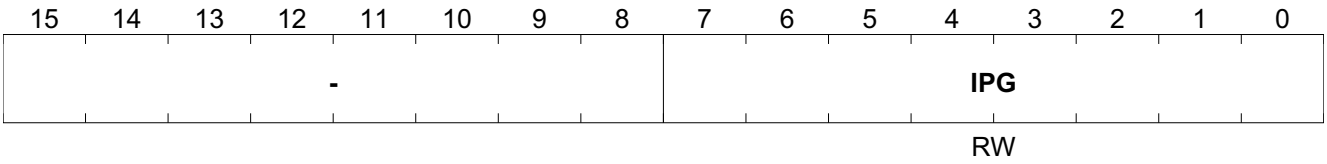
Table 38 Similar Registers

Register Short Name	Register Long Name	Offset Address	Reset Value
WOLPW1	Wake-On-LAN SecureON Password Byte 1	1F.078A$_H$	0000$_H$
WOLPW2	Wake-On-LAN SecureON Password Byte 2	1F.078B$_H$	0000$_H$
WOLPW3	Wake-On-LAN SecureON Password Byte 3	1F.078C$_H$	0000$_H$
WOLPW4	Wake-On-LAN SecureON Password Byte 4	1F.078D$_H$	0000$_H$
WOLPW5	Wake-On-LAN SecureON Password Byte 5	1F.078E$_H$	0000$_H$

Legacy LPI Configuration Register 2

Legacy LPI Configuration Register 2.

LEG_LPI_CFG2	Offset	Reset Value
Legacy LPI Configuration Register 2	$1F.0EB5_H$	$000E_H$

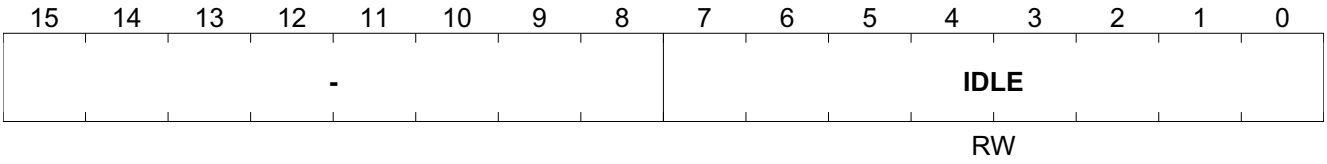


Field	Bits	Type	Description
IPG	7:0	RW	**IPG Storage Length** Defines the maximum IPG length to be stored in the LPI buffer. **Constants** 00001110_B**DEFAULT** Maximum IPG length is 14 bytes

Legacy LPI Configuration Register 3

Legacy LPI Configuration Register 3.

LEG_LPI_CFG3	Offset	Reset Value
Legacy LPI Configuration Register 3	$1F.0EB7_H$	0040_H



Field	Bits	Type	Description
IDLE	7:0	RW	**MII IDLE Time** Defines the MII IDLE time until TX LPI is indicated via MII in bytes. **Constants** 01000000_B**DEFAULT** MII IDLE time is 64 bytes

6 Electrical Characteristics

This chapter specifies the electrical characteristics of the the XWAY™ PHY11G.

6.1 Absolute Maximum Ratings

Table 39 shows the absolute maximum ratings for the XWAY™ PHY11G.

Attention: Stresses above the maximum values listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Attention: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

Table 39 Absolute Limit Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage temperature limits	T_{STG}	-55.0	–	125.0	°C	–
DC voltage limits on pad supply pins	V_{DDP}	-0.5	–	4.0	V	–
DC voltage limits on high supply pins	V_{DDH}	-0.5	–	4.0	V	–
DC voltage limits on DC/DC supply pins	V_{DDR}	-0.5	–	4.0	V	–
DC voltage limits on low supply pins	V_{DDL}	-0.5	–	1.6	V	–
DC voltage limits on core supply pins	V_{DDC}	-0.5	–	1.6	V	–
DC voltage limits on any digital pin[1)]	V_{DC}	-0.5	–	V_{DDP}+0.5	V	–
DC current limits on any digital input pin	$I_{DC,digital}$	-10.0	–	10.0	mA	–
DC current limits on DC/DC supply pin	$I_{DC,DC/DC}$	-400.0	–	400.0	mA	–
ESD robustness HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	–	–	2000.0	V	According to EIA/JESD22-A114-B
ESD robustness	$V_{ESD,CDM}$	–	–	500.0	V	According to ESD association standard DS5.3.1 - 1999

1) That is, any pin which is not a supply pin of one of the domains: V_{DDH}, V_{DDL}, V_{DDC}

6.2 Operating Range

Table 40 defines the limit values of voltages and temperature that can be applied while still guaranteeing proper operation of the XWAY™ PHY11G. As can be seen in the table, the device only needs one power supply, which can be arbitrarily chosen between 2.5 V and 3.3 V. When the optional DC/DC converter is not used, an additional low-voltage supply of 1.0 V is required.

Table 40 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient temperature under bias	T_A	-40.0	–	85.0	°C	–
Pad supply voltage	V_{DDP}	3.14	3.30	3.47	V	3.3 V supply
		2.37	2.50	2.62	V	2.5 V supply
High supply voltage	V_{DDH}	3.14	3.30	3.47	V	3.3 V supply
		2.37	2.50	2.62	V	2.5 V supply
DC/DC supply voltage	V_{DDR}	3.14	3.30	3.47	V	3.3 V supply
		2.37	2.50	2.62	V	2.5 V supply
Low supply voltage	V_{DDL}	0.95	1.00	1.05	V	–
Core supply voltage	V_{DDC}	0.95	1.00	1.05	V	–
Ground	V_{SS}	0.00	0.00	0.00	V	–

6.3 Recommended Operating Conditions

The recommended conditions for typical applications are to use nominal voltages of either 2.5 V or 3.3 V for V_{DDP}, V_{DDH} and V_{DDR}. Table 40 shows the supported operating ranges for these typical nominal voltage values. However, any other nominal voltage between 2.5 V and 3.3 V is also supported.

In order to optimize the overall power consumption of the XWAY™ PHY11G, a supply voltage of 2.5 V is recommended. The 3.3 V supply is intended to support legacy systems with only 3.3 V supply lines. At V_{DDH} = 2.5 V, it is not possible to fulfill the requirements according to the standard specified in IEEE 802.3, clause 14.3.1.2.1 [1], as the peak voltage requirement in 10BASE-T mode is slightly violated due to physical limitations. The timing characteristics specified from this point onwards are only valid for nominal voltages of either 2.5 V or 3.3 V.

6.4 Power-Up Sequence

It is recommended that the voltage domains are powered up simultaneously. It is essential that the chip-reset signal be asserted before or simultaneously with the voltage domains power-up, and that this signal remains asserted for as long as specified in the reset AC characteristics in Chapter 6.6.1.

6.5 DC Characteristics

The following sections describe the DC characteristics of the XWAY™ PHY11G external interfaces.

6.5.1 Digital Interfaces

This section describes the DC characteristics of the digital interfaces.

6.5.1.1 GPIO Interfaces

This chapter defines the DC characteristics of the GPIO Interface, consisting of the following interfaces:

- MDIO (MDC, MDIO)
- EEPROM/I^2C (SCL, SDA)
- Management interrupt (MDINT)
- Clock outputs (CLKOUT)
- Chip reset (RSTN)

The DC characteristics for V_{DDP} = 2.5 V are summarized in **Table 41**.

The DC characteristics for V_{DDP} = 3.3 V are summarized in **Table 42**.

Table 41 DC Characteristics of the GPIO Interfaces (VDDP = 2.5 V)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	1.8	–	V_{DDP}+0.5	V	
Input low voltage	V_{IL}	–	–	0.7	V	–
Output high voltage	V_{OH}	2.0	–	–	V	I_{OH} = -4 mA
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA

Table 42 DC Characteristics of the GPIO Interfaces (VDDP = 3.3 V)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	2.3	–	V_{DDP}+0.5	V	–
Input low voltage	V_{IL}	–	–	0.7	V	–
Output high voltage	V_{OH}	2.7	–	–	V	I_{OH} = -4 mA
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA

6.5.1.2 MII Receive Interface

This section defines the DC characteristics of the MII receive interface. Depending on the MII mode, this interface comprises the set of pins RX_CLK, RXD[3:0], RX_CTL, and MII_TXC. The DC characteristics summarized in **Table 43** are valid for V_{DDP} = 2.5 V and V_{DDP} = 3.3 V.

Table 43 DC Characteristics of the Receive MII Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output high voltage (R)GMII mode	V_{OH}	2.1	–	–	V	I_{OH} = -1 mA, V_{DDP} = 2.37 V
Output high voltage MII mode	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA, V_{DDP} = 3.13 V
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA

6.5.1.3 MII Transmit Interface

This section defines the DC characteristics of the MII transmit interface. Depending on the MII mode, this interface comprises the set of pins TX_CLK, TXD[3:0], TX_CTL. The DC characteristics summarized in **Table 44** are valid for V_{DDP} = 2.5 V and V_{DDP} = 3.3 V. Note that these pins are multiplexed with a SerDes interface, for example SGMII or 1000BASE-X, depending on the operational mode of the XWAY™ PHY11G. This chapter specifies the DC characteristics for the case that these pins operate in one of the non-SerDes modes.

Table 44 DC Characteristics of the Transmit MII Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	1.7	–	–	V	–
Input low voltage	V_{IL}	–	–	0.9	V	–

6.5.1.4 LED Interface

This section defines the DC characteristics of the LED interface, summarized in **Table 45**. Note that these characteristics only apply in LED-driving mode. During device startup, when the LED pins are serving the soft pin-strapping function, these characteristics do not necessarily apply.

Table 45 DC Characteristics of the Transmit LED Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	1.9	–	–	V	V_{DDH} = 2.5 V, I_{OH} = -15 mA
Output high voltage	V_{OH}	2.7	–	–	V	V_{DDH} = 3.3 V, I_{OH} = -15 mA
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 15 mA

6.5.1.5 JTAG Interface

The JTAG Interface comprises the set of pins TCK, TDI, TDO and TMS. It operates in the VDDH power domain. The DC characteristics for V_{DDH} = 2.5 V and V_{DDH} = 3.3 V are summarized in **Table 46** and **Table 47**, respectively.

Table 46 DC Characteristics of the JTAG Interface (VDDH = 2.5 V)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	1.8	–	V_{DDH}+0.5	V	–
Input low voltage	V_{IL}	–	–	0.7	V	–
Output high voltage	V_{OH}	2.1	–	–	V	I_{OH} = -4 mA
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA

Table 47 DC Characteristics of the JTAG Interface (VDDH = 3.3 V)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	2.3	–	V_{DDH}+0.5	V	–
Input low voltage	V_{IL}	–	–	0.7	V	–
Output high voltage	V_{OH}	2.7	–	–	V	I_{OH} = -4 mA
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA

6.5.2 Twisted-Pair Interface

The TPI conforms to the 10BASE-T, 100BASE-TX and 1000BASE-T specifications described in IEEE802.3 **[1]**, as well as ANSI X3.263-1995 **[4]**.

6.5.3 SGMII Interface

Since the SGMII interface implementation on the XWAY™ PHY11G is purely AC coupled, there are no DC characteristics to be specified. Instead, **Chapter 6.8.6** specifies the AC-coupling external circuitry with an option to generate the common-mode offset voltage required for DC-coupled operation (compliant with **[13]**) with the SGMII link partner. The AC characteristics which apply in SGMII mode are specified in **Chapter 6.6.9**.

6.5.4 1000BASE-X Interface

Since the 1000BASE-X interface implementation on the XWAY™ PHY11G is purely AC coupled, there are no DC characteristics to be specified. Instead, **Chapter 6.8.7** specifies the AC-coupling external circuitry. The AC characteristics which apply in 1000BASE-X mode are specified in **Chapter 6.6.10**.

6.6 AC Characteristics

The following sections describe the AC characteristics of the external interfaces.

6.6.1 Reset

The XWAY™ PHY11G supports an asynchronous hardware reset, RSTN. The timing requirements of the XWAY™ PHY11G related to the RSTN pin are listed in **Table 48**. The timing requirements refer to the signal sequence waveforms shown in **Figure 43**[1].

After the power supply settling time, all primary input signals to the XWAY™ PHY11G must be defined. In particular, the device reset RSTN must be held for a time t_{reset}. As shown in **Figure 43**, the reference clock (either generated internally using an attached crystal, or applied externally from an external crystal oscillator) should be available at the latest before the reset is released. This setup time is denoted as t_{ref}. The maximum slope of the rising edge of the reset signal is constrained by the rise time t_r. In case the integrated DC/DC switching regulator is used to self-supply the low-voltage domains, the reference clock must not be interrupted at all, unless when powering down the system.

The XWAY™ PHY11G only starts booting its integrated device controller after the clock is running and the reset signal has been released. After locking the PLL to the reference clock, the device does soft pin-strapping as well as an EEPROM scan (only if an EEPROM is connected). Since the default values inside the MDIO address space are modified by both procedures, the first MDIO access is only allowed after a time t_{MDIO}.

Once the device is powered up, the clock output is continuously driven, irrespective of the status of the reset pin.

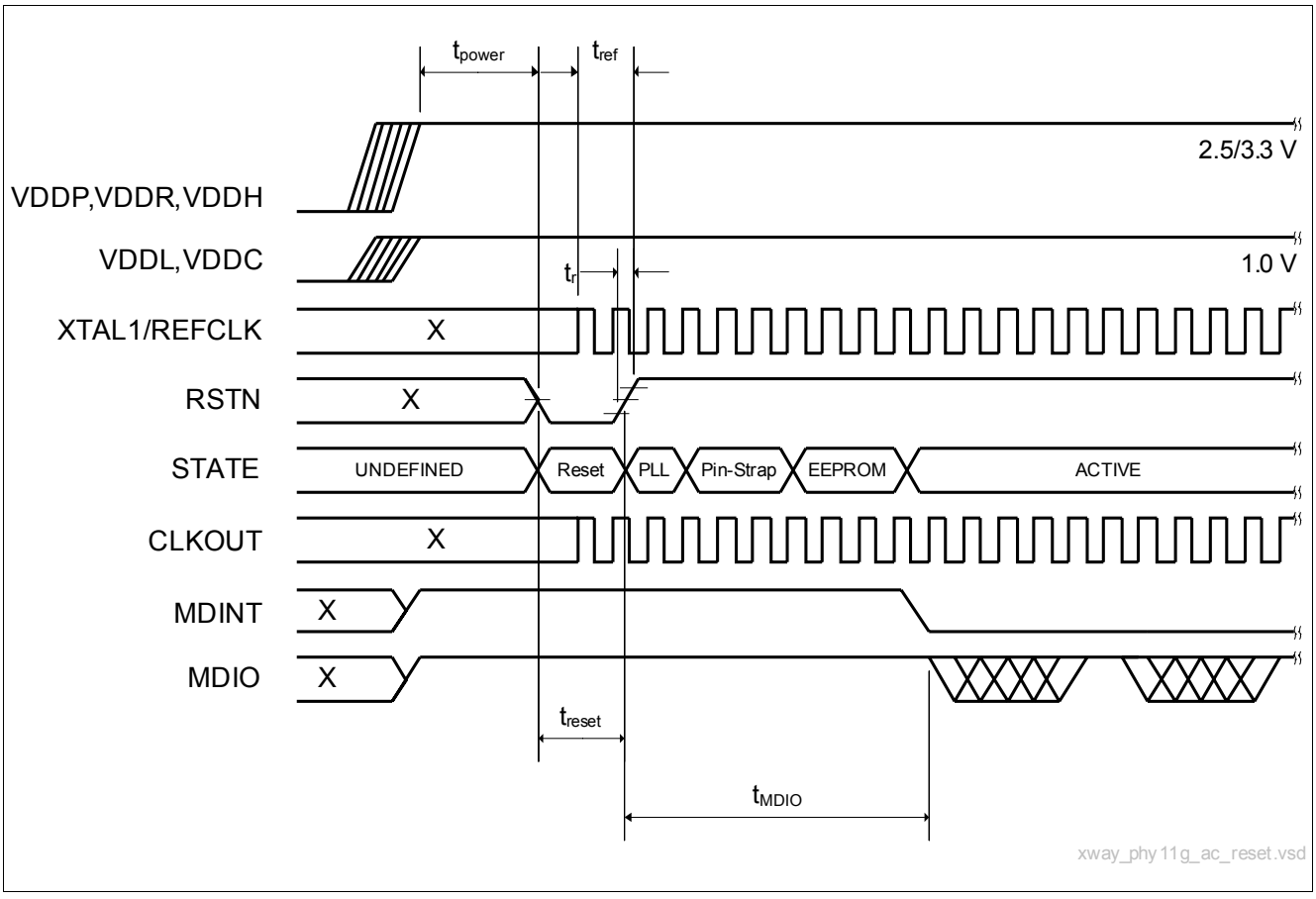


Figure 43 Timing Diagram for the XWAY™ PHY11G Reset Sequence

1) **Figure 43** shows an active-low MDINT signal. However, MDINT can be configured to either active-low or active-high, depending on the external configuration. Refer to **Chapter 3.4.3.3 - MDIO Interrupt** for more information.

Table 48 AC Characteristics of the RSTN Pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply settling time	t_{power}	–	–	50.0	ms	–
Reset time	t_{reset}	100.0	–	–	ns	–
Rise time	t_R	–	–	10.0	ns	–
First MDIO access after reset release	t_{MDIO}	300.0	–	–	ms	–

6.6.2 Power Supply

Table 49 lists the AC characteristics of the power supplies.

Table 49 AC Characteristics of the Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply ripple on VDDL	R_{VDDL}	–	–	30.0	mV	Peak value
Power supply ripple on VDDC	R_{VDDC}	–	–	30.0	mV	Peak value
Power supply ripple on VDDP	R_{VDDP}	–	–	100.0	mV	Peak value
Power supply ripple on VDDH	R_{VDDH}	–	–	50.0	mV	Peak value
Power supply ripple on VDDR	R_{VDDR}	–	–	100.0	mV	Peak value

6.6.3 Input Clock

Table 50 lists the input clock requirements for the case when no crystal is used, that is, when an external reference clock is applied at the XTAL1 pin of the XWAY™ PHY11G. The table includes nominal frequency, frequency deviation, duty cycle and signal characteristics. If a crystal is used with the integrated oscillator to generate the reference clock, the clock requirements stated here are implicitly met as long as the specification for the crystal outlined in Chapter 6.8.1 is satisfied.

Table 50 AC Characteristics of Input Clock on XTAL1 Pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency with 25 MHz input[1)]	f_{clk25}	–	25.0	–	MHz	–
Frequency with 125 MHz input[1)]	f_{clk125}	–	125.0	–	MHz	–
Frequency deviation		-50.0	–	+50.0	ppm	–
Duty cycle		40.0	50.0	60.0	%	–
Rise/fall times		–	–	1.0	ns	–

1) More details on how to select the output frequency are given in Chapter 3.4.1

6.6.4 Output Clock

Table 51 lists the output clock requirements for the CLKOUT pin on the XWAY™ PHY11G, including nominal frequency, frequency deviation, duty cycle and signal characteristics.

Table 51 AC Characteristics of Output Clock on CLKOUT Pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency at 25 MHz	f_{clk25}	–	25.0	–	MHz	–
Frequency at 125 MHz	f_{clk125}	–	125.0	–	MHz	–
Frequency deviation		-50.0	–	+50.0	ppm	–
Duty cycle		49.0	50.0	51.0	%	–
Rise/fall-times		–	–	1.0	ns	–

6.6.5 MDIO Interface

Figure 44 shows a timing diagram of the MDIO interface for a clock cycle in the read, write and turn-around modes. The timing measurements are annotated, and their absolute values defined in Table 52.

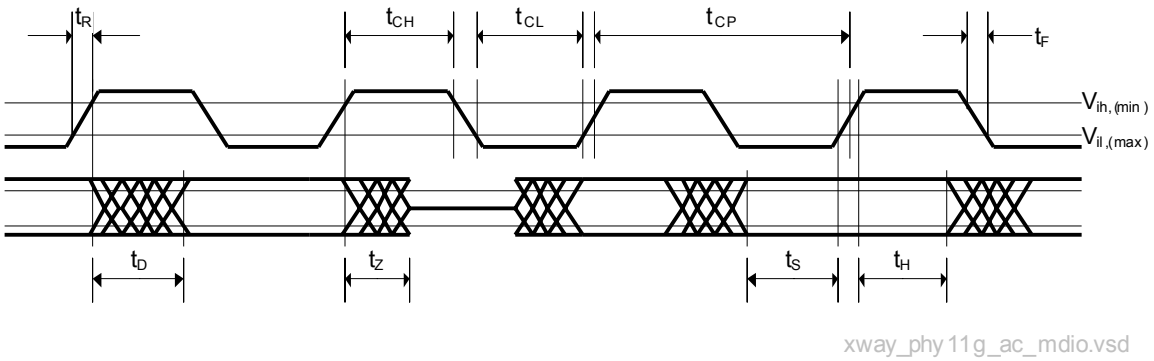


Figure 44 Timing Diagram for the MDIO Interface

Table 52 AC Characteristics of the MDIO Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC high time	t_{CH}	10.0	–	–	ns	Given timings are all subject to the MDC at the pin of the XWAY™ PHY11G.
MDC low time	t_{CL}	10.0	–	–	ns	
MDC clock period	t_{CP}	40.0	–	–	ns	
MDC clock frequency	t_{CP}	–	–	25.0	MHz	
MDC rise time	t_R	–	–	5.0	ns	
MDC fall time	t_F	–	–	5.0	ns	
MDIO read delay	t_D	0.0	–	10.0	ns	
MDIO high-Ohmic (Z) delay	t_Z	0.0	–	10.0	ns	
MDIO setup time	t_S	4.0	–	–	ns	
MDIO hold time	t_H	4.0	–	–	ns	

6.6.6 RMII Interface

This section describes the AC characteristics of the RMII interface on the XWAY™ PHY11G. This interface conforms to the RMII specification as defined by the RMII Consortium in **[11]**.

Figure 45 shows the timing diagram of the transmit MII interface on the XWAY™ PHY11G. It is referred to by **Table 53**, which specifies the timing requirements at 10 Mbit/s and 100 Mbit/s, respectively.

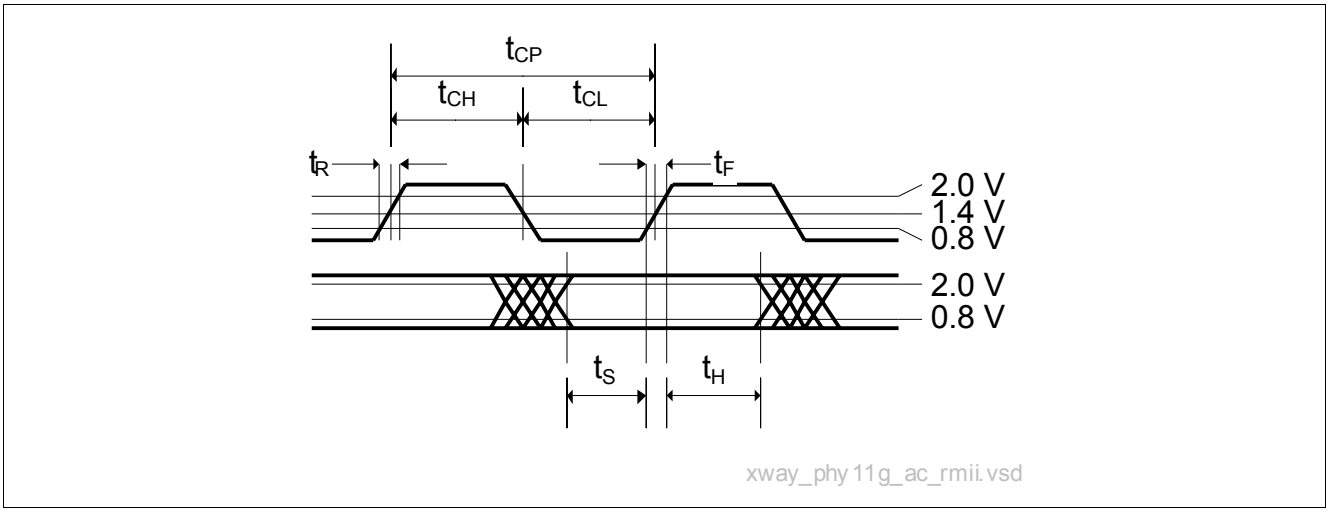


Figure 45 Transmit Timing Diagram of the RMII

Table 53 Timing Characteristics of the RMII at 10/100 Mbit/s

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference clock period	t_{CP}	19.999	20.00	20.001	ns	±50 ppm
Reference clock frequency	F_{REF}	50.00 - 50 ppm	50.00	50.0 +50 ppm	MHz	±50 ppm
Reference clock high time	t_{CH}	7.00	10.00	13.00	ns	–
Reference clock low time	t_{CL}	7.00	10.00	13.00	ns	–
Reference clock duty cycle	$D = t_{CH}/t_{CL}$	35.00	50.00	65.00	%	–
Rise time (clock and data)	t_R	1.00	–	5.00	ns	–
Fall time (clock and data)	t_F	1.00	–	5.00	ns	–
Setup time subject to ↑ REFCLK	t_S	4.00	–	–	ns	–
Hold time subject to ↑ REFCLK	t_H	2.00	–	–	ns	–

6.6.7 RGMII Interface

This section describes the AC characteristics of the RGMII interface on the XWAY™ PHY11G. Unless no HSTL voltages are supported, this interface conforms to the RGMII specification v1.3 and v2.0, as defined in [9] and [10] respectively. The RGMII interface can operate at speeds of 10 Mbit/s, 100 Mbit/s and 1000 Mbit/s.

6.6.7.1 Transmit Timing Characteristics

Figure 46 shows the timing diagram of the transmit RGMII interface on the XWAY™ PHY11G. It is referred to by Table 54, which specifies the timing requirements. Note that the setup and hold times are subject to the internal version of the TX_CLK, which is the external clock delayed by the integrated delay. The delay is adjustable in steps of 0.5 ns via MDIO. If the integrated delay is not used, for example because it is implemented externally by PCB wire delays, it must be set to zero, in which case all the timings are related directly to the TX_CLK on the pin.

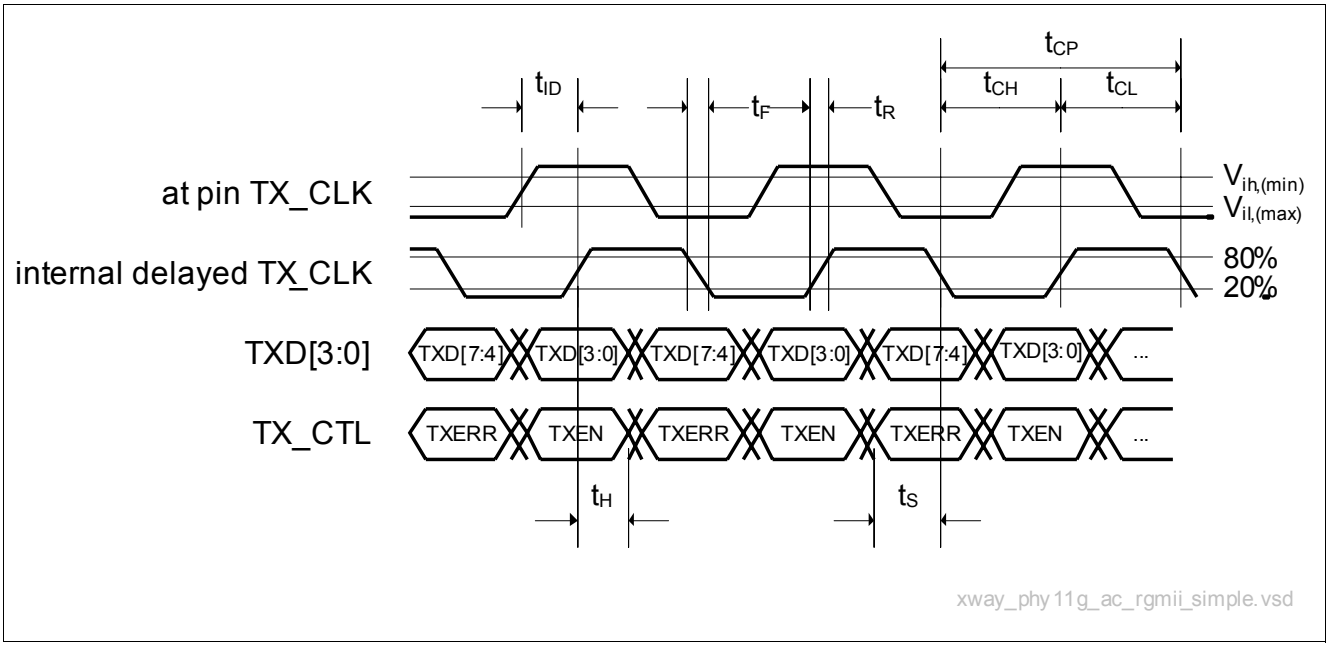


Figure 46 Transmit Timing Diagram of the RGMII

Table 54 Transmit Timing Characteristics of the RGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transmit clock frequency (TX_CLK)	f_{TX_CLK}	-50 ppm	125.0	+ 50 ppm	MHz	For 1000 Mbit/s speed
			25.0		MHz	For 100 Mbit/s speed
			2.5		MHz	For 10 Mbit/s speed
Transmit clock period (TX_CLK)	t_{CP}	7.2	8.0	8.8	ns	For 1000 Mbit/s speed
		36.0	40.0	44.0	ns	For 100 Mbit/s speed
		360.0	400.0	440.0	ns	For 10 Mbit/s speed
Duty cycle	t_H/t_{CP}, t_L/t_{CP}	45.0	50.0	55.0	%	Speed-independent
Transmit clock rise time (TX_CLK)	t_R	–	–	750.0	ps	20%→80%
Transmit clock fall time (TX_CLK)	t_F	–	–	750.0	ps	80%→20%
Setup time to ↑↓ internal TX_CLK	t_S	1.0	–	–	ns	

Table 54 Transmit Timing Characteristics of the RGMII (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Hold time to ↑↓ internal TX_CLK	t_H	1.0	–	–	ns	
Integrated transmit clock delay	t_{ID}	0.0	k*0.5	3.5	ns	Adjustable via MDIO register

6.6.7.2 Receive Timing Characteristics

Figure 47 shows the timing diagram of the receive RGMII interface on the XWAY™ PHY11G. It is referred to by **Table 55**, which specifies the timing requirements. Note that the clock-to-data skew time is subject to the internal version of the RX_CLK. The external clock on the pin is delayed by the integrated delay, which is adjustable in steps of 0.5 ns via MDIO. If the integrated delay is not used, for example because it is implemented externally by PCB wire delays, it must be set to zero, in which case all the timings are related directly to the RX_CLK on the pin.

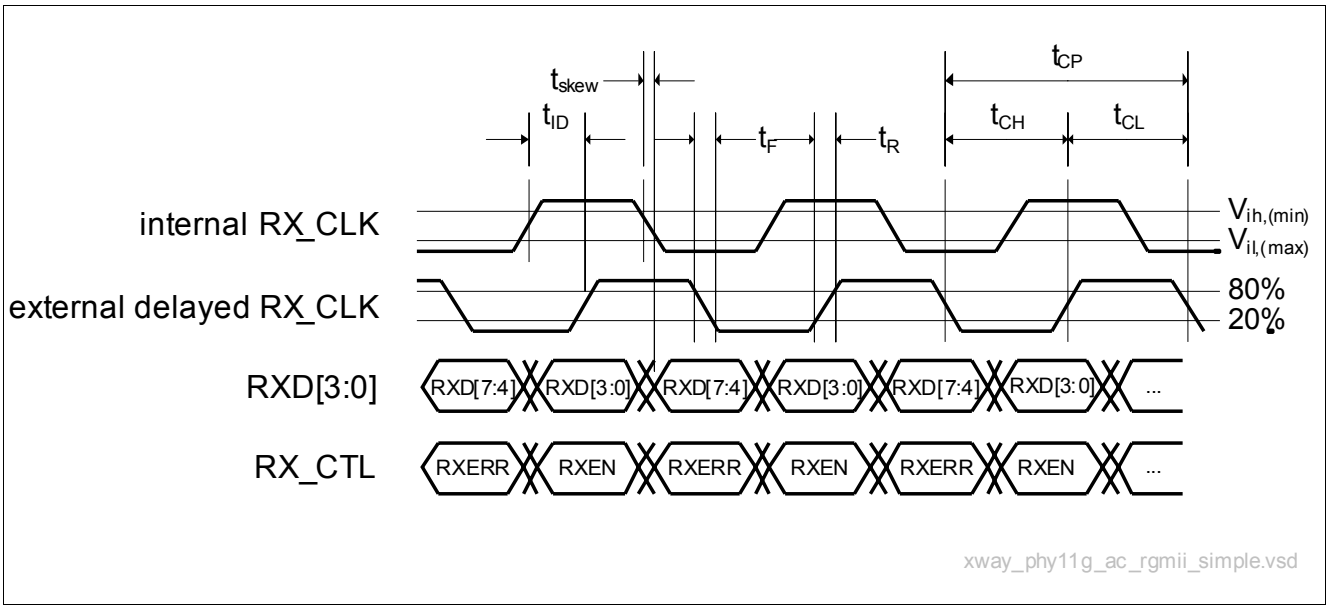


Figure 47 Receive Timing Diagram of the RGMII

Table 55 Receive Timing Characteristics of the RGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive clock frequency (RX_CLK)	f_{RX_CLK}	-50 ppm	125.0	+ 50 ppm	MHz	For 1000 Mbit/s speed
			25.0		MHz	For 100 Mbit/s speed
			2.5		MHz	For 10 Mbit/s speed
Receive clock period (TX_CLK)	t_{CP}	7.5	8.0	8.5	ns	For 1000 Mbit/s speed
		39.5	40.0	40.5	ns	For 100 Mbit/s speed
		399.5	400.0	400.5	ns	For 10 Mbit/s speed
Duty cycle	t_H/t_{CP}, t_L/t_{CP}	45.0	50.0	55.0	%	Speed-independent
Receive clock rise time (TX_CLK)	t_R	–	–	750.0	ps	20% → 80%
Receive clock fall time (TX_CLK)	t_F	–	–	750.0	ps	80% → 20%

Table 55 Receive Timing Characteristics of the RGMII (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock-to-data skew at RX	t_{skew}	-0.5	0.0	0.5	ns	
Integrated receive clock delay	t_{ID}	0.0	k*0.5	3.5	ns	Adjustable via MDIO register

6.6.8 RTBI Interface

This section describes the AC characteristics of the RTBI interface at the XWAY™ PHY11G. Unless no HSTL voltages are supported, this interface conforms to the RGMII specification v1.3 and v2.0, as defined in [9] and [10] respectively. The RTBI interface can operate at 1000 Mbit/s.

6.6.8.1 Transmit Timing Characteristics

Figure 48 shows the timing diagram of the transmit RTBI interface on the XWAY™ PHY11G. It is referred to by Table 56, which specifies the timing requirements. Note that the setup and hold times are subject to the internal version of the TX_CLK, which is the external clock delayed by the integrated delay. This delay is adjustable in steps of 0.5 ns via MDIO. If the integrated delay is not used, for example because it is implemented externally by PCB wire delays, it must be set to zero, in which case all the timings are related directly to the TX_CLK on the pin.

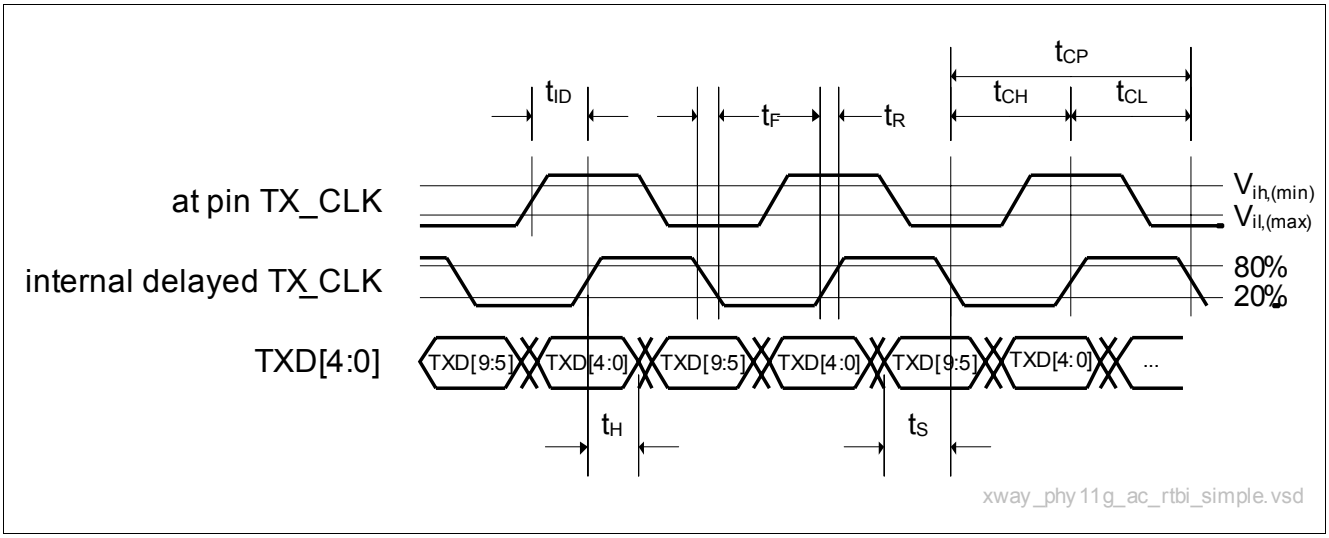


Figure 48 Transmit Timing Diagram of the RTBI

Table 56 Transmit Timing Characteristics of the RTBI

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transmit clock frequency (TX_CLK)	f_{TX_CLK}	-50 ppm	125.0	+ 50 ppm	MHz	
Transmit clock period (TX_CLK)	t_{CP}	7.2	8.0	8.8	ns	
Transmit clock high time (TX_CLK)	t_H	3.6	4.0	4.4	ns	
Transmit clock low time (TX_CLK)	t_L	3.6	4.0	4.4	ns	
Transmit clock rise time (TX_CLK)	t_R	–	–	750.0	ps	20%→80%
Transmit clock fall time (TX_CLK)	t_F	–	–	750.0	ps	80%→20%
Setup time to ↑↓ internal TX_CLK	t_S	1.0	–	–	ns	
Hold time to ↑↓ internal TX_CLK	t_H	1.0	–	–	ns	
Integrated transmit clock delay	t_{ID}	0.0	k*0.5	3.5	ns	Adjustable via MDIO register

6.6.8.2 Receive Timing Characteristics

Figure 49 shows the timing diagram of the receive RTBI interface on the XWAY™ PHY11G. It is referred to by Table 57, which specifies the timing requirements. Note that the clock-to-data skew time is subject to the internal version of the RX_CLK. The external clock on the pin is delayed by the integrated delay, which is adjustable in steps of 0.5 ns via MDIO. If the integrated delay is not used, for example because it is implemented externally by PCB wire delays, it must be set to zero, in which case all the timings are related directly to the RX_CLK on the pin.

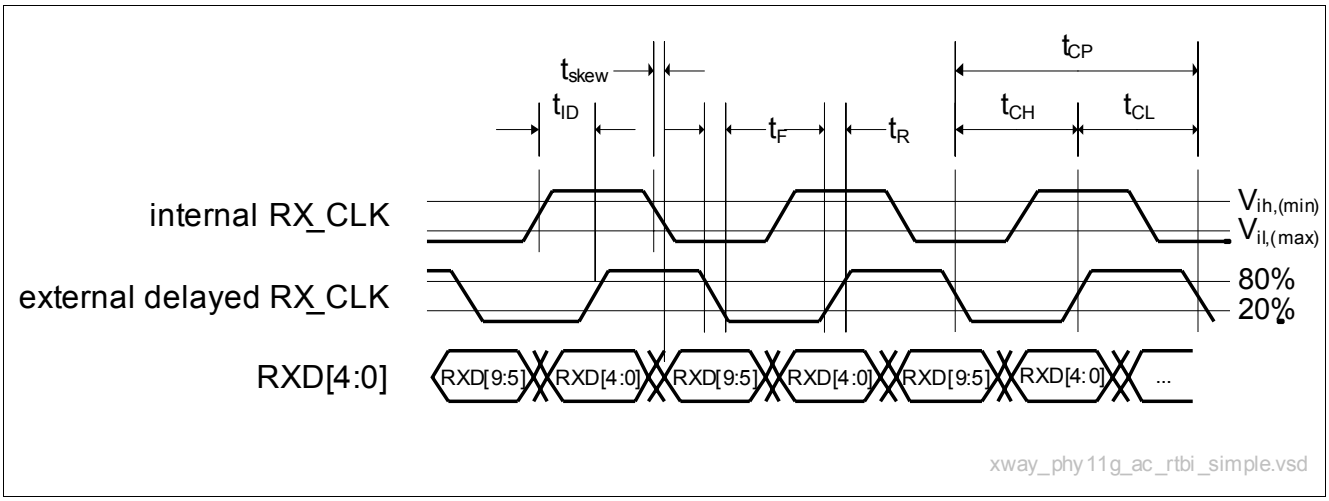


Figure 49 Receive Timing Diagram of the RTBI

Table 57 Receive Timing Characteristics of the RTBI

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive clock frequency (RX_CLK)	f_{RX_CLK}	-50 ppm	125.0	+ 50 ppm	MHz	
Receive clock period (RX_CLK)	t_{CP}	7.5	8.0	8.5	ns	
Receive clock high time (RX_CLK)	t_H	3.6	4.0	4.4	ns	
Receive clock low time (RX_CLK)	t_L	3.6	4.0	4.4	ns	
Receive clock rise time (RX_CLK)	t_R	–	–	750.0	ps	20%→80%
Receive clock fall time (RX_CLK)	t_F	–	–	750.0	ps	80%→20%
Clock-to-data skew at RX	t_{Skew}	-0.5	0.0	0.5	ns	
Integrated receive clock delay	t_{ID}	0.0	k*0.5	3.5	ns	Adjustable via MDIO register

6.6.9 SGMII Interface

This section describes the AC characteristics of the SGMII Interface on the XWAY™ PHY11G. This interface conforms to the SGMII specification v1.7, as defined in **[13]**. The SGMII interface can operate at 1.25 Gbaud. The net data-rate is 1000 Mbit/s. Using repetition modes, 10 Mbit/s and 100 Mbit/s are supported.

Also note that **Chapter 6.8.6** specifies the external circuitry.

6.6.9.1 Transmit Timing Characteristics

Figure 50 shows the timing diagram of the transmit SGMII interface at the XWAY™ PHY11G. It is referred to by **Table 58**, which specifies the timing requirements.

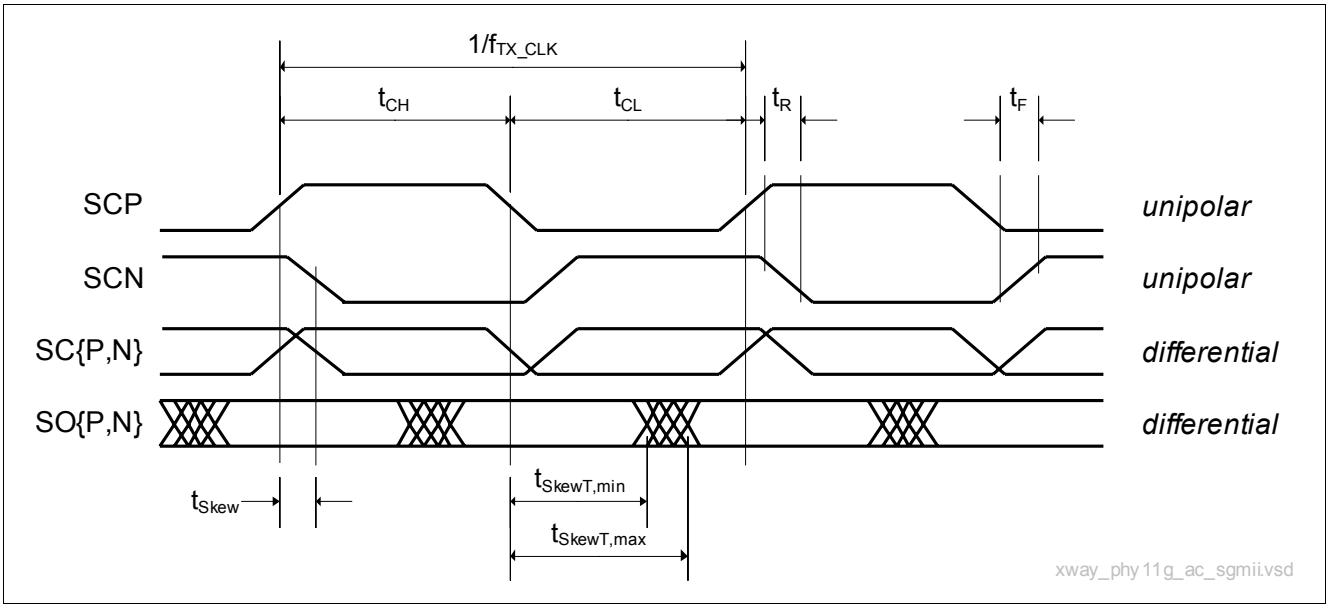


Figure 50 Transmit Timing Diagram of the SGMII

Table 58 Transmit Timing Characteristics of the SGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transmit clock frequency	f_{TX_CLK}	-50 ppm	625.0	+ 50 ppm	MHz	
Transmit clock duty cycle	$D_{CP} = t_{CH}/t_{CL}$	48	50	52	%	
Transmit rise time	t_R	100	–	200	ps	20%→80%
Transmit fall time	t_F	100	–	200	ps	80%→20%
Clock-to-data skew at TX	t_{SkewT}	250	–	550	ps	
Output timing jitter	J_{TX}	–	–	240	ps	Peak-peak[1)]
Time skew between pairs	t_{Skew}	–	–	20	ps	
Output differential voltage	V_{OD}	150	–	400	mV	Peak-amplitude
Output voltage ringing	V_{ring}	–	–	10	%	
Output impedance (single-ended)	R_O	40	–	60	Ω	
Output impedance (differential)	R_O	80	–	120	Ω	
Delta output impedance	dR_O	–	–	10	%	

1) Assuming BER = 1e-12 and tracking BW = 1 MHz

6.6.9.2 Receive Timing Characteristics

Figure 51 shows the timing diagram of the receive SGMII interface on the XWAY™ PHY11G. It is referred to by Table 59, which specifies the timing requirements. Note that the integrated SGMII operates using a CDR (Clock and Data Recovery), and therefore does not require the 625 MHz differential receive clock. Consequently, there are no timing requirement related to this clock.

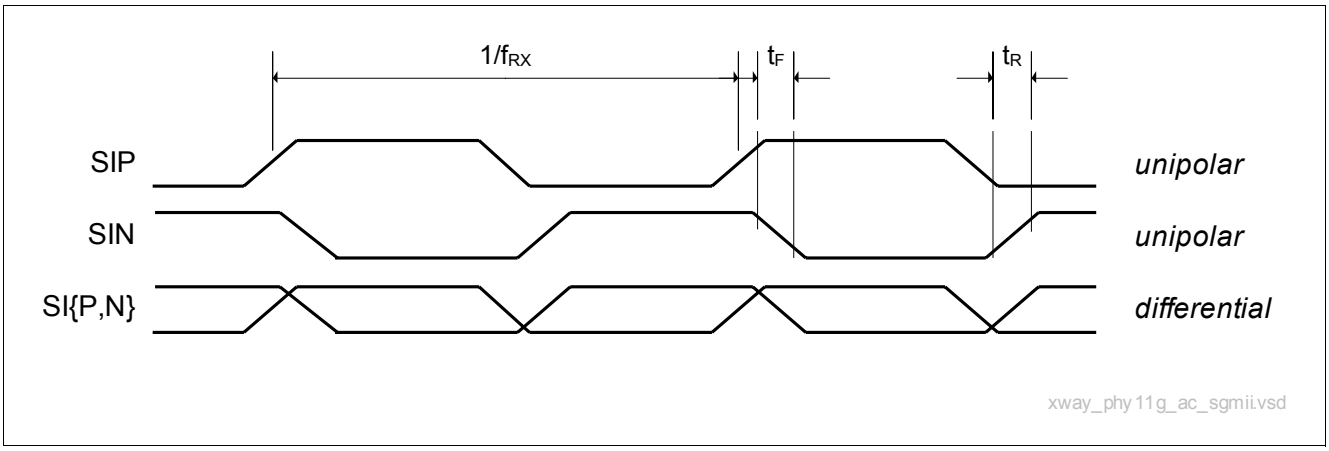


Figure 51 Receive Timing Diagram of the SGMII

Table 59 Receive Timing Characteristics of the SGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive data rate	f_{RX}	-50 ppm	1250.0	+ 50 ppm	Mbit/s	
Receive data jitter tolerance	J_{RX}	–	–	500	ps	
Receive signal rise time	t_R	–	–	300	ps	20%→80%
Receive signal fall time	t_F	–	–	300	ps	80%→20%
Input differential voltage	V_{ID}	50	–	500	mV	Peak-amplitude
Input impedance (single-ended)	R_I	40	–	60	Ω	
Input impedance (differential)	R_I	80	–	120	Ω	

6.6.10 1000BASE-X Interface

This section describes t he AC characteristic s of the 1000BASE-X in terface on the XW AY™ PHY11G. This interface conforms to the specifications given in IEEE802.3, clause 36 (see **[1]**). The 1000BASE-X interface can operate at 1.25 Gbaud. The net data-rate is 1000 Mbit/s.

Also note that **Chapter 6.8.7** describes the external circuitry.

6.6.10.1 Transmit Timing Characteristics

Figure 52 shows the timing diagram of the transmit 1000BASE-X interface on the XWAY™ PHY11G. It is referred to by **Table 60**, which specifies the timing requirements.

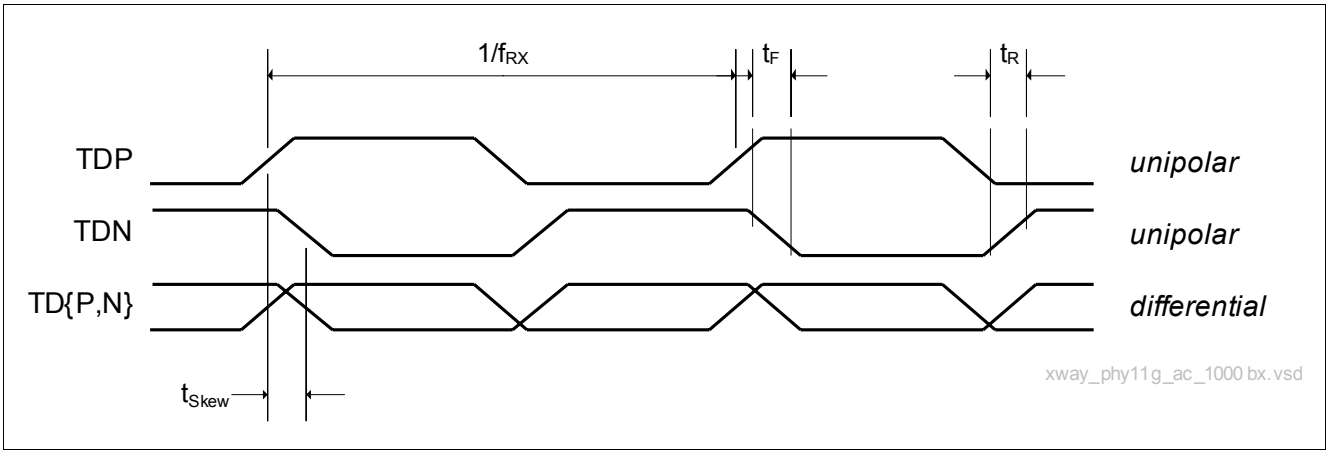


Figure 52 Transmit Timing Diagram of the 1000BASE-X Interface

Table 60 Transmit Timing Characteristics of the 1000BASE-X Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transmit data rate	f_{RX}	-50 ppm	1250.0	+ 50 ppm	Mbit/s	
Transmit rise time	t_R	100	–	200	ps	20%→80%
Transmit fall time	t_F	100	–	200	ps	80%→20%
Output data jitter	J_{TX}	–	–	240	ps	Peak-peak[1)]
Time skew between pairs	t_{Skew}	–	–	20	ps	
Output differential voltage	V_{OD}	150	–	400	mV	Peak-amplitude
Output voltage ringing	V_{ring}	–	–	10	%	
Output impedance (single-ended)	R_O	40	–	60	Ω	
Output impedance (differential)	R_O	80	–	120	Ω	
Delta output impedance	dR_O	–	–	10	%	

1) Assuming BER = 1e-12 and tracking BW = 1 MHz

6.6.10.2 Receive Timing Characteristics

Figure 53 shows the timing diagram of the receive 1000BASE-X interface on the XWAY™ PHY11G. It is referred to by **Table 61**, which specifies the timing requirements.

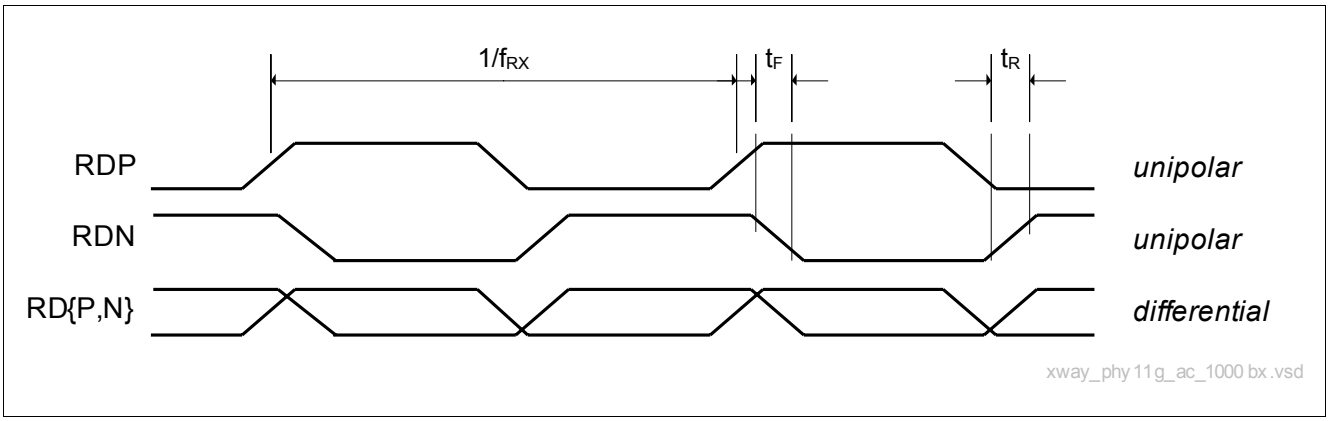


Figure 53 Receive Timing Diagram of the 1000BASE-X

Table 61 Receive Timing Characteristics of the 1000BASE-X

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive data rate	f_{RX}	-50 ppm	1250.0	+ 50 ppm	Mbit/s	
Receive data jitter tolerance	J_{RX}	–	–	500	ps	
Receive signal rise time	t_R	–	–	300	ps	20%→80%
Receive signal fall time	t_F	–	–	300	ps	80%→20%
Input differential voltage	V_{ID}	50	–	500	mV	Peak-amplitude
Input impedance (single-ended)	R_I	40	–	60	Ω	
Input impedance (differential)	R_I	80	–	120	Ω	

6.6.11 Twisted-Pair Interface

The AC characteristics for the TPI on pins VxpA, VxnA, VxpB, VxnB, VxpC, VxnC, VxpD and VxnD are specified in **[1]** and **[4]**. Since the XWAY™ PHY11G conforms to these standards, the values and limits specified there apply to this specification as well.

6.7 Isolation Requirements

The XWAY™ PHY11G meets the isolation requirements specified in **[1]**, clause 14.7.2.4 and clause 40.6.1.1, as well as in **[4]** clause 8.4.

6.8 External Circuitry

This chapter specifies the component characteristics of the external circuitry connected to the XWAY™ PHY11G.

6.8.1 Crystal

In case no external reference clock (as described in **Chapter 6.6.3**) is available, the device must generate its own self-contained clock using an external crystal (parallel resonator) connected to XTAL1 and XTAL2. The internal crystal oscillator internally generates a reference clock which conforms to the specification defined in **Chapter 6.6.3**, as long as the component specification outlined in this section is satisfied. In order to specify the crystal, an equivalent circuit is shown in **Figure 54**. This circuit is referred to by the component characteristics specification given in **Table 62**.

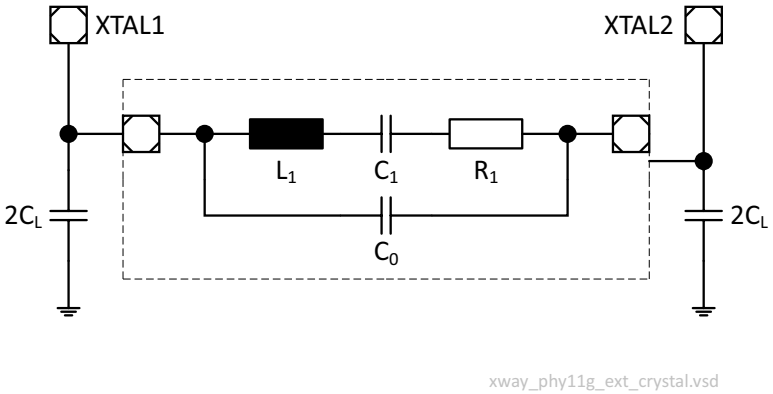


Figure 54 Equivalent Circuit for Crystal Specification

Table 62 Electrical Characteristics for Supported Crystals

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Main resonant frequency	f_{Res}		25		MHz	
Total frequency stability[1)]		-50	0	+50	ppm	
Temperature range	T	-40		+85	°C	
Series capacitance	C_1		15	30	fF	
ESR	R_1		30	70	Ω	
Shunt capacitance	C_0			7	pF	
Load capacitance	$2C_L$		33.0		pF	
Drive level	P_{drive}	0.1			mW	

1) Refers to the sum of all effects, e.g. general tolerances, aging, temperature dependency

6.8.2 LED

This section specifies the electrical characteristics of the LEDs which are supported. Note that the requirements specified here are given to guarantee proper operation of the pin-strapping (Chapter 3.4.1), which shares the LED pins. Nevertheless, the requirements are selected to fit almost every LED available on the target market.

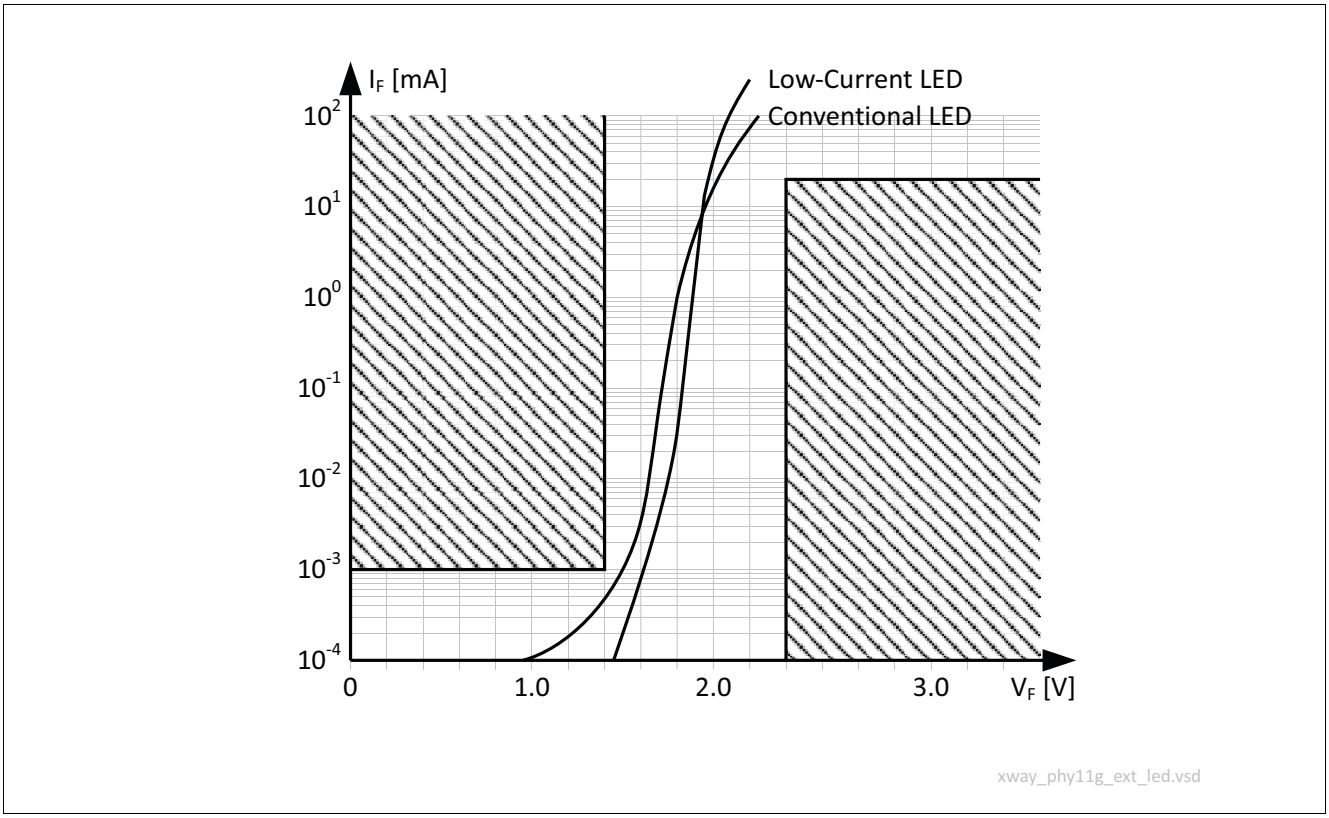


Figure 55 Tolerance Graph for the Forward Current Versus Voltage of the Supported LEDs

Note that LED devices also significantly contribute to the system power consumption. A conventional LED has an operating point of $V_F \approx 2.0$ V and $I_F \approx 20.0$ mA. This results in a power consumption of 40 mW per LED. Three LEDs would consume up to 120 mW, which is already as high as 30% of the maximum power consumption of the entire XWAY™ PHY11G device. Using low-current LEDs would improve this figure to 12 mW, that is, only 3% of the device power consumption. Figure 55 shows a tderance graph with typical U-I characteristics of the supported LED types. The tolerance values referred to by this figure are listed in Table 63.

Table 63 Electrical Characteristics for Supported LEDs

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature range	T	-40.0		+85.0	°C	
Forward current	I_F			1.0	µA	$V_F \leq 1.4$ V
Forward current (low-current LEDs)[1)]	I_F		2.0		mA	$1.4 \text{ V} \leq V_F \leq 2.5$ V
Forward current (conventional LEDs)	I_F		20.0		mA	$1.4 \text{ V} \leq V_F \leq 2.5$ V
Forward voltage (nominal)	V_F	1.6	1.9	2.2	V	Nominal forward voltage, where LED is emitting light

1) Low-current LEDs are preferred in order to reduce the system power consumption.

6.8.3 Transformer (Magnetics)

This section specifies the electrical characteristics of the transformer[1] devices that are supported. The specifications listed here guarantee proper operation according to IEEE 802.3 [1]. A typical Gigabit Ethernet capable transformer device is depicted in Figure 56. Table 64 lists the characteristics of the supported transformer devices. Note that these characteristics represent the bare minimum for achieving standard performance. Since the transformer significantly impacts the link performance, it is possible to increase the loop reach by selecting transformers with improved parameters.

Note that the IC-side center taps of the transformer must not be connected and should be left open. In particular, transformer types which short all IC-side center taps together must not be used.

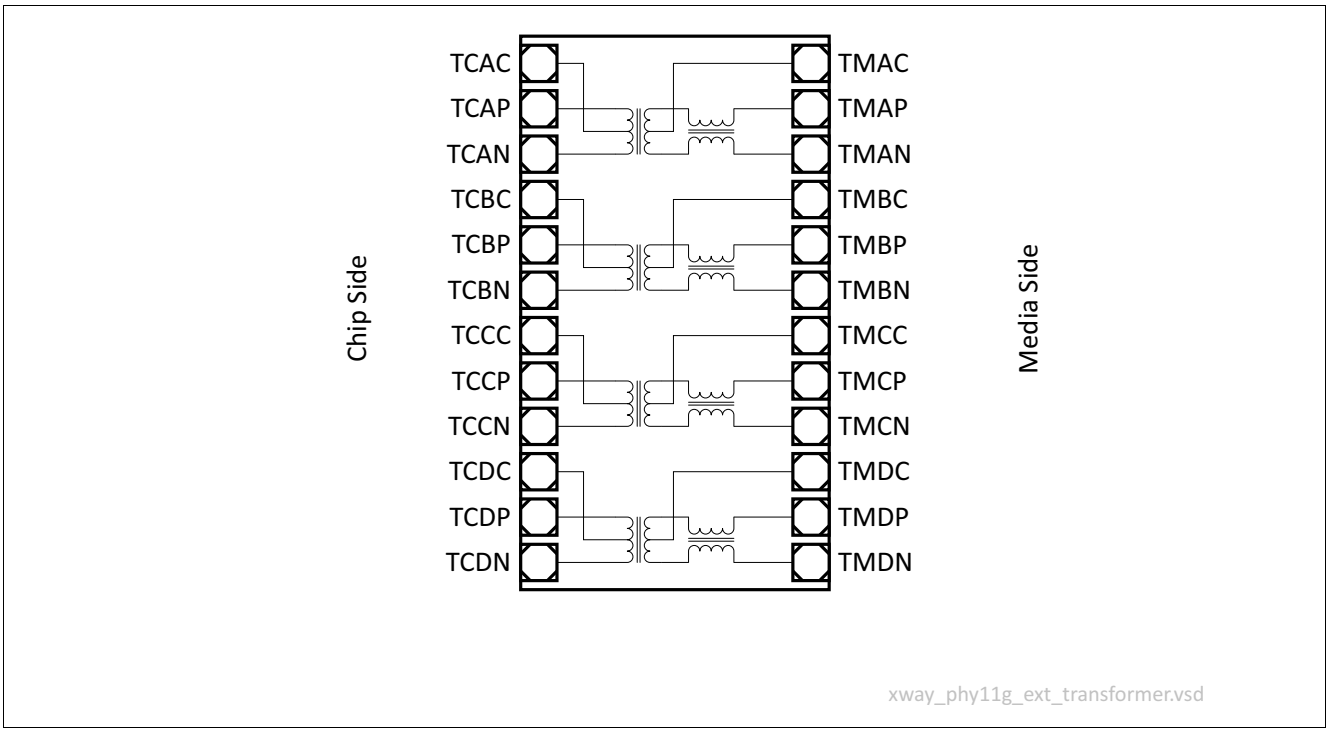


Figure 56 Schematic of a Typical Gigabit Ethernet Transformer Device

Table 64 Electrical Characteristics for Supported Transformers (Magnetics)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Turns ratio	1:tr	0.95	1.00	1.05		±5%
Differential-to-common-mode rejection	DCMR	43			dB	30 MHz
		37			dB	60 MHz
		33			dB	100 MHz
Crosstalk attenuation	CTA	45			dB	30 MHz
		40			dB	60 MHz
		35			dB	100 MHz
Insertion loss	IL			1	dB	0.1 MHz ≤ f ≤ 100 MHz

1) Also often referred to as “magnetics”.

Table 64 Electrical Characteristics for Supported Transformers (Magnetics) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Return loss	RL	18.0			dB	1 MHz ≤ f ≤ 30 MHz
		14.0			dB	31 MHz ≤ f ≤ 40 MHz
		13.0			dB	41 MHz ≤ f ≤ 50 MHz
		12.0			dB	51 MHz ≤ f ≤ 80 MHz
		10.0			dB	81 MHz ≤ f ≤ 100 MHz

6.8.4 RJ45 Plug

Table 65 describes the electrical characteristics of the RJ45 plug to be used in conjunction with the XWAY™ PHY11G.

Table 65 Electrical Characteristics for Supported RJ45 Plugs

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Crosstalk attenuation	CTA	45			dB	30 MHz
		40			dB	60 MHz
		35			dB	100 MHz
Insertion loss	IL			1	dB	1 MHz ≤ f ≤ 100 MHz
Return loss	RL	25.0			dB	1 MHz ≤ f ≤ 100 MHz

6.8.5 Twisted-Pair Common-Mode Rejection and Termination Circuitry

This section describes the external circuitry which is required to properly terminate the common mode of the Twisted-Pair Interface (TPI). Also, these external components are required to perform proper rejection of alien disturbers which are injected into the common mode of the TPI. **Figure 57** shows a typical external circuit, and in particular the common-mode components. **Table 63** defines the component values and their supported tolerances.

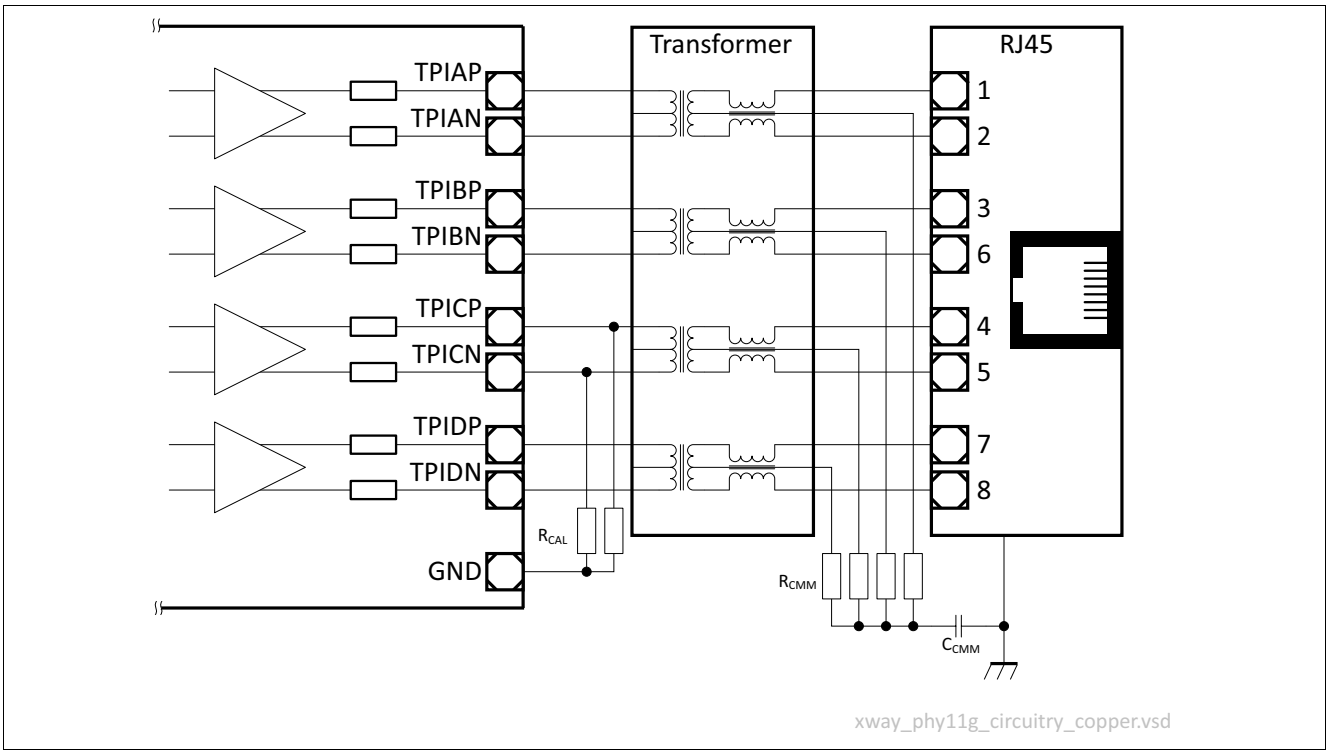


Figure 57 Twisted-Pair Common-Mode Rejection and Termination Circuitry

Table 66 Electrical Characteristics for supported Transformers (Magnetics)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Common-mode de-coupling capacitance (media end)	C_{CMM}	800	1000	1200	pF	±20%, 2 kV
Common-mode termination resistance (media end)	R_{CMM}	80	75	70	Ω	±10%
Calibration resistor	R_{CAL}	15840	16000	16160	Ω	±1%

6.8.6 SGMII Interface

Figure 58 shows the external analog circuitry that may be used to properly set up an SGMII MAC-to-PHY connection. All optional circuitry is considered. Since the XWAY™ PHY11G fully implements CDR (Clock and Data Recovery) functionality, it is not required to connect the MAC source clock. However, it may be required to wire the PHY source clock, in case the MAC does not implement CDR. If the MAC supports CDR, the elements shaded in dark gray in the figure may be omitted. The XWAY™ PHY11G does not directly generate the defined common-mode offset voltage of 1.2 V, since this is not required for an AC-coupled interface. If a MAC requires this offset voltage for proper DC-coupled operation, this offset can be injected using the resistive dividers (R_1 and R_2) marked by the regions shaded in light gray in the figure. If the MAC is purely AC-coupled, these components can be omitted. Also the MAC may have properly terminated inputs, and therefore the termination resistors R_3 are not necessary. Component values for this type of circuit are defined in Table 67. The simplest circuitry is used when the XWAY™ PHY11G is connected to a MAC with CDR and AC-coupled, well-terminated differential pins. This configuration is shown in Figure 59.

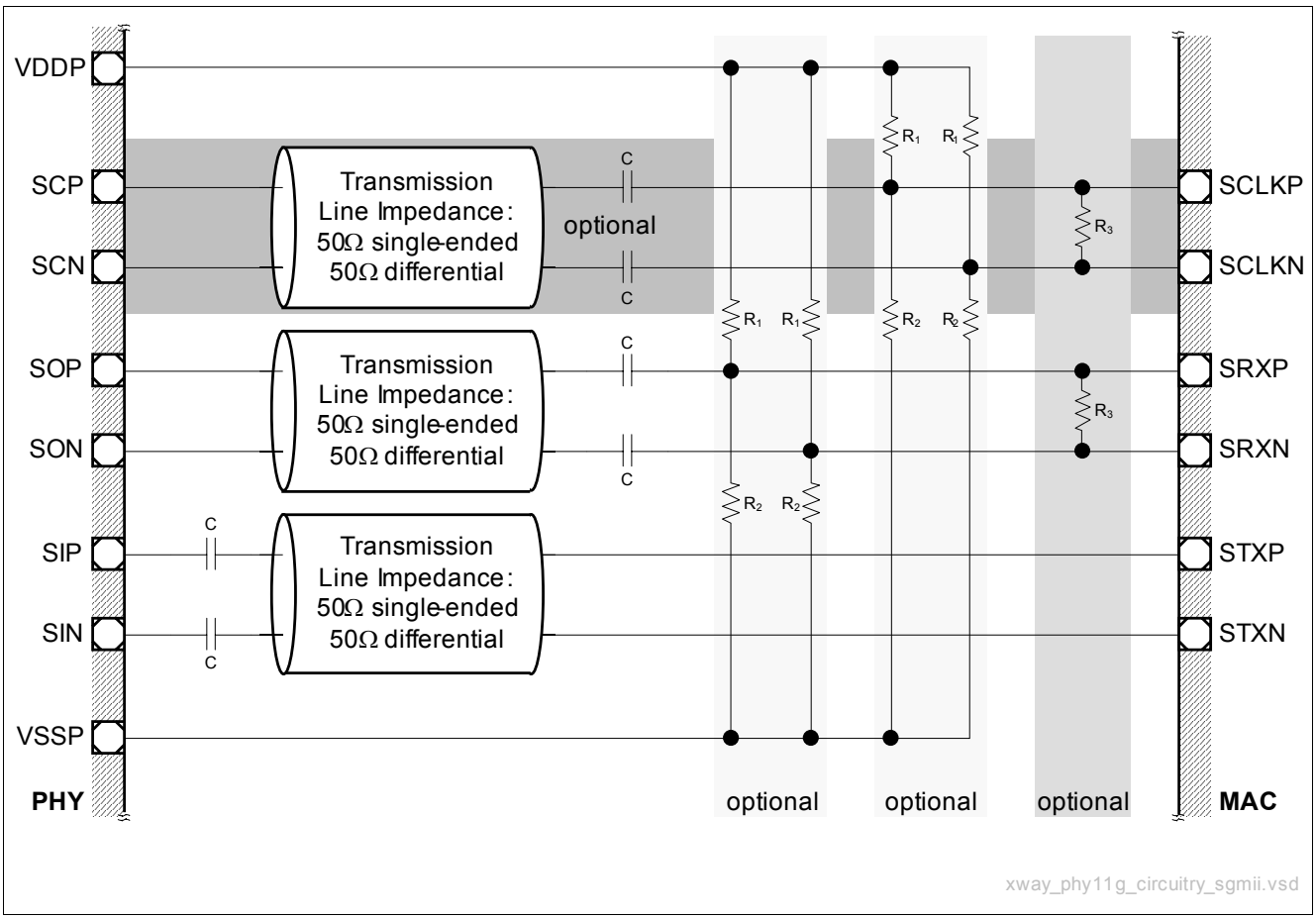


Figure 58 External Circuitry for SGMII

Table 67 Electrical Characteristics for the SGMII External Components

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
BIAS resistance 1	R_1	-10%	1k	+10%	Ω	VDDP = 3.3 V
		-10%	1k	+10%	Ω	VDDP = 2.5 V

Table 67 Electrical Characteristics for the SGMII External Components (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
BIAS resistance 2	R_2	-10%	1.7k	+10%	Ω	VDDP = 3.3 V
		-10%	1.1k	+10%	Ω	VDDP = 2.5 V
Termination resistance	R_3	-10%	100	+10%	Ω	
Coupling capacitance	C	-10%	100	+10%	nF	

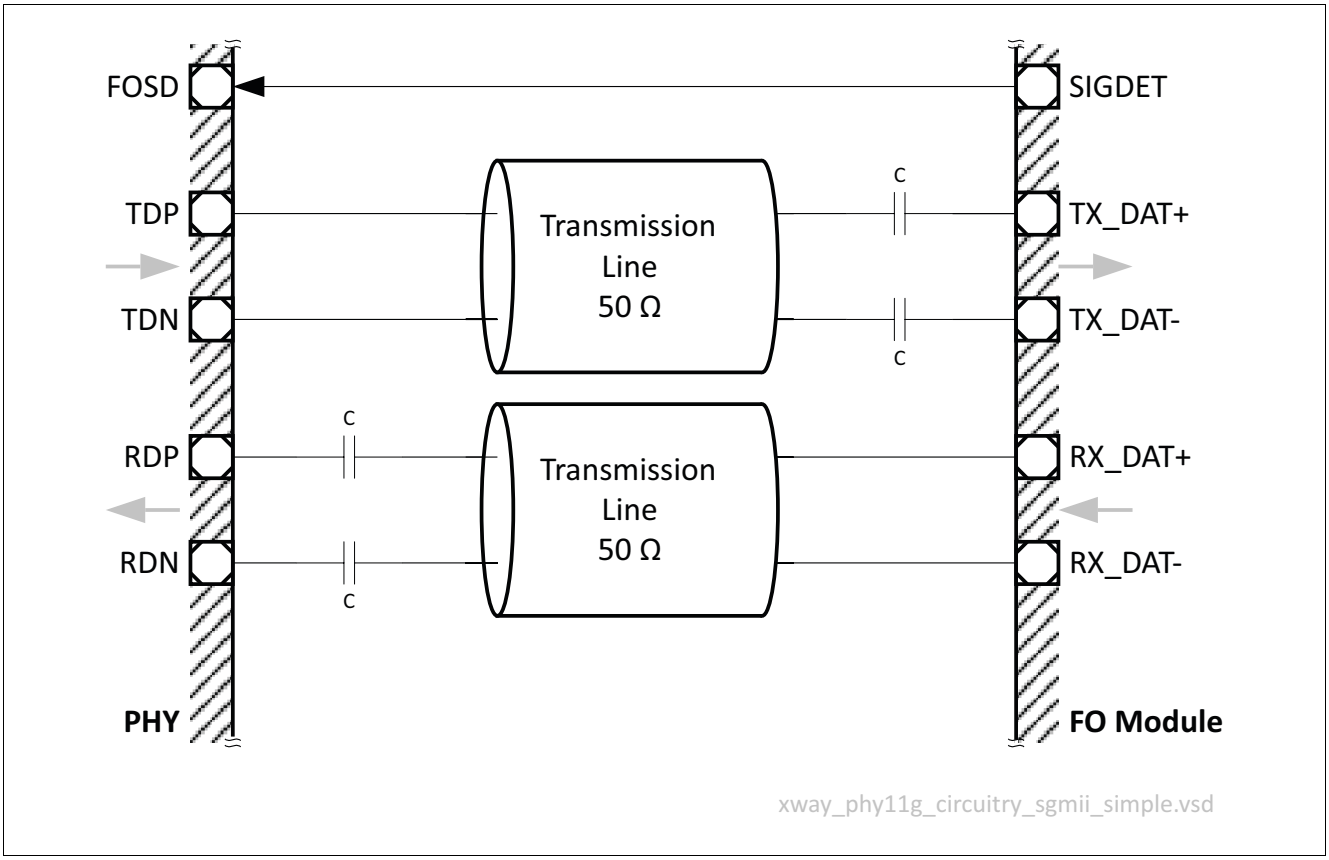


Figure 59 Simplified External Circuitry for SGMII

6.8.7 1000BASE-X Interface

Figure 60 depicts the external analog circ uitry that may be used to properly set up a 1000BASE-X PHY-to-FO connection. There are FO modules available that already integrate all coupling circuitry components, in which case a straight connection is sufficient and the external coupling caps may be omitted. Component values for this type of circuit are defined in **Table 68**. Many FO modules have open-drain outputs, which can cause conflict with the weak pull-down nature of the SIGDET pin. In such cases, a pull-up resistor R_{pu} should be included to weakly pull the SIGDET signal to V_{DDP} in a high-impedance situation. This is shown in **Figure 60** by the area shaded in gray.

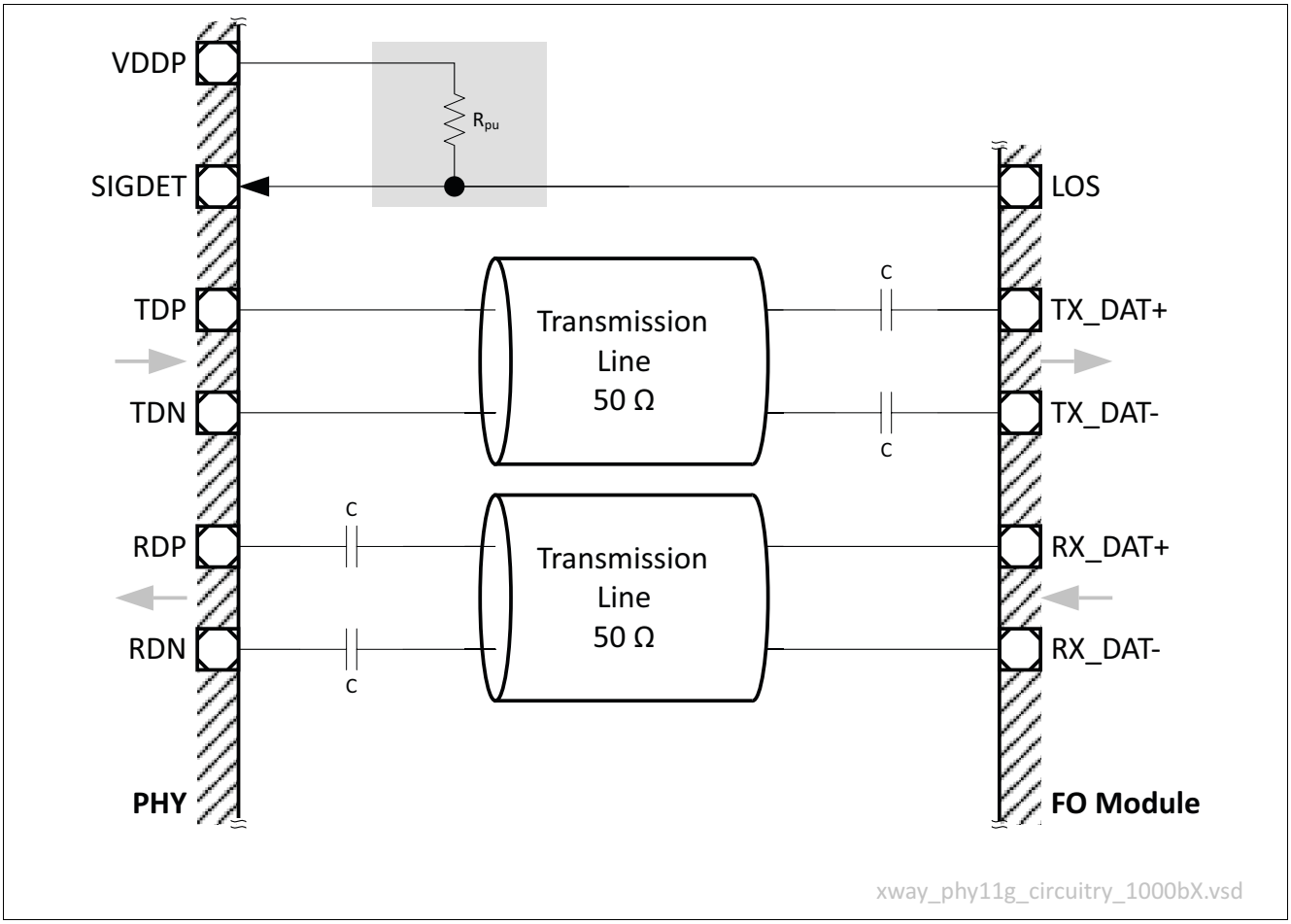


Figure 60 External Circuitry for a 1000BASE-X Interface

Table 68 Electrical Characteristics for the 1000BASE-X External Components

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Coupling capacitance	C	90	100	110	nF	±10%
Pull-up resistance	R_{pu}	1			kΩ	±10%

7 Package Outline

This section outlines all relevant packaging information.

The Lantiq XWAY™ PHY11G device is available in a 48-pin Very Thin Quad Flat Non-leaded (VQFN) package with an exposed pad (EPAD). The pad pitch is 0.5 mm and the size of the EPAD is 5.2 x 5.2 mm. The EPAD is used as the common ground and must be connected to the PCB ground plane. The package is a lead-free “green package”, and its exact name for purposes of reference is PG-VQFN48-15.

Figure 61 contains the top, side and bottom dimension drawings of the VQFN48 package.

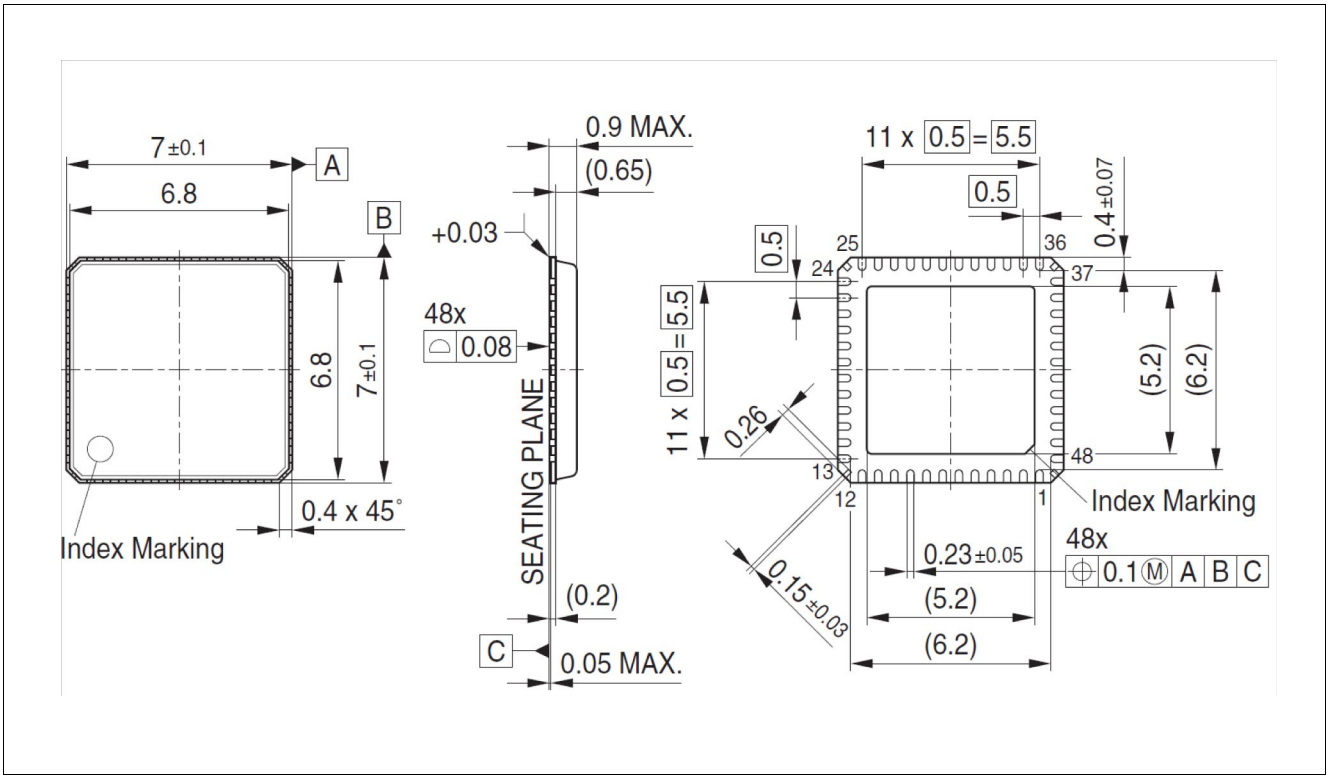


Figure 61 Package Dimension Drawing of the VQFN48 Package

Note: The corners of the VQFN Package expose contacts that are residuals of the EPAD construction. Such pins must not be connected, and false contacts to signal lines on the PCB layer must be prevented.

Package description, package handling, PCB and board assembly information is available on request.

Figure 62 shows a recommended soldering footprint for the VQFN48.

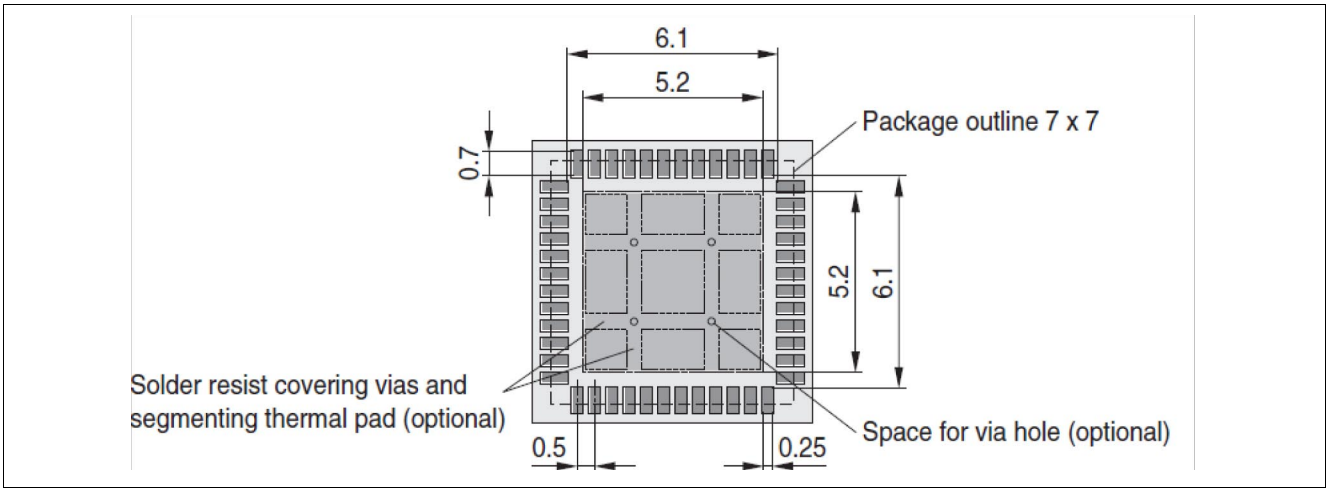


Figure 62 Soldering Footprint for the VQFN48 Package

The XWAY™ PHY11G is packed and shipped according to the specifications outlined in Figure 63.

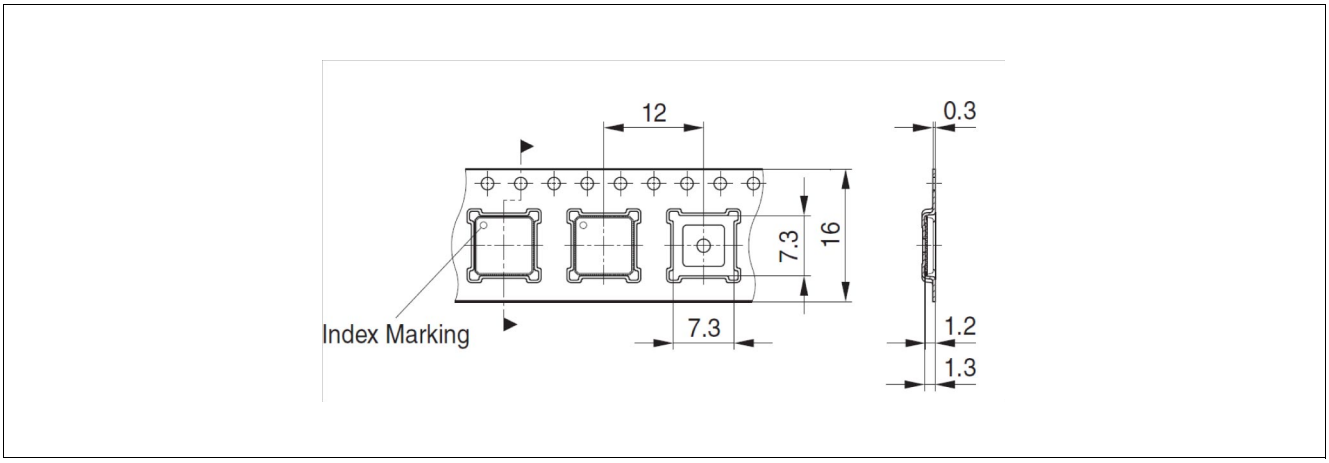


Figure 63 Tape Reel Packing Dimension Drawing of VQFN48

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Terminology

A	
ADS	Auto-Downspeed
ANEG	Auto-Negotiation
ANSI	American National Standards Institute
B	
BER	Bit Error Rate
BW	Bandwidth
C	
CAT5	Category 5 Cabling
CCR	Configuration Content Record
CDR	Clock and Data Recovery
CRC	Cyclic Redundancy Check
CSR	Configuration Signature Record
CRS	Carrier Sense
D	
DEC	Digital Echo Canceler
E	
ECM	Externally Controlled Mode (LED)
EEE	Energy-Efficient Ethernet
EEPROM	Electrically Erasable Programmable ROM
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
F	
FO	Fiber-Optic
G	
GbE	Gigabit Ethernet
GBIC	Gigabit Interface Converter
GMII	Gigabit Media-Independent Interface
GPIO	General Purpose Input/Output
H	
HBM	Human Body Model
HSTL	High-Speed Transceiver Logic
HYB	Hybrid
I	
I^2C	Internally Integrated Circuit Interface (also I2C)
IC	Integrated Circuit
ICM	Internally Controlled Mode (LED)
IEEE	Institute of Electrical and Electronics Engineers

IPG	Inter-Packet Gap
J	
JTAG	Joined Test Action Group
L	
LAN	Local Area Network
LED	Light Emitting Diode
LPI	Low Power Idle
LSB	Least Significant Bit
M	
MAC	Media Access Controller
MDI	Media-Dependent Interface
MDIO	Management Data Input/Output
MDIX	Media-Dependent Interface Crossover
MII	Media-Independent Interface
MMD	MDIO Manageable Device
MoCA	Multimedia over Coax Alliance
MSB	Most Significant Bit
N	
NAS	Network Attached Storage
NP	Next Page
O	
OSI	Open Systems Interconnection
OUI	Organizationally Unique Identifier
P	
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PD	Powered Device
PHY	Physical Layer (device)
PICMG	PCI Industrial Computer Manufacturers Group
PLL	Phase-Locked Loop
PMA	Physical Media Attachment
PoE	Power over Ethernet
PON	Passive Optical Network
PSE	Power-Sourcing Equipment
R	
RGMII	Reduced (pin-count) Gigabit Media-Independent Interface
RMII	Reduced (pin-count) Media-Independent Interface
RTBI	Reduced (pin-count) Ten-Bit Interface
RX	Receive
S	

SFP	Small Form-Factor Pluggable
SGMII	Serial Gigabit Media-Independent Interface
SMD	Surface-Mounted Device
SoC	System on Chip
T	
TAP	Test Access Port
TBI	Ten-Bit Interface
TPG	Test-Packet Generator
TPI	Twisted-Pair Interface
TX	Transmit
V	
VQFN	Very Thin Quad Flat Non-leaded
W	
WLAN	Wireless Local Area Network
WoL	Wake-on-LAN
X	
xMII	Symbolic shortening which denotes the set of supported MII Interfaces, e.g. RGMII and SGMII

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