AMI SEMICONDUCTOR

Peripheral Imaging Corporation

PI3034A
200DPI CIS Sensor Chip
Engineering Data Sheet

Description:

Peripheral Imaging Corporation PI3034A CIS sensor chip is a 200 dot per inch resolution linear array image sensor chip, which uses PIC's proprietary CMOS Image Sensing Technology. This image sensor's intended applications are to fabricate Contact Image Sensor, CIS modules with various lengths. This is accomplished by mounting them on a printed circuit board (PCB) through an end-to-end butting process. This process is generally referred to as the chip-on-board technology. Its typical circuit implementation in an A4 size 1728 elements CIS module is shown in a schematic diagram on page 6. The schematic demonstrates its operational implementation and interfacing circuits. They are used in facsimile, scanner, check reader, and office automation equipment.
Figure 1 is a block diagram of the sensor chip. Each sensor chip consists of 64 detector elements, their associated multiplexing switches, buffers, and a chip selector. The detector element-to-element spacing is approximately 125 um. The size of each chip without scribe lines is 7950 um by 290 um. Each sensor chip has 6 bonding pads. The pad symbols and functions are described in Table 1.

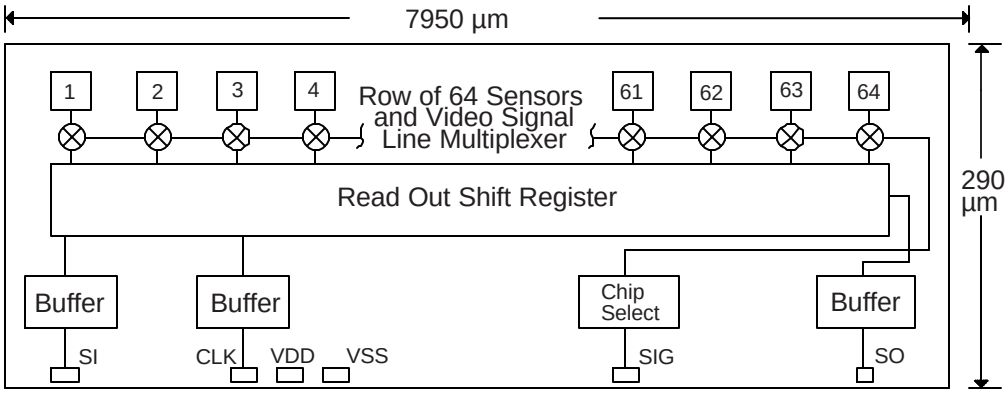


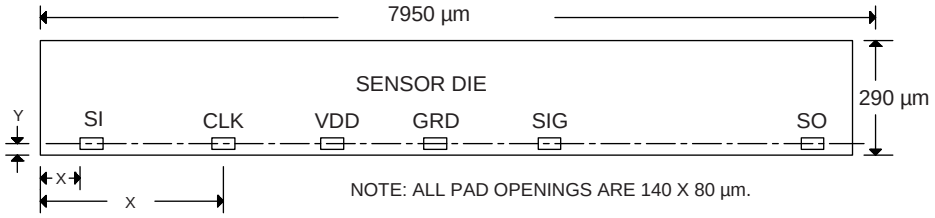
Figure 1. PI3034A Sensor Chip Block Diagram

SYMBOL	FUNCTION
SI	Start Pulse: Input to start the line scan.
CLK	Clock Pulse: Input to clock the Shift Register.
VDD	Positive Supply: +5 volt supply connected to substrate.
VSS	Digital Ground: Connection topside common.
SIG	Signal Current Output: Output for video signal current
SO	End of Scan Pulse: Output from the shift register at end of scan.

Table 1. Pad Symbols and Functions

Bonding pad layout diagram:

Figure 2 shows the bonding pad locations for PI3034A Sensor Chip relative to the lower left corner of the die.



PAD	FUNCTION	Y	X
SI	START INPUT	67.5	737.0
CLK	CLOCK INPUT	67.5	1546.5
VDD	+5 SUPPLY	67.5	2356.0
VSS	GROUND	67.5	3156.5
SIG	VIDEO SIGNAL OUT	67.5	3975.0
SO	SCAN OUTPUT	67.5	7213.0

NOTES:
1. THE DRAWING IS NOT TO SCALE.
2. THE DIE LENGTH AND WIDTH ARE GIVEN AS SHOWN.
3. THE PAD LOCATION ARE GIVEN IN THE TABLE.
4. THERE ARE TWO EXAMPLES OF THE X AND Y LOCATIONS SHOWN ON THE FIRST TWO PADS. THEY ARE MEASURED TO THE LEFT BOTTOM CORNER OF THE PAD OPENING.
5. ALL DIMENSIONS ARE IN µm.

PI3034A IMAGE SENSOR

Figure 2. Bonding Pad Layout Diagram

Electro-Optical Characteristics (25 ℃)

Table 2, below, lists the electro-optical characteristics of PI3034A sensor chip at 25 ℃.

Parameters	Symbols	Typical	Units	Notes
Number of Photo-elements		64	elements	
Pixel-to-pixel spacing		125	µm	
Line scanning rate	Tint (1)	3.45	ms/line	
Clock frequency	f (2)	0.5	MHz	
Video Output Voltage Amplitude	Vp (3)	1.0	Volts	Vp depends the output circuits. See note 3.
Output voltage non-uniformity	Up (4)	± 7.5	%	

Chip-to-chip non-uniformity	Ud	± 7.5	%	
Dark output voltage	Vd (5)	<50	mV	
Dark output non-uniformity	Ud (6)	<50	mV	

Table 2. Electro-Optical Characteristic

Notes: (1) Tint stands for the line scanning rate or the integration time. It is determined by the time interval between two start pulses.

(2) f stands for the input clock frequency:
@ 500 kHz the total active line scan time for a A4 CIS module is 3.45 ms of the line integration time.

(3) Vp is an average of the pixel amplitudes in one complete line scan. These video pixels are converted from signal currents produced by the phototransistor at each pixel site. The signal current charges the video line capacitance that is isolated with amplifier buffer. The output current is proportional to the charges that have been collected on the phototransistor's base through a photon-to-electron conversion process. These charges on the base draw signal current through the emitter proportionally to the Beta of the phototransistor. Then the emitter current flows out onto the output video line capacitance where it is integrated and converted to signal voltage. This is the signal voltage that the host receiver senses. Before accessing the subsequent pixel, this video signal on the video line capacitance is reset through a shunt switch on the video line. Then the next pixel in sequence is readout onto the video line. This video buffer amplifier terminating the video line provides the necessary amplification. Most user generally set their operating output signal to ~ 1.0 V peak average with the saturation level of ~ 1.5 V. For the circuit reference see the attached schematic diagram on page 6. Typical amplification (adjustable) gain is between 4 to 5 times the voltage that is measured on the video line.

(4) Up = [(Vpmax-Vp)/ Vp]x100%
Or [(Vp-Vpmin)/ Vp]x100%

$$\text{Where Vp} = \sum_{n}^{N} Vpn / N$$

Vpmax is the maximum pixel output voltage in the light.
Vpmin is the minimum pixel output voltage in the light.
In the light means module exposed a uniform light.

(5) Vd = (Vdmax+Vdmin)/2
Vdmax is the maximum pixel output voltage in the dark.
Vdmin is the minimum pixel output voltage in the dark.
In the dark means that sensor has no exposure to the light.

(6) Ud = [(Vdmax-Vdmin)/ Vd]x100%

Absolute Maximum Ratings (not operational conditions):

Parameters	Symbol	Maximum Rating	Units
Power Supply Voltage	VDD	10	Volts
Power Supply Current	IDD	<2.0	ma
Input clock pulse (high level)	Vih	Vdd + 0.5	Volts
Input clock pulse (low level)	Vil	-0.25	Volts

Table 3. Maximum Specification

Operating Conditions at Room Temperature

Parameters	Symbol	Min.	Typical	Max.	Units	Notes
Power Supply	VDD	4.5	5.0	5.5	Volts	
Input clock pulses high level	Vih (1)	3.0	5.0	VDD	Volts	1
Input clock pulse low level	Vil (1)	0	0	0.8	Volts	1
Operating high level exposed output	Vsig (Isig) (2)		1.0		Volts	2
Clock Frequency	f		0.5	1.0	MHz	
Clock pulse duty cycle			25		%	
Clock pulse high durations	tw		0.5		µsec	
Integration time	Tint		3.45	10	ms	
Operating Temperature	Top		25	50	^{o}C	

Table 4. Operating Specifications

Note: (1) Applies to both CLK and SI.
(2) See note 3 under Table 2. Electro-Optical Characteristics. See the schematic on page 6.

Switching Characteristics @ 25 ℃

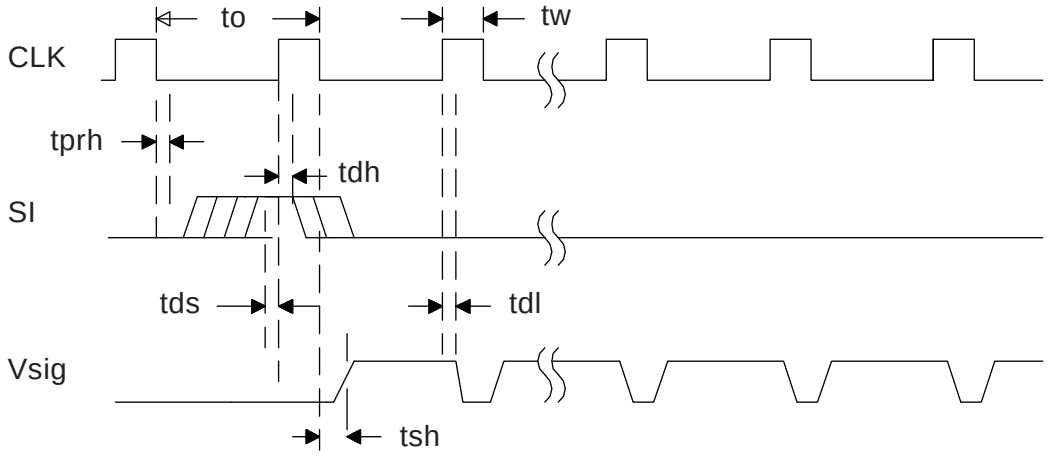


Figure 3. Timing Diagram of the PI3034A Sensor

Item	Symbol	Minimum	Mean	Maximum	Units
Clock cycle time	to	1000		10000	ns
Clock pulse width(1)	tw	250			ns
Clock duty cycle		25	50	75	%
Data setup time	tds	50			ns
Data hold time	tdh	20			ns
Prohibit crossing time(2)	tprh		30		ns
EOS rise delay	terdl		60		ns
EOS fall delay	tefdl		70		ns
Signal delay time(3)	tdl		100		ns
Signal settling time(3)	tsh		200		ns

Table 5. Timing Symbols and Definition

Notes:

1. Clock pulse width varies with frequency, as it was explained foregoing paragraphs.
2. Prohibit crossing time to insure that two start pulses are not locked into the shift register during any single scan time.
3. Pixel delay times and settling time depend on the output amplifier. The numbers, which are given, are measured with an EL2044 amplifier. The faster the amplifier, the faster the signal will respond. In other words, faster rise and settle times are faster.

Output Circuits for Video Signal

The circuit in following page shows the PI3034A in a CIS module application. It also serves not only a reference for the above operational explanation given in note 3 under Table 2. Electro-Optical Characteristics; it further exemplifies a method for interfacing the device in developing a 1728 element, A4 size CIS module.