8V to 36Vin, 15A Cool-Power ZVS Buck Regulator

Description

The PI33XX-X1 is a family of high efficiency, wide input range DC-DC ZVS-Buck regulators integrating controller, power switches, and support components all within a high density System-in-Package (SiP). The integration of a high performance Zero-Voltage Switching (ZVS) topology, within the PI33XX-X1 series, increases point of load performance providing best in class power efficiency. The PI33XX-X1 requires only an external inductor and minimal capacitors to form a complete DC-DC switching mode buck regulator.

Device	Output Voltage		Iout Max
	Set	Range	
PI3311-X1-LGIZ	1.0V	1.0 to 1.4V	15A
PI3318-X1-LGIZ	1.8V	1.4 to 2.0V	15A
PI3312-X1-LGIZ	2.5V	2.0 to 3.1V	15A
PI3301-X1-LGIZ	3.3V	2.3 to 4.1V	15A

Table 1 *- PI33XX-X1-X1 Portfolio.*

The ZVS architecture also enables high frequency operation while minimizing switching losses and maximizing efficiency. The high switching frequency operation reduces the size of the external filtering components, improves power density, and enables very fast dynamic response to line and load transients. The PI33XX-X1 series sustains high switching frequency all the way up to the rated input voltage without sacrificing efficiency and, with its 20ns minimum on-time, supports large step down conversions up to 36Vin.

Features

- High Efficiency ZVS-Buck Topology
- Wide input voltage range of 8V to 36V
- Very-Fast transient response
- High accuracy pre-trimmed output voltage
- User adjustable soft-start & tracking
- Power-up into pre-biased load (select versions)
- Parallel capable with single wire current sharing
- Input Over/Under Voltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Over Temperature Protection (OTP)
- Fast and slow current limits
- -40°C to 125°C operating range (T_J)
- Optional I^2C functionality & programmability:
  - Vout margining
  - Fault reporting
  - Enable and SYNCI pin polarity
  - Phase delay (interleaving multiple regulators)

Applications

- High efficiency systems
- Computing, Communications, Industrial, Automotive Equipment
- High voltage battery operation

Package Information

- 10mm x 14mm x 2.6mm LGA SiP

I^2C is a trademark of NXP Semiconductors

Contents

Order Information

Cool-Power	Output Range		Iout Max	Package	Transport Media
	Set	Range			
PI3311-01-LGIZ	1.0V	1.0 to 1.4V	15A	10mm x 14mm 123-pin LGA	TRAY
PI3318-01-LGIZ	1.8V	1.4 to 2.0V	15A	10mm x 14mm 123-pin LGA	TRAY
PI3312-01-LGIZ	2.5V	2.0 to 3.1V	15A	10mm x 14mm 123-pin LGA	TRAY
PI3301-01-LGIZ	3.3V	2.3 to 4.1V	15A	10mm x 14mm 123-pin LGA	TRAY
I^2C Functionality & Programmability					
PI3311-21-LGIZ	1.0V	1.0 to 1.4V	15A	10mm x 14mm 123-pin LGA	TRAY
PI3318-21-LGIZ	1.8V	1.4 to 2.0V	15A	10mm x 14mm 123-pin LGA	TRAY
PI3312-21-LGIZ	2.5V	2.0 to 3.1V	15A	10mm x 14mm 123-pin LGA	TRAY
PI3301-21-LGIZ	3.3V	2.3 to 4.1V	15A	10mm x 14mm 123-pin LGA	TRAY

Absolute Maximum Ratings

VIN		-0.7V to 36V
VS1		-0.7 to 36V, -4V for 5ns
SGND		100mA
PGD, SYNCO, SYNCI, EN, EAO, ADJ, TRK, ADR1, ADR2, SCL, SDA		-0.3V to 5.5V / 5mA
VOUT, REM	PI3311-X0-LGIZ	-0.3V to 5.5V
	PI3318-X0-LGIZ	-0.5V to 9V
	PI3312-X0-LGIZ	-0.8V to 13V
	PI3301-X0-LGIZ	-1.0V to 18V
Storage Temperature		-65°C to 150°C
Operating Junction Temperature		-40°C to 125°C
Soldering Temperature for 20 seconds		245°C
ESD Rating		2kV HBM

Notes: At 25°C ambient temperature. Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted. Test conditions are per the specifications within the individual product electrical characteristics.

Block Diagram

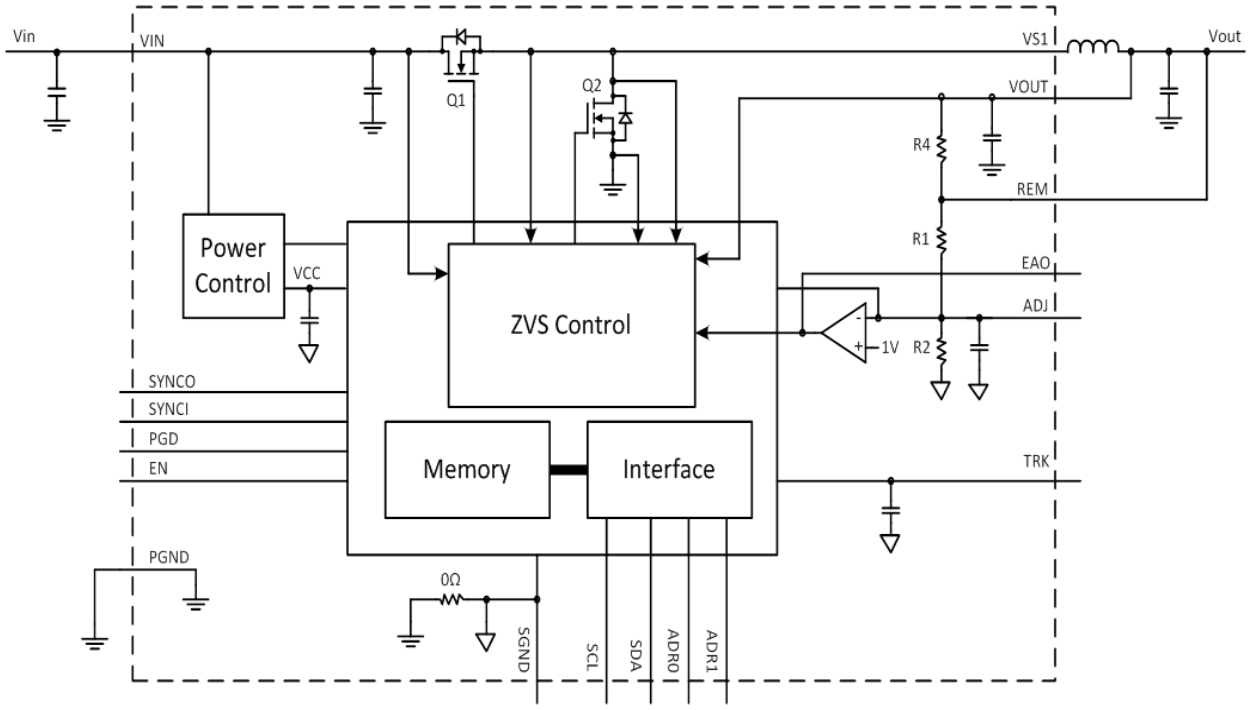


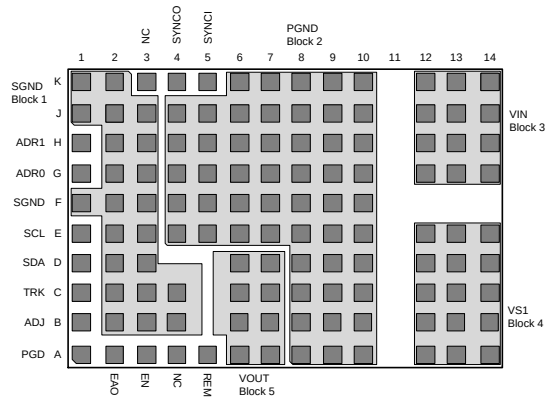
Figure 1: *Simplified Block Diagram*

(I^2C pins SCL, SDA, ADR0, and ADR1 only active for PI33XX-21 device versions)

Pin Description

Name	Number	Description
SGND	Block 1	**Signal ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO, ADJ and I^2C (options) communication returns. SGND and PGND are star connected within the regulator package.
PGND	Block 2	**Power ground:** VIN and VOUT power returns
VIN	Block 3	**Input voltage:** and sense for UVLO, OVLO and feed forward ramp
VOUT	Block 5	**Output voltage:** and sense for power switches and feed-forward ramp
VS1	Block 4	**Switching node:** and ZVS sense for power switches
PGD	A1	**Parallel Good:** Used for parallel timing management intended for lead regulator.
EAO	A2	**Error amp output:** External connection for additional compensation and current sharing.
EN	A3	**Enable Input:** Regulator enable control. Asserted high or left floating – regulator enabled; Asserted low, regulator output disabled. Polarity is programmable via I^2C interface.
REM	A5	**Remote Sense:** High side connection. Connect to output regulation point.
ADJ	B1	**Adjust input:** An external resistor may be connected between ADJ pin and SGND or VOUT to trim the output voltage up or down.
TRK	C1	**Soft-start and track input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft-start.
NC	K3, A4	**No Connect:** Leave pins floating.
SYNCO	K4	**Synchronization output:** Outputs a low signal for ½ of the minimum period for synchronization of other converters.
SYNCI	K5	**Synchronization input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use.
SDA	D1	**Data Line:** Connect to SGND for PI33XX-10 and -11. For use with PI33XX-20 and -21 only.
SCL	E1	**Clock Line:** Connect to SGND for PI33XX-01. For use with PI33XX-21 only.
ADR1	H1	**Tri-state Address** : No connect for PI33XX-01. For use with PI33XX-21 only.
ADR0	G1	**Tri-state Address** : No connect for PI33XX-01. For use with PI33XX-21 only.

Package Pin-Out



123-Lead LGA (10mm x 14mm)
Top view

Block 1: B2-4, C2-4, D2-3, E2-3, F1-3, G2-3, H2-3, J1-3, K1-2

Block 2: A8-10, B8-10, C8-10, D8-10, E4-10, F4-10, G4-10, H4-10, J4-10, K6-10

Block 3: G12-14, H12-14, J12-14, K12-14

Block 4: A12-14, B12-14, C12-14, D12-14, E12-14,

Block 5: A6-7, B6-7, C6-7, D6-7

PI3311-X1 (1.0 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =24V, L1=85nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Specifications						
Input Voltage	V_{IN_DC}	8	24	36	V	Minimum 1mA load required
Input Current	I_{IN_DC}		740		mA	Vin = 24V, T_C = 25°C, Iout=15A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}			25	mA	Note 2.
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled (no load)
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	Note 2.
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	0.987	1.0	1.013	V	Note 2.
Output Voltage Trim Range	V_{OUT_DC}	1.0		1.4	V	Note 3.
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10		%	@25°C, 8V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10		%	@25°C, 0.5A<Iout<15A
Output Voltage Ripple	V_{OUT_AC}		45		mVp-p	Iout=5A, Cout=8x100µF, 20MHz BW Note 4.
Continuous Output Current Range	I_{OUT_DC}	0.001		15	A	Note 2.
Current Limit	I_{OUT_CL}		18.0		A	
Protection						
VIN UVLO Start Threshold	V_{UVLO_START}	7.10	7.60	8.00	V	
VIN UVLO Stop Threshold	V_{UVLO_STOP}	6.80	7.25	7.60	V	
VIN UVLO Hysteresis	V_{UVLO_HYS}		0.35		V	
VIN OVLO Start Threshold	V_{OVLO_START}	36.1	37.6		V	
VIN OVLO Stop Threshold	V_{OVLO_STOP}	37.0	38.4		V	
VIN OVLO Hysteresis	V_{OVLO_HYS}		0.8		V	
VIN UVLO/OVLO Fault Delay Time	t_{f_DLY}			128	Cycles	Number of the switching freq cycles
VIN UVLO/OVLO Response Time	t_f		500		ns	
Output Over Voltage Protection	V_{OVP}		20		%	Above V_{OUT}
Over-Temperature Fault Threshold	T_{OTP}	130	135	140	°C	Note 2.
Over-Temperature Restart Hysteresis	T_{OTP_HYS}		30		°C	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33XX evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or Vout is modified.

Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

PI3311-X1 (1.0 Vout) Electrical Characteristics

Specifications apply for -40 C < T_J < 125 C, Vin =24V, L1=85nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Timing						
Switching Frequency	f_S		500		kHz	Note 6.
Fault Restart Delay	t_{FR_DLY}		30		ms	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	Relative to set switching frequency. Note 3.
SYNCI Threshold	V_{SYNCI}		2.5		V	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5			V	Source 1mA
SYNCO Low	V_{SYNCO_LO}			0.5	V	Sink 1mA
SYNCO Rise Time	t_{SYNCO_RT}		10		ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10		ns	20pF load
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}	0		1.04	V	Internal reference tracking range.
TRK Max Output Voltage	V_{TRK_MAX}		1.2		V	
TRK Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2		ms	C_{TRK} = 0uF
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}		2		V	With positive logic EN polarity
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}		0		V	With negative logic EN polarity
Source Current	I_{EN_SO}		-50		µA	With positive logic EN polarity
Sink Current	I_{EN_SK}		50		µA	With negative logic EN polarity

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33XX evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or Vout is modified.

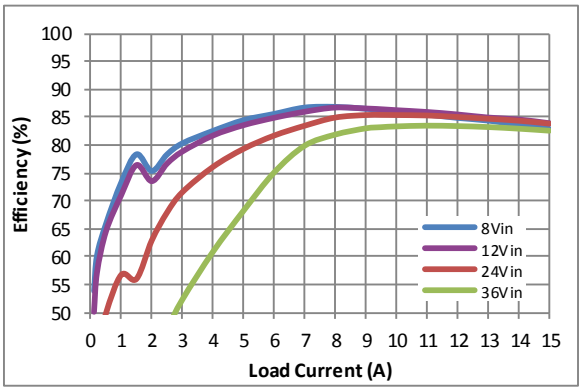
Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

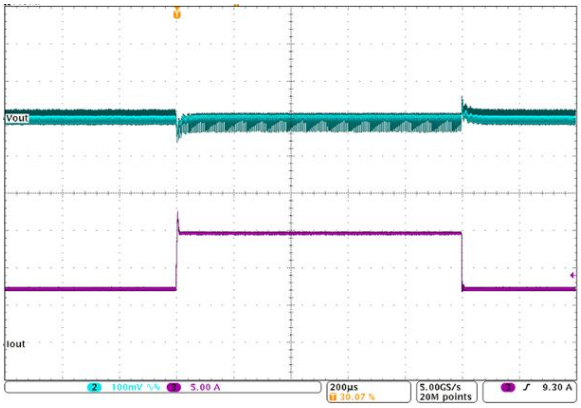
PI3311-X1 (1.0 Vout) Electrical Characteristics

Efficiency at 25°C



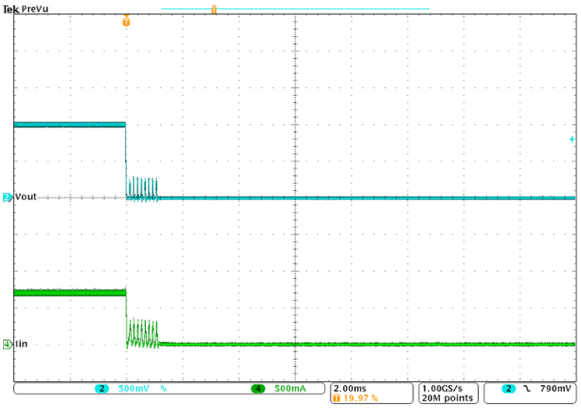
Regulator and inductor performance **331101**

Transient Response: 7.5A to 15A, at 5A/µs



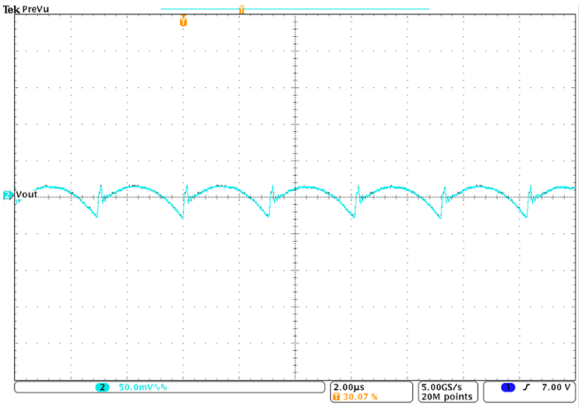
24Vin to 1.0Vout, Cout = 8X 100µF Ceramic **331102**
Vout (Ch2) = 100mV/Div, Iout (Ch3) = 5A/Div, 200uS/Div

Short Circuit Test



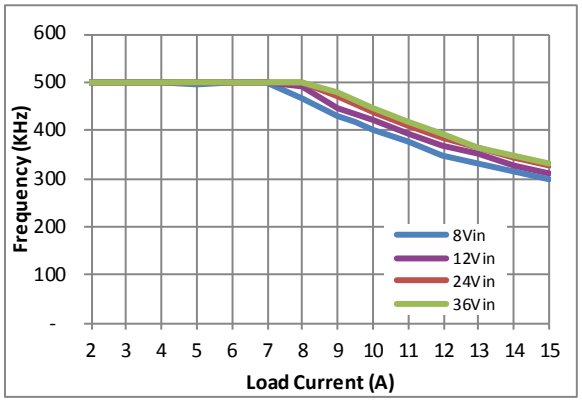
Vout (Ch2) = 500mV/Div, Iin (Ch4) = 500mA/Div, 2ms/Div **331103**

Output Ripple: 24Vin, 1.0Vout at 15A



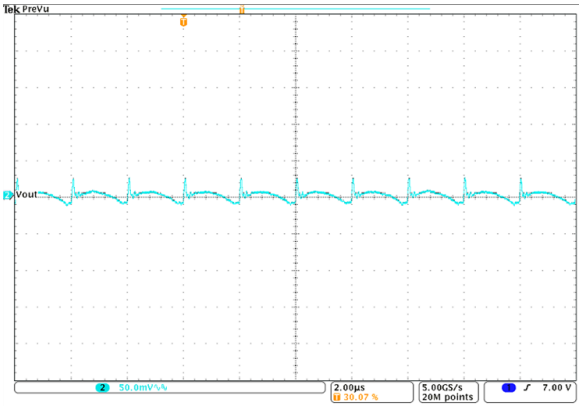
Cout = 8X 100µF Ceramic, Vout = 50mV/Div, 2.0us/Div **331104**

Switching Frequency vs. Load Current



331105

Output ripple: 24Vin, 1.0Vout at 7A



Cout = 8X 100µF Ceramic, Vout = 50mV/Div, 2.0us/Div **331106**

PI3318-X1 (1.8 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =24V, L1=125nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Specifications						
Input Voltage	V_{IN_DC}	8	24	36	V	
Input Current	I_{IN_DC}		1.25		A	Iout=15A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}			45	mA	Note 2.
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled (no load)
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	Note2.
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	1.773	1.8	1.827	V	Note 2.
Output Voltage Trim Range	V_{OUT_DC}	1.4		2.0	V	Note 3.
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10		%	@25°C, 8V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10		%	@25°C, 0.5A<Iout<15A
Output Voltage Ripple	V_{OUT_AC}		30		mVp-p	Iout=5A, Cout=8x100µF, 20MHz BW Note 4.
Continuous Output Current Range	I_{OUT_DC}	0		15	A	Note 2.
Current Limit	I_{OUT_CL}		18.0		A	
Protection						
VIN UVLO Start Threshold	V_{UVLO_START}	7.10	7.60	8.00	V	
VIN UVLO Stop Threshold	V_{UVLO_STOP}	6.80	7.25	7.60	V	
VIN UVLO Hysteresis	V_{UVLO_HYS}		0.35		V	
VIN OVLO Start Threshold	V_{OVLO_START}	36.1	37.6		V	
VIN OVLO Stop Threshold	V_{OVLO_STOP}	37.0	38.4		V	
VIN OVLO Hysteresis	V_{OVLO_HYS}		0.8		V	
VIN UVLO/OVLO Fault Delay Time	t_{f_DLY}			128	Cycles	Number of the switching freq cycles
VIN UVLO/OVLO Response Time	t_f		500		ns	
Output Over Voltage Protection	V_{OVP}		20		%	Above V_{OUT}
Over-Temperature Fault Threshold	T_{OTP}	130	135	140	°C	Note 2.
Over-Temperature Restart Hysteresis	T_{OTP_HYS}		30		°C	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33XX evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or Vout is modified.

Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

PI3318-X1 (1.8 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =24V, L1=125nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Timing						
Switching Frequency	f_S		550		kHz	Note 6.
Fault Restart Delay	t_{FR_DLY}		30		ms	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	Relative to set switching frequency. Note 3.
SYNCI Threshold	V_{SYNCI}		2.5		V	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5			V	Source 1mA
SYNCO Low	V_{SYNCO_LO}			0.5	V	Sink 1mA
SYNCO Rise Time	t_{SYNCO_RT}		10		ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10		ns	20pF load
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}	0		1.04	V	Internal reference tracking range.
TRK Max Output Voltage	V_{TRK_MAX}		1.2		V	
TRK Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2		ms	C_{TRK} = 0uF
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}		2		V	
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		µA	
Sink Current	I_{EN_SK}		50		µA	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33XX evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or Vout is modified.

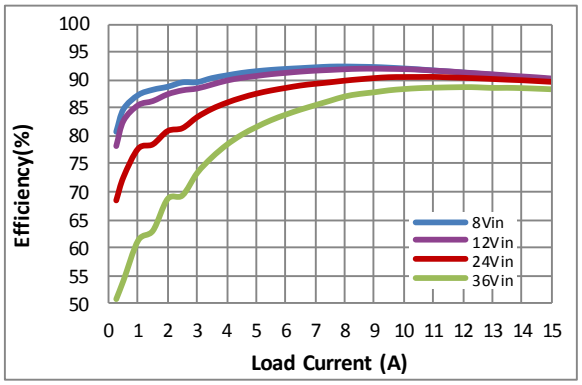
Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

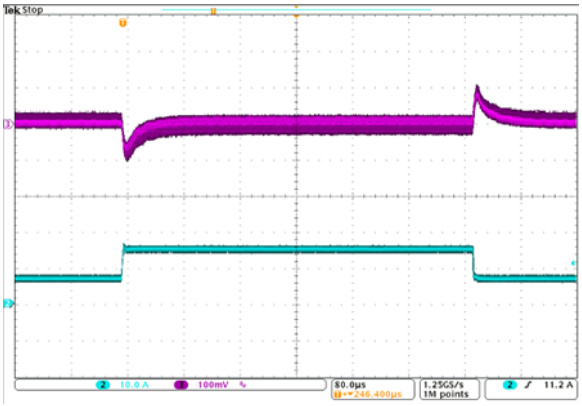
PI3318-X1 (1.8 Vout) Electrical Characteristics

Efficiency at 25°C



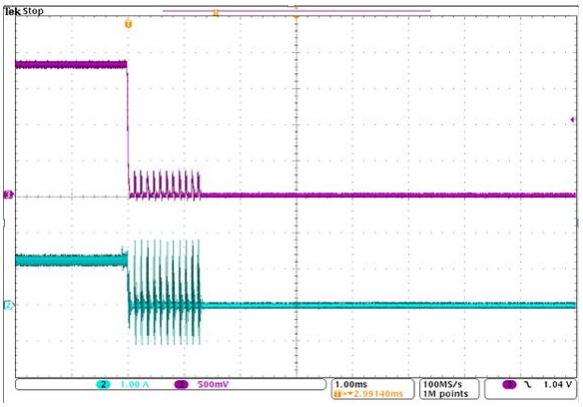
Regulator and inductor performance **331801**

Transient Response: 7A to 15A, at 5A/µs



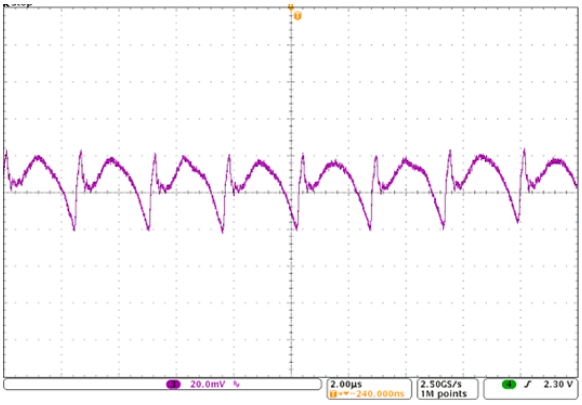
24Vin to 1.8Vout, Cout = 8X 100µF Ceramic **331802**
Vout (Ch3) = 100mV/Div, Iin (Ch4) = 10A/Div, 80us/Div

Short Circuit Test



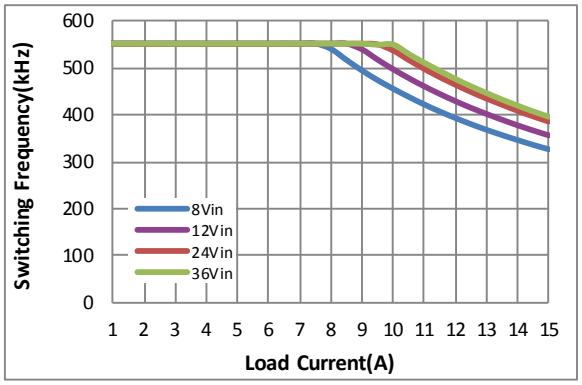
Vout (Ch3) = 500mV/Div, Iin (Ch2) = 1A/Div, 1ms/Div **331803**

Output Ripple: 24Vin, 1.8Vout at 15A



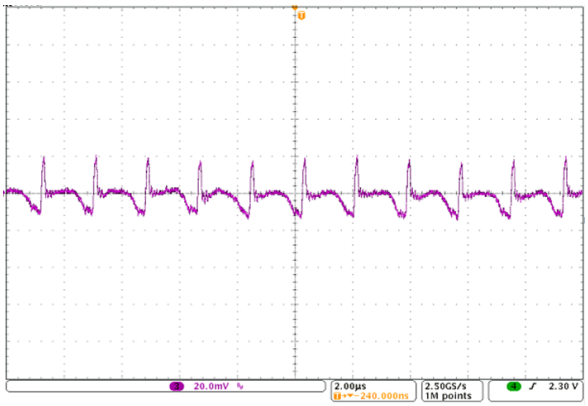
Cout = 8X 100µF Ceramic, Vout = 20mV/Div, 2.0us/Div **331804**

Switching Frequency vs. Load Current



331805

Output ripple: 24Vin, 1.8Vout at 7.5A



Cout = 8X 100µF Ceramic, Vout = 20mV/Div, 2.0us/Div **331806**

PI3312-X1 (2.5 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =24V, L1=125nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Specifications						
Input Voltage	V_{IN_DC}	8	24	36	V	Note 7.
Input Current	I_{IN_DC}		1.7		A	Vin = 24V, T_C = 25°C, Iout=15A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}			60	mA	Note 2.
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled (no load)
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	Note 2.
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	2.465	2.5	2.535	V	Note 2.
Output Voltage Trim Range	V_{OUT_DC}	2.0	2.5	3.1	V	Note 3. Note 7.
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10		%	@25°C, 8V<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10		%	@25°C, 0.5A<Iout<15A
Output Voltage Ripple	V_{OUT_AC}		28		mVp-p	Iout=5A, Cout=8x100µF, 20MHz BW Note 4.
Continuous Output Current Range	I_{OUT_DC}	0		15	A	Note 2. Note 7.
Current Limit	I_{OUT_CL}		18.0		A	
Protection						
VIN UVLO Start Threshold	V_{UVLO_START}	7.10	7.60	8.00	V	
VIN UVLO Stop Threshold	V_{UVLO_STOP}	6.80	7.25	7.60	V	
VIN UVLO Hysteresis	V_{UVLO_HYS}		0.35		V	
VIN OVLO Start Threshold	V_{OVLO_START}	36.1	37.6		V	
VIN OVLO Stop Threshold	V_{OVLO_STOP}	37.0	38.4		V	
VIN OVLO Hysteresis	V_{OVLO_HYS}		0.8		V	
VIN UVLO/OVLO Fault Delay Time	t_{f_DLY}			128	Cycles	Number of the switching freq cycles
VIN UVLO/OVLO Response Time	t_f		500		ns	
Output Over Voltage Protection	V_{OVP}		20		%	Above V_{OUT}
Over-Temperature Fault Threshold	T_{OTP}	130	135	140	°C	Note 2.
Over-Temperature Restart Hysteresis	T_{OTP_HYS}		30		°C	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33XX evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or Vout is modified.

Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

Note 7: Minimum 5V between Vin-Vout must be maintained or a minimum load of 1mA required.

PI3312-X1 (2.5 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =24V, L1=125nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Timing						
Switching Frequency	f_S		650		kHz	Note 6.
Fault Restart Delay	t_{FR_DLY}		30		ms	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	Relative to set switching frequency. Note 3.
SYNCI Threshold	V_{SYNCI}		2.5		V	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5			V	Source 1mA
SYNCO Low	V_{SYNCO_LO}			0.5	V	Sink 1mA
SYNCO Rise Time	t_{SYNCO_RT}		10		ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10		ns	20pF load
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}	0		1.04	V	Internal reference tracking range.
TRK Max Output Voltage	V_{TRK_MAX}		1.2		V	
TRK Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2		ms	C_{TRK} = 0uF
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}		2		V	
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		µA	
Sink Current	I_{EN_SK}		50		µA	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33XX evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or Vout is modified.

Note 4: Refer to Output Ripple plots.

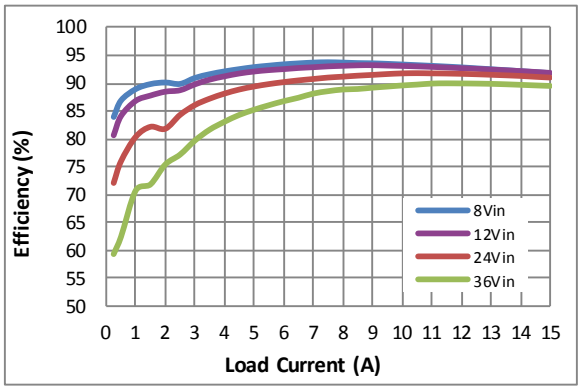
Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

Note 7: Minimum 5V between Vin-Vout must be maintained or a minimum load of 1mA required.

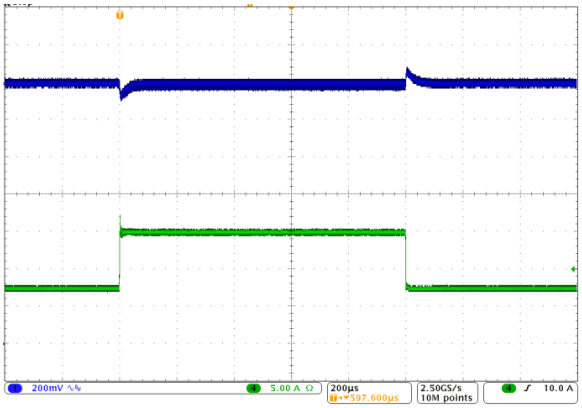
PI3312-X1 (2.5 Vout) Electrical Characteristics

Efficiency at 25°C



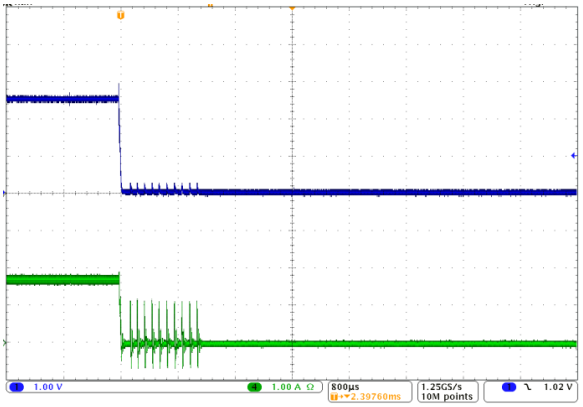
Regulator and inductor performance **331201**

Transient Response: 7.5A to 15A, at 5A/µs



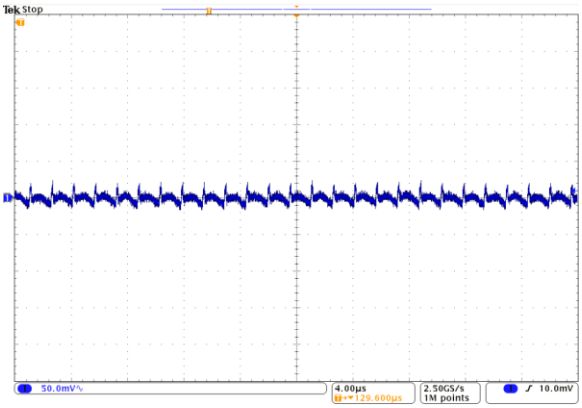
24Vin to 2.5Vout, Cout = 8 x 100µF Ceramic **331202**
Vout (Ch1) = 200mV/Div, Iout (Ch4) = 5A/Div, 200us/Div

Short Circuit



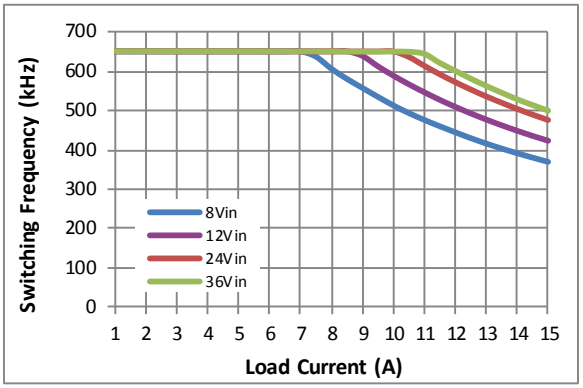
Vout (Ch1) = 1V/Div, Iin (Ch4) = 1A/Div, 800us/Div **331203**

Output Ripple: 24Vin, 2.5Vout at 15A



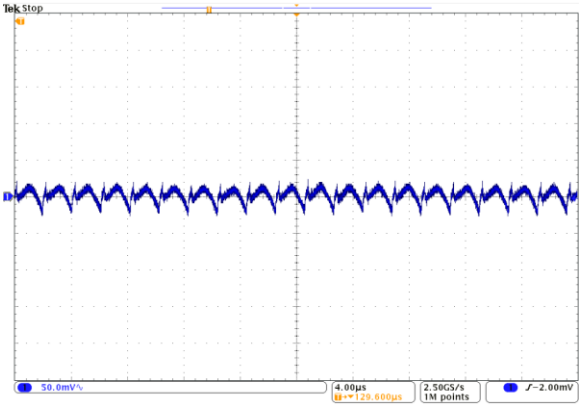
Vout = 50mV/Div, 4.0us/Div, Cout = 8 x 100µF Ceramic **331204**

Switching Frequency vs. Load Current



331205

Output Ripple: 24Vin, 2.5Vout at 7.5A



Vout = 50mV/Div, 4.0us/Div, Cout = 8 x 100µF Ceramic **331206**

PI3301-X1 (3.3 Vout) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, Vin =24V, L1=155nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Specifications						
Input Voltage	V_{IN_DC}	8	24	36	V	Note 7.
Input Current	I_{IN_DC}		2.25		A	Vin = 24V, T_C = 25°C, Iout=15A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}			75	mA	Note 2.
Input Quiescent Current	I_{Q_VIN}		2 2.5		mA	Disabled Enabled (no load)
Input Voltage Slew Rate	V_{IN_SR}			1	V/µs	Note 2.
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	3.25	3.30	3.36	V	Note 2.
Output Voltage Trim Range	V_{OUT_DC}	2.3	3.3	4.1	V	Note 3. Note 7.
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$		0.10		%	@25°C, 8<Vin<36V
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$		0.10		%	@25°C, 0.5A<Iout<15A
Output Voltage Ripple	V_{OUT_AC}		37.5		mVp-p	Iout=5A, Cout=8x100µF, 20MHz BW Note 4.
Continuous Output Current Range	I_{OUT_DC}	0		15	A	Note 2. Note 7.
Current Limit	I_{OUT_CL}		18.0		A	
Protection						
VIN UVLO Start Threshold	V_{UVLO_START}	7.10	7.60	8.00	V	
VIN UVLO Stop Threshold	V_{UVLO_STOP}	6.80	7.25	7.60	V	
VIN UVLO Hysteresis	V_{UVLO_HYS}		0.35		V	
VIN OVLO Start Threshold	V_{OVLO_START}	36.1	37.6		V	
VIN OVLO Stop Threshold	V_{OVLO_STOP}	37.0	38.4		V	
VIN OVLO Hysteresis	V_{OVLO_HYS}		0.8		V	
VIN UVLO/OVLO Fault Delay Time	t_{f_DLY}			128	Cycles	Number of the switching freq cycles
VIN UVLO/OVLO Response Time	t_f		500		ns	
Output Over Voltage Protection	V_{OVP}		20		%	Above V_{OUT}
Over-Temperature Fault Threshold	T_{OTP}	130	135	140	°C	Note 2.
Over-Temperature Restart Hysteresis	T_{OTP_HYS}		30		°C	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33XX evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or Vout is modified.

Note 4: Refer to Output Ripple plots.

Note 5: Refer to Load Current vs. Ambient Temperature curves.

Note 6: Refer to Switching Frequency vs. Load current curves.

PI3301-X1 (3.3 Vout) Electrical Characteristics

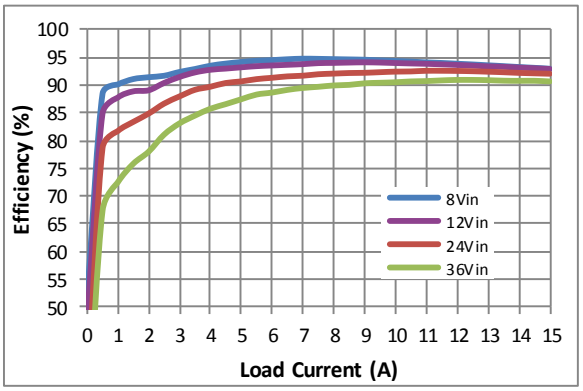
Specifications apply for -40°C < T_J < 125°C, Vin =24V, L1=155nH (Note 1) unless other conditions are noted.

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Timing						
Switching Frequency	f_S		650		kHz	Note 6.
Fault Restart Delay	t_{FR_DLY}		30		ms	
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	50		110	%	Relative to set switching frequency. Note 3.
SYNCI Threshold	V_{SYNCI}		2.5		V	
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	4.5			V	Source 1mA
SYNCO Low	V_{SYNCO_LO}			0.5	V	Sink 1mA
SYNCO Rise Time	t_{SYNCO_RT}		10		ns	20pF load
SYNCO Fall Time	t_{SYNCO_FT}		10		ns	20pF load
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}	0		1.04	V	Internal reference tracking range.
TRK Max Output Voltage	V_{TRK_MAX}		1.2		V	
TRK Disable Threshold	V_{TRK_OV}	20	40	60	mV	
Charge Current (Soft – Start)	I_{TRK}	-70	-50	-30	µA	
Discharge Current (Fault)	I_{TRK_DIS}		6.8		mA	
Soft-Start Time	t_{SS}		2.2		ms	C_{TRK} = 0uF
Enable						
High Threshold	V_{EN_HI}	0.9	1	1.1	V	
Low Threshold	V_{EN_LO}	0.7	0.8	0.9	V	
Threshold Hysteresis	V_{EN_HYS}	100	200	300	mV	
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}		2		V	
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}		0		V	
Source Current	I_{EN_SO}		-50		µA	
Sink Current	I_{EN_SK}		50		µA	

Note 1: All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33XX-X1 evaluation board with 3x4" dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
Note 2: Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.
Note 3: Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or Vout is modified.
Note 4: Refer to Output Ripple plots.
Note 5: Refer to Load Current vs. Ambient Temperature curves.
Note 6: Refer to Switching Frequency vs. Load current curves.
Note 7: Minimum 5V between Vin-Vout must be maintained or a minimum load of 1mA required.

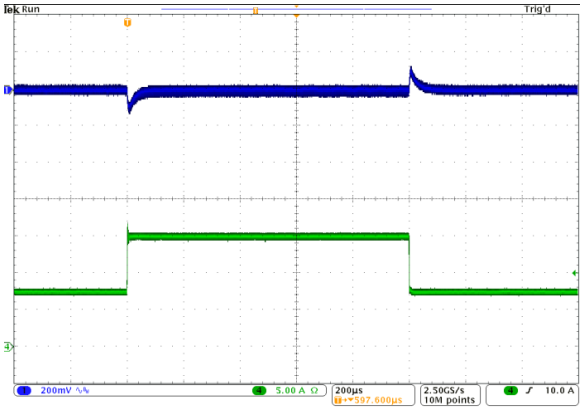
PI3301-X1 (3.3 Vout) Electrical Characteristics

Efficiency at 25°C



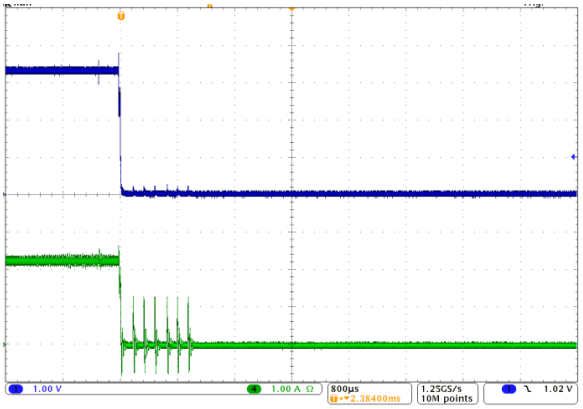
Regulator and inductor performance **330101**

Transient Response: 7.5 to 15A, at 5A/µs



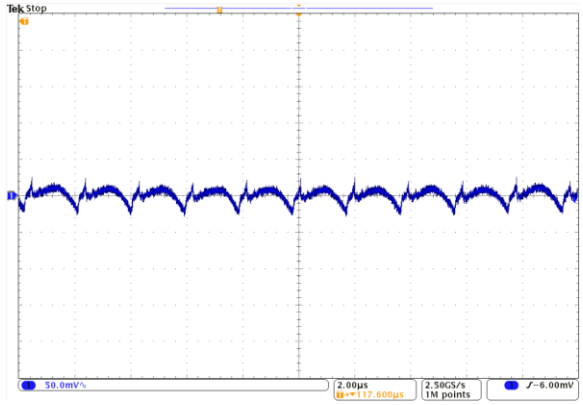
24Vin to 3.3Vout, Cout = 8 x 100µF Ceramic **330102**
Vout (Ch1) = 200mV/Div, Iout (Ch4) = 5A/Div, 200us/Div

Short Circuit



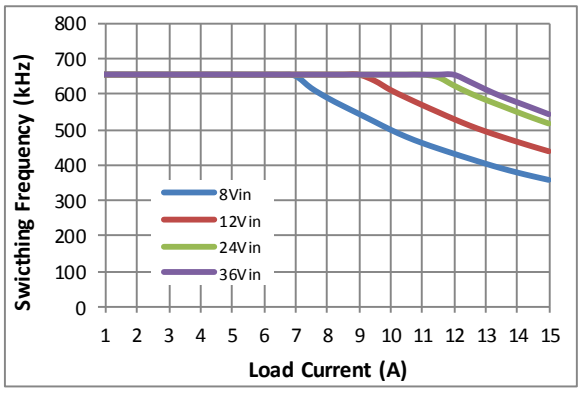
Vout (Ch1) = 1V/Div, Iout (Ch4) = 1A/Div, 800us/Div **330103**

Output Ripple: 24Vin, 3.3Vout at 15A



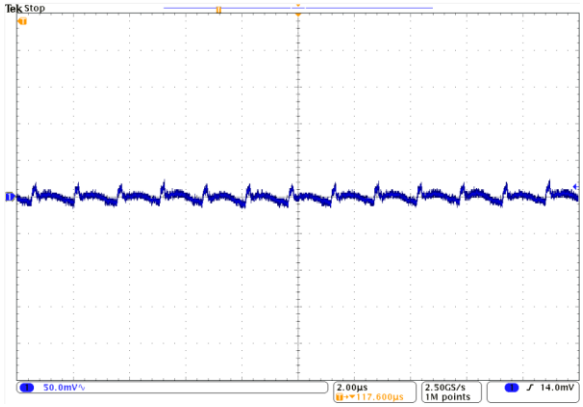
Vout = 50mV/Div, 2.0us/Div, Cout = 8 x 100µF Ceramic **330104**

Switching Frequency vs. Load Current



330105

Output Ripple: 24Vin, 3.3Vout at 7.5A



Vout = 50mV/Div, 2.0us/Div, Cout = 8 x 100µF Ceramic **330106**

Functional Description

The PI33XX-X1 is a family of highly integrated ZVS-Buck regulators. The PI33XX-X1 has a set output voltage that is trimmable within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 5).

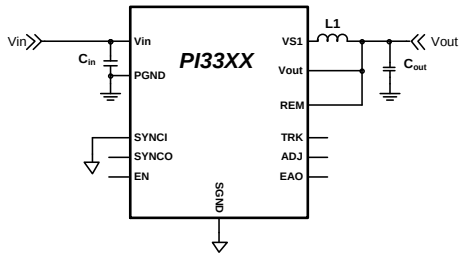


Figure 2 - *ZVS-Buck with required components*

For basic operation, Figure 2 shows the connections and components required. No additional design or settings are required.

ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the converter on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below 0.8 Vdc with respect to SGND will disable the regulator output.

The EN input polarity can be programmed (PI33XX-21 device versions only) via the I^2C data bus. When the EN pin polarity is programmed for negative logic assertion; and if the EN pin is left floating, the regulator output is enabled. Pulling the EN pin above 1.0 Vdc with respect to SGND, will disable the regulator output.

Remote Sensing

An internal 100Ω resistor is connected between REM pin and VOUT pin to provide regulation when the REM connection is broken. Referring to Figure 2, it is important to note that L1 and Cout are the output filter and the local sense point for the power supply output. As such, the REM pin should be connected at Cout as the default local sense connection unless remote sensing to compensate additional distribution losses in the system. The REM pin should not be left floating.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency by an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (f_S). For PI33XX-21 device versions only, the phase delay can be programmed via I^2C bus with respect to the clock applied at SYNCI pin. Phase delay allows PI33XX-X1 regulators to be paralleled and operate in an interleaving mode.

The PI33XX-X1 default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI33XX-X1 devices without the need for further user programming or external sync clock circuitry. The user can change the SYNCI polarity to sync with the external clock rising edge via the I^2C data bus (PI33XX-21 device versions only).

When using the internal oscillator, the SYNCO pin provides a 5V clock that can be used to sync other regulators. Therefore, one PI33XX-X1 can act as the lead regulator and have additional PI33XX-X1s running in parallel and interleaved.

Soft-Start

The PI33XX-X1 includes an internal soft-start capacitor to ramp the output voltage in 2ms from 0V to full output voltage. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, “Soft Start Adjustment and Track,” in the Applications Description section for more details.

Output Voltage Trim

The PI33XX-X1 output voltage can be trimmed up from the preset output by connecting a resistor from ADJ pin to SGND and can be trimmed down by connecting a resistor from ADJ pin to VOUT. The Table 2 defines the voltage ranges for the PI33XX-X1 family.

Device	Output Voltage	
	Set	Range
PI3311-X1-LGIZ	1.0V	1.0 to 1.4V
PI3318-X1-LGIZ	1.8V	1.4 to 2.0V
PI3312-X1-LGIZ	2.5V	2.0 to 3.1V
PI3301-X1-LGIZ	3.3V	2.3 to 4.1V

Table 2 - *PI33XX-X1 family output voltage ranges.*

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Output Current Limit Protection

PI33XX-X1 has two methods implemented to protect from output short or over current condition.

Slow Current Limit protection: prevents the output load from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024us, a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: PI33XX-X1 monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to a sudden low impedance short. If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

Both the Fast and Slow current limit faults are stored in a Fault Register and can be read and cleared (PI33XX-21 device versions only) via I^2C data bus.

Input Under-Voltage Lockout

If VIN falls below the input Under Voltage Lockout (UVLO) threshold, the regulator will enter a low power state and initiate a fault. The system will restart once the input voltage is reestablished and after the Fault Restart Delay. A UVLO fault is stored in a Fault Register and can be read and cleared (PI33XX-21 device versions only) via I^2C data bus.

Input Over Voltage Lockout

If VIN exceeds the input Over Voltage Lockout (OVLO) threshold (V_{OVLO}), while the regulator is running, the PI33XX-X1 will complete the current cycle and stop switching. The system will resume operation after the Fault Restart Delay. The OVLO fault is stored in a Fault Register and can be read and cleared (PI33XX-21 device versions only) via I^2C data bus.

Output Over Voltage Protection

The PI33XX-X1 family is equipped with output Over Voltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay. The OVP fault is stored in a Fault Register and can be read and cleared (PI33XX-21 device versions only) via I^2C data bus.

Over Temperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Over Temperature Protection Threshold (OTP) is exceeded (T_{OTP}), the regulator will complete the current switching cycle, enter a low power mode, set a fault flag, and will soft-start when the internal temperature falls below Over-Temperature Restart Hysteresis (T_{OTP_HYS}). The OTP fault is stored in a Fault Register and can be read and cleared (PI33XX-21 device versions only) via I^2C data bus.

Pulse Skip Mode (PSM)

PI33XX-X1 features a PSM to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

Variable Frequency Operation

Each PI33XX-X1 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 5), to operate at peak efficiency across line and load variations. At low line and high load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

Parallel Operation

Paralleling modules can be used to increase the output current capability of a single power rail and reduce output voltage ripple.

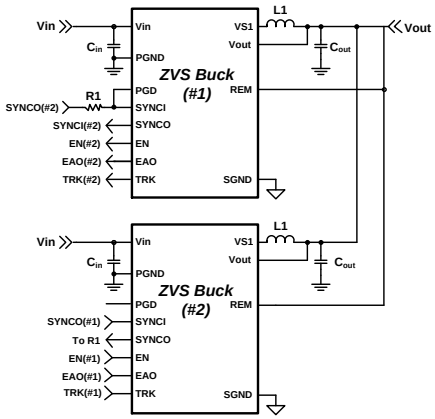


Figure 3 *- PI33XX-X1 parallel operation*

By connecting the EAO pins and SGND pins of each module together the units will share the current equally. When the TRK pins of each unit are connected together, the units will track each other during soft-start and all unit EN pins have to be released to allow the units to start (See Figure 3). Also, any fault event in any regulator will disable the other regulators. The two regulators will be out of phase with each other reducing output ripple (refer to Switching Frequency Synchronization).

To provide synchronization between regulators over the entire operational frequency range, the Parallel Good (PGD) pin must be connected to the lead regulator's (#1) SYNCI pin and a 2.5kΩ Resistor, R1, must be placed between SYNCO (#2) return and the lead regulator's SYNCI (#1) pin, as shown in Figure 3. In this configuration, at system soft-start, the PGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop startup synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to adjust, on the fly, when any of the individual regulators begin to enter variable frequency mode in the loop.

Multi-phasing three regulators is possible (PI33XX-21 only) with no change to the basic single-phase design. For more information about how to program phase delays within the regulator, please refer to Picor application note *PI33XX-2X Multi-Phase Design Guide.*

I²C Interface Operation

PI33XX-21 devices provide an I²C digital interface that enables the user to program the EN pin polarity (from high to low assertion) and switching frequency synchronization phase/delay. These are one time programmable options to the device.

Also, the PI33XX-21 devices allow for dynamic Vout margining via I²C that is useful during development (settings stored in volatile memory only and not retained by the device). The PI33XX-21 also have the option for fault telemetry including:

- Over temperature protection
- Fast/Slow current limit
- Output voltage high
- Input overvoltage
- Input undervoltage

For more information about how to utilize the I²C interface please refer to Picor application note *PI33XX-2X I²C Digital Interface Guide.*

Application Description

Output Voltage Trim

The PI33XX-X1 family of Buck Regulators provides four common output voltages: 1.0V, 1.8V, 2.5V, and 3.3V. A post-package trim step is implemented to offset any resistor divider network errors ensuring maximum output accuracy. With a single resistor connected from the ADJ pin to SGND or REM, each device's output can be varied above or below the nominal set voltage (with the exception of the PI3311-X1 which can only be above the set voltage of 1V).

Device	Output Voltage	
	Set	Range
PI3311-X1-LGIZ	1.0V	1.0 to 1.4V
PI3318-X1-LGIZ	1.8V	1.4 to 2.0V
PI3312-X1-LGIZ	2.5V	2.0 to 3.1V
PI3301-X1-LGIZ	3.3V	2.3 to 4.1V

Table 3 *- PI33XX-X1 family output voltage ranges*

The remote pin (REM) should always be connected to the VOUT pin, if not used, to prevent an output voltage offset. Figure 4 shows the internal feedback voltage divider network.

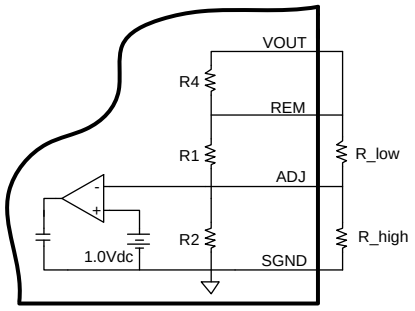


Figure 4 *- Internal resistor divider network*

R1, R2, and R4 are all internal 1.0 % resistors and R_low and R_high are external resistors for which the designer can add to modify VOUT to a desired output. The internal resistor value for each regulator is listed below in Table 4.

Device	R1	R2	R4
PI3311-X1-LGIZ	1k	Open	100
PI3318-X1-LGIZ	0.806k	1.0k	100
PI3312-X1-LGIZ	1.5k	1.0k	100
PI3301-X1-LGIZ	2.61k	1.13k	100

Table 4 *- PI33XX-X1 Internal divider values*

By choosing an output voltage value within the ranges stated in Table 3, VOUT can simply be adjusted up or down by selecting the proper R_high or R_low value, respectively. The following equations can be used to calculate R_high and R_low values:

$$R_{high} = \frac{1}{\frac{(Vout-1)}{R1} - \left(\frac{1}{R2}\right)} \qquad (1)$$

$$R_{low} = \frac{1}{\frac{1}{R2(Vout-1)} - \left(\frac{1}{R1}\right)} \qquad (2)$$

If, for example, a 4.0V output is needed, the user should choose the regulator with a trim range covering 4.0V from Table 3. For this example, the PI3301 is selected (3.3V set voltage). First step would be to use Equation (1) to calculate R_high since the required output voltage is higher than the regulator set voltage. The resistor-divider network values for the PI3301 are can be found in Table 4 and are R1=2.61kΩ and R2=1.13kΩ. Inserting these values in to Equation (1), R_high is calculated as follows:

$$3.78k = \frac{1}{\frac{(4.0-1)}{2.61k} - \left(\frac{1}{1.13k}\right)}$$

Resistor R-high would be connected as in Figure 4 to achieve the 4.0V regulator output. No R_low resistor would be used since in this example the trim is above the regulator set voltage.

The PI3311-X1 output voltage can only be trimmed higher than the factory 1V setting. The following

equation (3) can be used to calculate R_{high} values for the PI3311-X0 regulators.

$$R_{high(1V)} = \frac{1}{\frac{(Vout - 1)}{1}} \qquad (3)$$

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal capacitor and a fixed charge current to provide a Soft-Start Time t_{SS} for all PI33XX-X1 regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = (t_{TRK} \times I_{TRK}) - 100x10^{-9},$$

Where, t_{TRK} is the soft-start time and I_{TRK} is a 50uA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at startup, simply connect all devices TRK pins together. This type of tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 5 (a)).

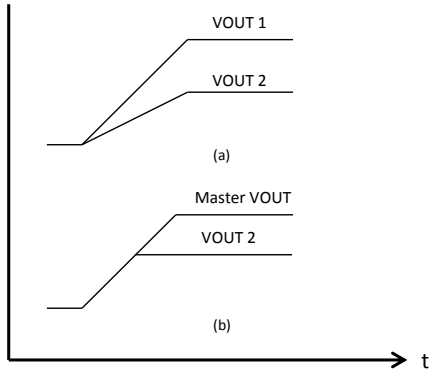


Figure 5 - *PI33XX-X1 tracking methods*

For Direct Tracking, choose the regulator with the highest output voltage as the master and connect the master to the TRK pin of the other regulators through a divider (Figure 6) with the same ratio as the slave's feedback divider (see Table 4 for values).

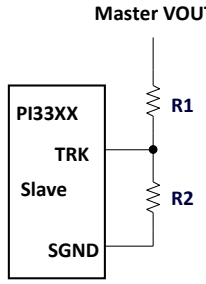


Figure 6 - *Voltage divider connections for direct tracking*

All connected regulators' soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 5 (b). All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI33XX-X1 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 5 details the specific inductor value and part number utilized for each PI33XX-X1 device which are manufactured by Eaton.Data sheets are available at http://www.cooperindustries.com.

Device	Inductor [nH]	Inductor Part Number	Manufacturer
PI3311-X1	85	FPV1006-85-R	Eaton
PI3318-X1	125	FPV1006-125-R	Eaton
PI3312-X1	125	FPV1006-125-R	Eaton
PI3301-X1	150	FPV1006-150-R	Eaton

Table 5 - *PI33XX-X1 Inductor pairing*

Layout Guidelines

To optimize maximum efficiency and low noise performance from a PI33XX-X1 design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 9. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

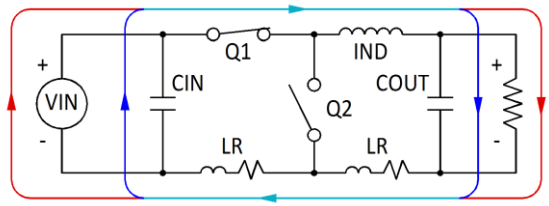


Figure 9 *- Typical Buck Converter*

The path between the COUT and CIN capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on. Figure 10, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI33XX-X1 performance.

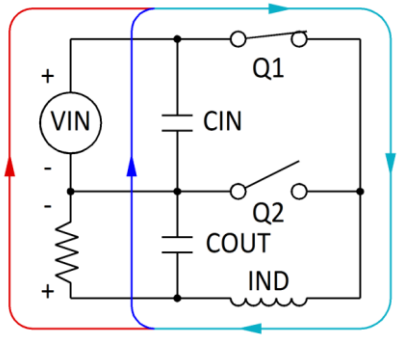


Figure 10 *- Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of CIN's current is used to satisfy the output load and to recharge the COUT capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the COUT capacitor as shown in Figure 11. During this period CIN is also being recharged by the VIN. Minimizing CIN loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the CIN loop and COUT loop is vital to minimize switching and GND noise.

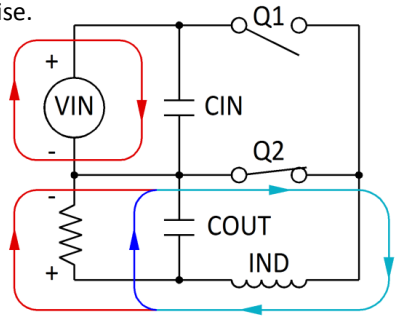


Figure 11 *- Current flow: Q2 closed*

The recommended component placement, shown in Figure 12, illustrates the tight path between CIN and COUT (and VIN and VOUT) for the high AC return current. This optimized layout is used on the PI33XX-X1 evaluation board.

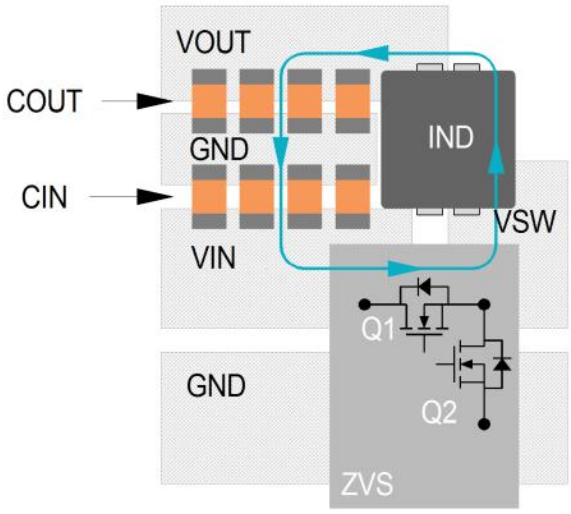


Figure 12 *- Recommended component placement and metal routing*

Recommended PCB Footprint and Stencil

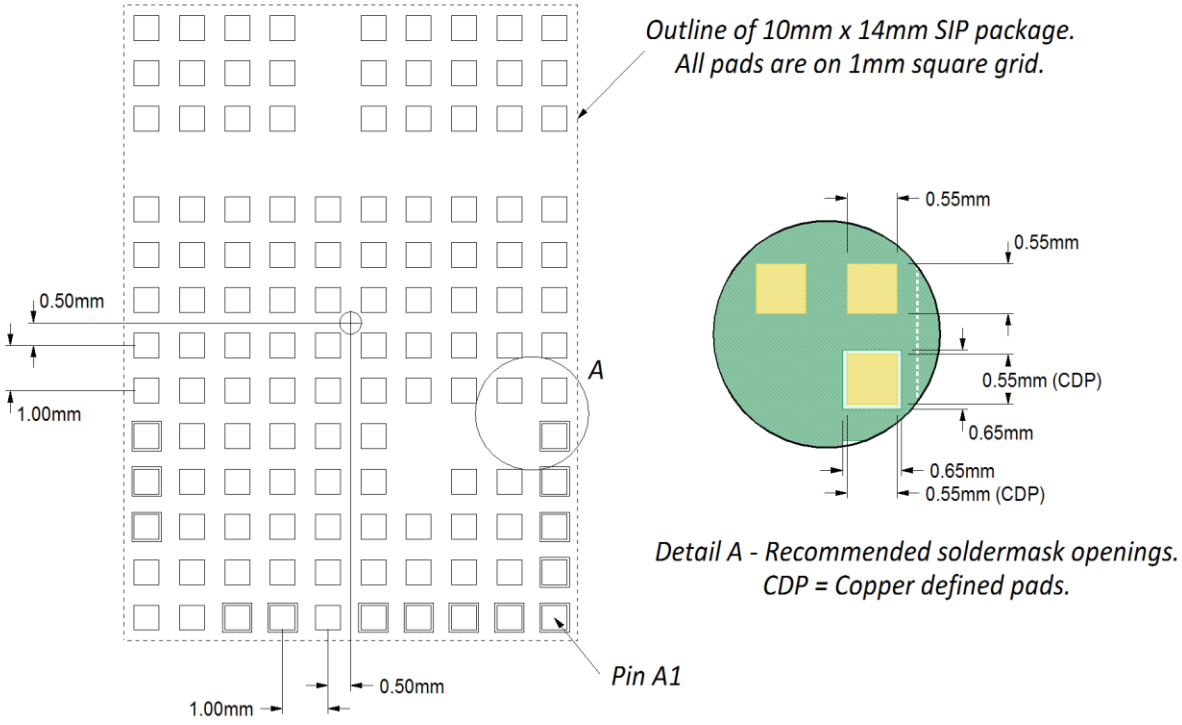
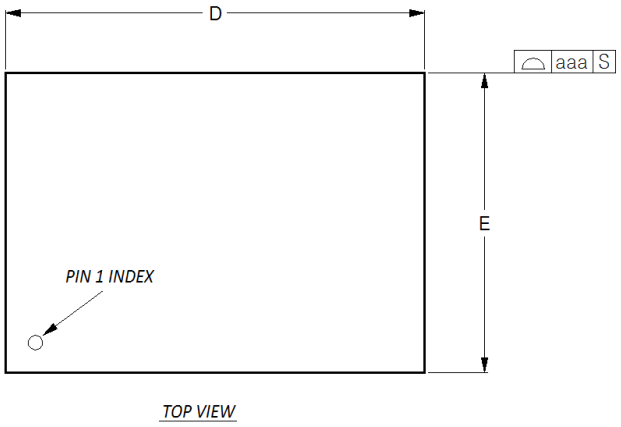


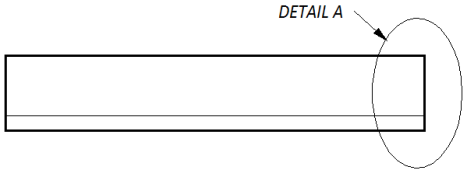
Figure 13 *- Recommended Receiving PCB footprint.*

Figure ***13***3 details the recommended receiving footprint for PI33XX-X1 10mm x 14mm package. All pads should have a final copper size of 0.55mm x 0.55mm, whether they are solder-mask defined or copper defined, on a 1mm x 1mm grid. All stencil openings are 0.55mm when using a 6mil stencil.

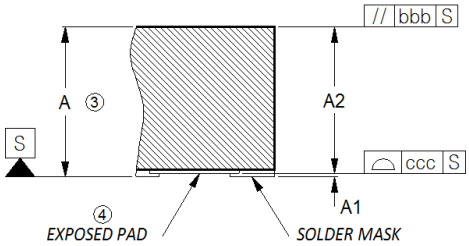
Package Drawings



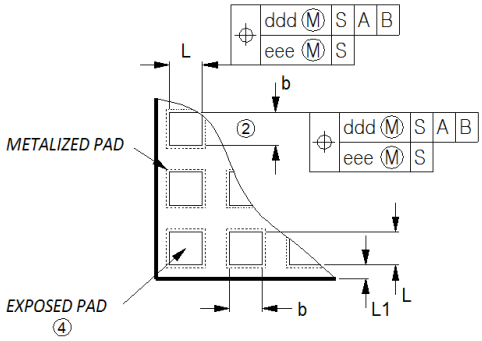
TOP VIEW



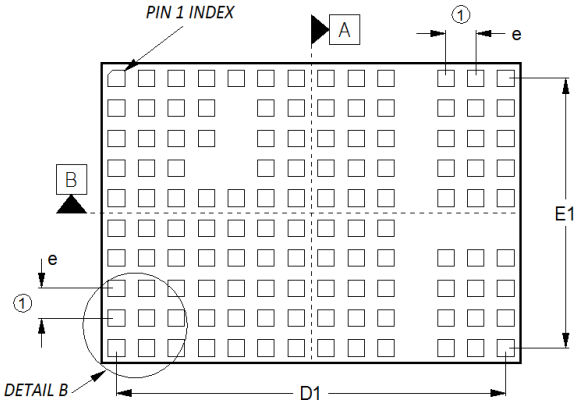
SIDE VIEW



DETAIL A



DETAIL B



BOTTOM VIEW

DIMENSIONAL REFERENCES

REF.	Min.	Nom.	Max.
A	2.50	2.56	2.62
A1	--	--	0.05
A2	--	--	2.57
b	0.50	0.55	0.60
L	0.50	0.55	0.60
D		14.00 BSC	
E		10.00 BSC	
D1		13.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	
L1	0.10	0.15	0.20
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.08

Notes :

① *'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.*

② *DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURE BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.*

③ *DIMENSION 'A' INCLUDES PACKAGE WARPAGE.*

④ *EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.*

5. *ALL DIMENSIONS ARE IN MILLIMETERS.*

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