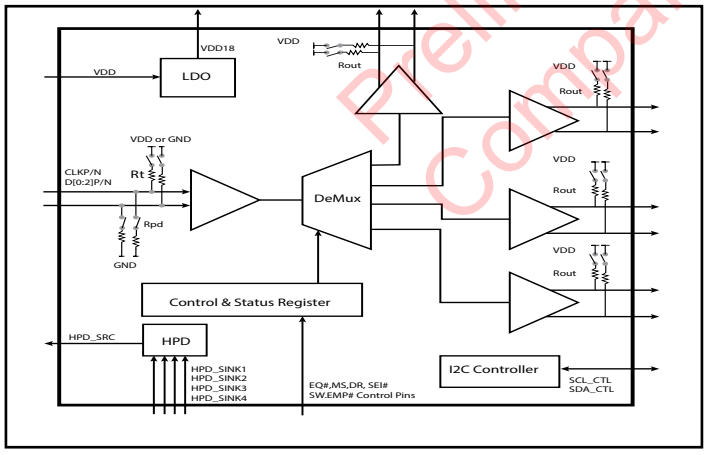
HDMI 1.4b Splitter 1:4 for 3.4 Gbps Data Rate with Equalization & Pre-emphasis

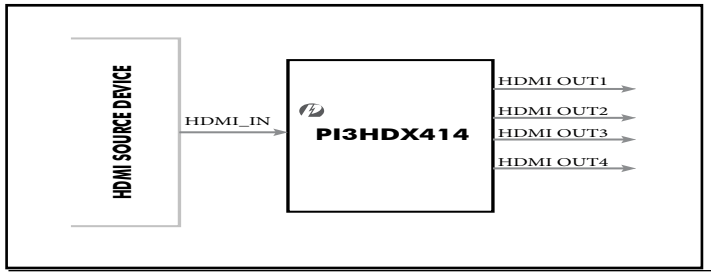
Feature

- ➔ Support up to 3.4 Gbps Serial Link
- ➔ HDMI1.4b 1-to-4 Active Splitter and Demux with TMDS clock Frequencies up to 340 MHz
- ➔ AC and DC coupled Differential Signaling Input
- ➔ Configurable TMDS Output Signal Conditioning Setting for Port Selection, Pre-emphasis, Voltage Swing, Slew Rate Setting
- ➔ Highly Configurable Receiver Equalization Setting up to 20dB
- ➔ Support Receiver Squelch mode with clock channel detector
- ➔ Support HPD_SINK signal detection for active source ports management
- ➔ Support Pin strap and I^2C programming for Control Status Register
- ➔ ESD protection on I/O pins to connector: 8KV contact per IEC6100-4-2 and 2KV HBM
- ➔ Supply Voltage: 3.3V±5%
- ➔ Industrial Temperature Range: -40°C to 85°C
- ➔ Packaging (Pb-free & Green): LQFP80 (FCE80)

Block Diagram



Typical Application



Description

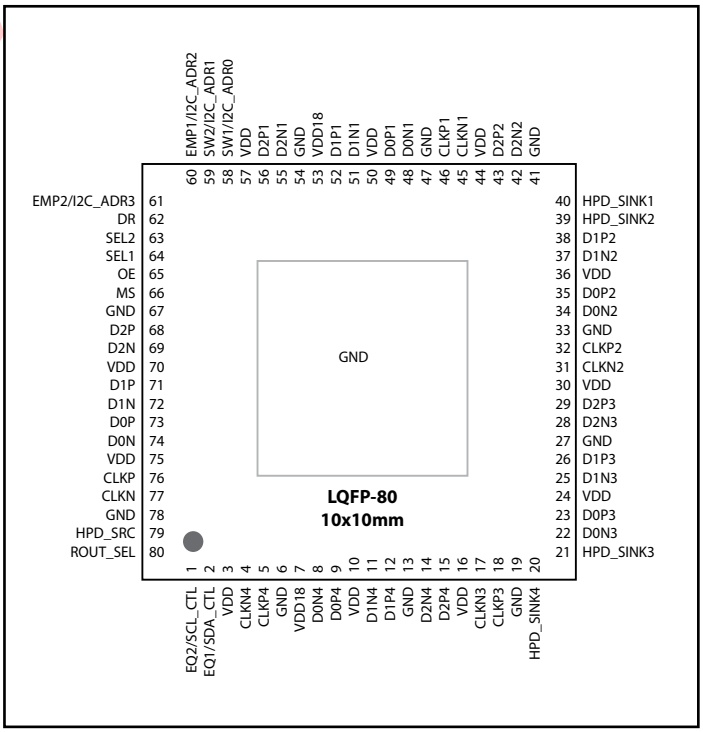
The device provides HDMI 1.4b 1-to-4 Splitter and Demux with 3.4 Gbps data rate support. Signal conditioning features are programmable equalization, output voltage swing and pre-emphasis by setting with pin strapping option or I^2C control, to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the high speed Demux, whereas the integrated pre-emphasis circuitry provides flexibility with signal integrity of the signal after the ReDriver.

Application

- ➔ HDMI Peripherals
- ➔ Wall Multi Screen Display
- ➔ Notebook PC and Docking
- ➔ TV, Monitor and Set-Top-Box

Pin Configuration (Top-Side View)



Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
77 76 74 73 72 71 69 68	CLKN CLKP D0N D0P D1N D1P D2N D2P	I	TMDS inputs. Rt = 50 Ohm; Rpd = 200 kOhm.
45 46 48 49 51 52 55 56	CLKN1 CLKP1 D0N1 D0P1 D1N1 D1P1 D2N1 D2P1	O	Port 1 TMDS outputs. Rout = 50 Ohm by control.
31 32 34 35 37 38 43 44	CLKN2 CLKP2 D0N2 D0P2 D1N2 D1P2 D2N2 D2P2	O	Port 2 TMDS outputs. Rout = 50 Ohm by control.
17 18 22 23 25 26 28 29	CLKN3 CLKP3 D0N3 D0P3 D1N3 D1P3 D2N3 D2P3	O	Port 3 TMDS outputs. Rout = 50 Ohm by control.
4 5 8 9 11 12 14 15	CLKN4 CLKP4 D0N4 D0P4 D1N4 D1P4 D2N4 D2P4	O	Port 4 TMDS outputs. Rout = 50 Ohm by control.

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Control Signals</td></tr>
<tr><td>1</td><td>EQ2/SCL_CTL</td><td>IO</td><td>Shared Pin for EQ or I²C Clock, compatible with I²C-Bus specification up to 400kb/s.
<table>
<tr><td>EQ2/SCL_CTL</td><td>Functional Description</td></tr>
<tr><td>MS = "High"</td><td>Assign to SCL_CTL Pin</td></tr>
<tr><td>MS = "Low"</td><td>Assign to EQ2 Pin</td></tr>
</table>
Internal Pull-up at 100 kOhm and Pull-Down at 100 kOhm. Pin Control EQ mode setting is below. "M" is Tri-state.
<table>
<tr><th>MS
(Pin# 1)</th><th>EQ2/SCL_CTL
(Pin# 19)</th><th>EQ1/SDA_CTL
(Pin# 20)</th><th>Equalization Setting
(dB)</th></tr>
<tr><td rowspan="8">"Low"</td><td>0</td><td>M</td><td>2.5</td></tr>
<tr><td>0</td><td>0</td><td>5</td></tr>
<tr><td>M</td><td>0</td><td>7.5</td></tr>
<tr><td>0</td><td>1</td><td>10</td></tr>
<tr><td>M</td><td>M</td><td>12.5</td></tr>
<tr><td>1</td><td>0</td><td>15</td></tr>
<tr><td>1</td><td>M</td><td>17.5</td></tr>
<tr><td>1</td><td>1</td><td>20</td></tr>
</table></td></tr>
<tr><td>2</td><td>EQ1/SDA_CTL</td><td>IO</td><td>Shared Pin for EQ1 or I²C Data, compatible with I2C-Bus specification, up to 400 kb/s. Internal Pull-Up at 100 kOhm and Pull-Down at 100 kOhm. Please refer to Pin# 1 Control EQ mode setting table above.</td></tr>
<tr><td>58
59
60
61</td><td>SW1/I2C_ADR0
SW2/I2C_ADR1
EMP1/I2C_ADR2
EMP2/I2C_ADR3</td><td>I</td><td>Shared Pin for SW/EMP or I²C Address. When MS = "High", pins are assigned as I²C Address Pins; When MS = "Low", pins are assigned as Pin control mode.
<table>
<tr><td>Pin# 58,59,60,61</td><td>Function Description</td></tr>
<tr><td>"High"</td><td>Assign as I²C_ADR[3:0]</td></tr>
<tr><td>"Low"</td><td>Assign as SW1,SW2, EMP1, EMP2 for Pin Control Mode</td></tr>
</table>
SW2 and SW1 for voltage swing control, internal Pull-Up at 100 kOhm.
<table>
<tr><th>SW2</th><th>SW1</th><th>Voltage Swing</th></tr>
<tr><td>0</td><td>0</td><td>500 mV</td></tr>
<tr><td>0</td><td>1</td><td>-10 %</td></tr>
<tr><td>1</td><td>0</td><td>+10 %</td></tr>
<tr><td>1</td><td>1</td><td>+20 %</td></tr>
</table>
EMP2 and EMP1 pin configuration for pre-emphasis control are shown below. These pins are internally Pull-Up at 100 kOhm.
<table>
<tr><th>EMP2</th><th>EMP1</th><th>Pre-emphasis Setting (dB)</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1.5</td></tr>
<tr><td>1</td><td>0</td><td>2.5</td></tr>
<tr><td>1</td><td>1</td><td>3.5</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>66</td><td>MS</td><td>I</td><td>Mode Selection Pin. Internal Pull-Up with 100 kOhm.
<table>
<tr><td>MS</td><td>Functional Description</td></tr>
<tr><td>"High"</td><td>I²C Control Mode</td></tr>
<tr><td>'Low"</td><td>Pin Control Mode</td></tr>
</table></td></tr>
<tr><td>80</td><td>Rout_SEL</td><td>I</td><td>Source Termination Selection Pin. Internal pull-up at 100 kOhm.
<table>
<tr><td>ROUT_SEL</td><td>Functional Description</td></tr>
<tr><td>"High"</td><td>Source Termination Output in TX side</td></tr>
<tr><td>"Low"</td><td>Open Drain Output in TX side</td></tr>
</table></td></tr>
<tr><td>65</td><td>OE</td><td>I</td><td>Output Enable Control Pin. Active high. Internal pull-up at 100 kOhm.
<table>
<tr><td>OE</td><td>Functional Description</td></tr>
<tr><td>"High"</td><td>Output Enable</td></tr>
<tr><td>"Low"</td><td>Turn off Rout and R_T (Termination Resistor), disabling TMDS Rx and TMDS Tx block</td></tr>
</table></td></tr>
<tr><td>62</td><td>DR</td><td>I</td><td>Direction Control Pin. When DR = "High", all ports are active at same time. DR = "Low", Output ports are controlled by SEL2 (Pin#64) and SEL1 (Pin#63).</td></tr>
<tr><td>64
63</td><td>SEL1
SEL2</td><td>I</td><td>Port Selection Pins. Internal pull-up at 100 kOhm.
<table>
<tr><td>SEL2</td><td>SEL1</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>Port 1 is Active</td></tr>
<tr><td>0</td><td>1</td><td>Port 2 is Active</td></tr>
<tr><td>1</td><td>0</td><td>Port 3 is Active</td></tr>
<tr><td>1</td><td>1</td><td>Port 4 is Active</td></tr>
</table></td></tr>
<tr><td>40
39
21
20</td><td>HPD_SINK1
HPD_SINK2
HPD_SINK3
HPD_SINK4</td><td>I</td><td>Sink-side Hot Plug Detect Pins</td></tr>
<tr><td>79</td><td>HPD_SRC</td><td>O</td><td>Source-side Hot Plug Detect Pin</td></tr>
<tr><td colspan="4">Power Pins</td></tr>
<tr><td>3,10,16,24,30
36,44,50,57,70
75</td><td>VDD</td><td>PWR</td><td>3.3V Power Supply Pins</td></tr>
<tr><td>7, 53</td><td>VDD18</td><td>PWR</td><td>LDO Output Pin for internal core supplier. Add external 4.7 uF capacitor to GND</td></tr>
<tr><td>6,13,19,27,33,
42,47,54,67,78</td><td>GND</td><td>GND</td><td>Ground Pins</td></tr>
</table>

Description of Operation

Output Disable (Squelch) Mode:

Output Disable (Squelch) Mode uses CLK channel signal detection. When low-signal levels on the source TMDS (Main Link) input are sensed(a squelch event), a transition to this state occurs and TMDS D [0:2]P/N signals are disable; when the source TMDS(Main Link) input signal levels are above a pre-determined threshold, a transition back to the appropriate active mode occurs.

In squelch state, TMDS output is set to "high impedance at TMDS open drain output" or "pull-up to VDD by internal 50 Ohm resistor at TMDS double termination output".

Squelch is enabled as default setting. Enable squelch mode means input termination resistor is enabled. When squelch is disable in RX_SET[1]="1", TMDS D[0:2]P/N will be unknown during no TMDS input signals.

Source Connection Detector Mode:

Default is "enable connector detector" and can be disabled by I2C Register Offset 0x00 CONFIG[2] = "0". When HPD_SINKx (x=1,2,3,4) = "Low" signal, the port has no HDMI connector inserted in and will disable the port. When all of ports do not have HDMI connector inserted, TMDS input 50 Ohm will turn off also. In standby mode, source connection detector mode is under operation.

I^2C Register Control

Pin Name	I/O	Description
SCL_CTL	I	I^2C Clock, compatible with I2C-bus specification, up to 400 kb/s
SDA_CTL	IO	I^2C Data, compatible with I2C-bus specification, up to 400 kb/s
I2C_ADR0/1/2/3	I	I^2C control address setting
Byte output : 0x00 - 0x07	O	I^2C control registers output (there are 10 Byte register in base)

I^2C Address Byte

	b[7] MSB	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (R/W)
Address Byte	1	0	1	A3	A2	A1	A0	1/0*

* Read "1", Write "0"

I²C Control Register

<table>
<tr><th>Offset</th><th>Name</th><th>Description</th><th>Power Up Condition</th><th>Type</th></tr>
<tr><td>0x00</td><td>CONFIG[7:0]</td><td>[7] Enable Standby
"0": Standby mode
"1": Normal mode
In standby mode, TMDS equalizer and output driver are powered down.
[6] Port 1 is selected
"0" : Disable
"1" : Active
[5] Port 2 is selected
"0" : Disable
"1" : Active
[4] Port 3 is selected
"0" : Disable
"1" : Active
[3] Port 4 is selected
"0" : Disable
"1" : Active
[2] Source connection detector enable
"0" : Disable source connection detector
"1" : Enable connection detector (as default)
When this port no connector as HPD_SINKx = "Low", the port will be no active. When four of ports do not inserted any connectors, it will turn off TMDS input 50 Ohm
[1:0] Reserved</td><td>0xFF</td><td>R/W</td></tr>
<tr><td>0x01</td><td>RX_SET[7:0]</td><td>Receiver Equalization setting
[7] Disable port termination resistors
"0" = Rpd connected
"1" = Rpd disconnected
[6] TMDS input termination V-bias selection
"0" : Connect to GND (default)
"1" : Connect to VDD
[5] V-bias register selection enable
"0" : b[6] control disable (as default, pin control only)
"1" : b[6] control enable
[4:2] EQ programmable setting
<table><tr><th>b[4:2]</th><th>EQ Setting (dB)</th></tr><tr><td>000</td><td>2.5</td></tr><tr><td>001</td><td>5</td></tr><tr><td>010</td><td>7.5</td></tr><tr><td>011</td><td>10</td></tr><tr><td>100</td><td>12.5</td></tr><tr><td>101</td><td>15</td></tr><tr><td>110</td><td>17.5</td></tr><tr><td>111</td><td>20</td></tr></table>[1] Squelch disable
"0" : Squelch enable (as default)
"1" : Squelch disable
[0] Reserved</td><td>0x00</td><td>R/W</td></tr>
</table>

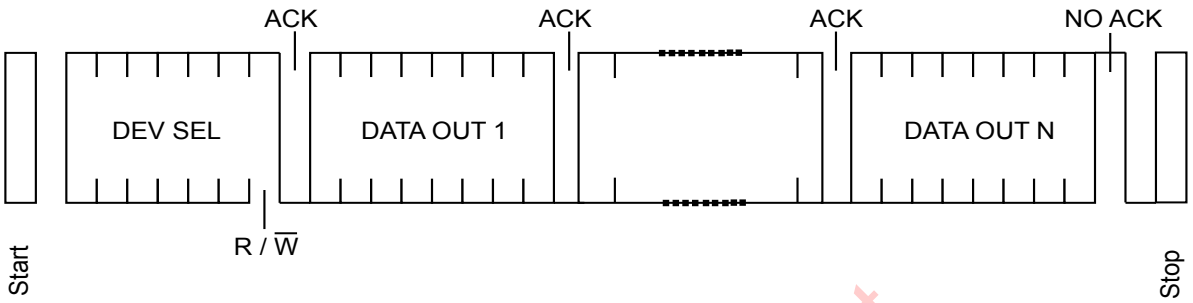
Offset	Name	Description	Power Up Condition	Type
0x02	TX_SET[7:0] for Port 1	TMDS output setting [7] TMDS output control "0" : Open drain "1" : Double termination [6:4] TMDS output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011" : 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] Reserved by test adjust TMDS output swing setting "00" : 500 mV as default setting "01" : -10% "10" : +10% "11" : +20% [1:0] Reserved by test adjust TMDS output slew rate setting "00" : Default setting "01"/"10" : + 5% "11" : +10%	0x00	R/W
0x03	TX_SET[7:0] for Port 2	TMDS Output Setting [7] TMDS output control "0" : Open drain "1" : Double termination [6:4] TMDS output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011" : 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] Reserved by test only TMDS output swing setting "00" : 500mV as default "01" : -10% "10" : +10% "11" : +20% [1:0] Reserved by test adjust TMDS output slew rate setting "00" : Default Setting "01"/"10" : + 5% "11" : +10%	0x00	R/W

Offset	Name	Description	Power Up Condition	Type
0x04	TX_SET[7:0] for Port 3	TMDS Output Setting [7] TMDS output control "0" : Open drain "1" : Double termination [6:4] TMDS output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011": 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] Reserved by test only TMDS output swing setting "00" : 500mV as default "01" : -10% "10" : +10% "11" : +20% [1:0] Reserved by test adjust TMDS output slew rate setting "00" : Default Setting "01" : +5% "10" : + 5% "11" : +10%	0x00	R/W
0x05	TX_SET[7:0] for port4	TMDS Output Setting [7] TMDS output control "0" : Open drain "1" : Double termination [6:4] TMDS output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011" : 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] Reserved by test only TMDS output swing setting "00" : 500 mV as default "01" : -10% "10" : +10% "11" : +20% [1:0] Reserved by test adjust TMDS output slew rate setting "00" : Default Setting "01"/"10" : + 5% "11" : +10%	0x00	R/W

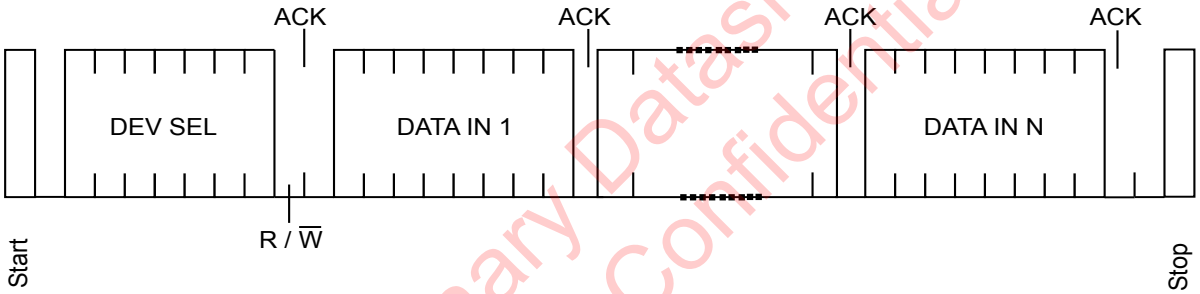
Offset	Name	Description	Power Up Condition	Type
0x06	HPD_SINKx[7:0]	[7] HPD_SRC output logic function (with external 1 kOhm pull-up resistor) "1" : HPD_SRC = /HPD_SINKx "0" : HPD_SRC = HPD_SINKx [6:4] Reserved b[3] : HPD_SINK4 status as read only b[2] : HPD_SINK3 status as read only b[1] : HPD_SINK2 status as read only b[0] : HPD_SINK1 status as read only	0x00	R/W
0x07	Reserved	[7:0] Reserved	0x00	R/W

I²C Data Transfer

1. Read Sequence



2. Write Sequence



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential 3.6V
DC SIG Voltage . . . . . –0.5V to V_{DD}+0.5V
DC Output Current . . . . . TBD
Power Dissipation Continuous . . . . . TBD
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . -40 to +85°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Specifications (VDD=3.3V +/- 10%)

	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Operation Voltage		3.0	3.3	3.6	V
I_{DD}	V_{DD} Supply Current			TBD		mA
I_{DDQ}	V_{DD} Quiescent Current	OE = 1, No input signal		15		mA
I_{STB}	Standby mode	OE = 0		6		mA
TMDS Differential Pins						
V_{OH}	Single-ended high level output voltage	V_{DD} = 3.3 V, Rout=50 Ω	V_{DD}-10		V_{DD}+10	mV
V_{OL}	Single-ended low level output voltage		V_{DD}-600		V_{DD}–400	mV
Vswing	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage				180	mV
$V_{OD(U)}$	Undershoot of output differential voltage				200	mV
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				5	mV
I_{OS}	Short Circuit output current		-12		12	mA
I_{OS}	Short Circuit output current at double termination mode		-24		24	mA
VI(open)	Single-ended input voltage under high impedance input or open input	I_L = 10 uA	V_{DD}-10		V_{DD}+10	mV
R_T	Input termination resistance	V_{IN} = 2.9 V	45	50	55	Ohm
I_{OZ}	Leakage current with Hi-Z I/O	V_{DD} = 3.6 V, OE = 0		30	100	µA

HPD_SINKx(5V tolerance)						
I_{IH}	High level digital input current	$V_{IH} = V_{DD}$	-10		50	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage	V_{DD} = 3.3 V	2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
Control pins (OE, SEL,EMP,SW,MS)						
I_{IH}	High level digital input current	$V_{IH} = V_{DD}$	-10		10	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-50		10	µA
V_{IH}	High level digital input voltage		2.4			V
V_{IL}	Low level digital input voltage		0		0.8	V

AC Specifications

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
TMDS Differential Pins						
t_{pd}	Propagation delay	V_{DD} = 3.3 V, R_{OUT} = 50 Ohm			2000	ps
t_r	Differential output signal rise time (20% - 80%), 0 dB / Open drain			140		ps
t_f	Differential output signal fall time (20% - 80%), 0 dB / Open drain			140		ps
$t_{sk(p)}$	Pulse Skew			15	50	ps
$t_{sk(D)}$	Intra-pair Differential Skew			25	50	ps
$t_{sk(O)}$	Inter-pair Differential Skew				100	ps
t_{SX}	Select to switch output				50	ns
t_{en}	Enable Time				600	ns
t_{dis}	Disable Time				50	ns
$t_{jit\_clk(pp)}$	Peak-to-peak output jitter CLK residual jitter	Data: 3.4 Gb data pattern Clock: 340 MHz		TBD		ps
$t_{jit\_data(pp)}$	Peak-to-peak output jitter Date residual jitter			TBD		ps
DDC I/O Pins (HPD_SINK)						
$t_{pd(HPD)(tphl)}$	Propagation Delay (from active port HPD_SINK to HPD_SRC)	C_L = 10 pF		2	6.0	ns
$t_{pd(HPD)(tphl)}$	Switching Time (from port select to the latest)			3	6.5	ns

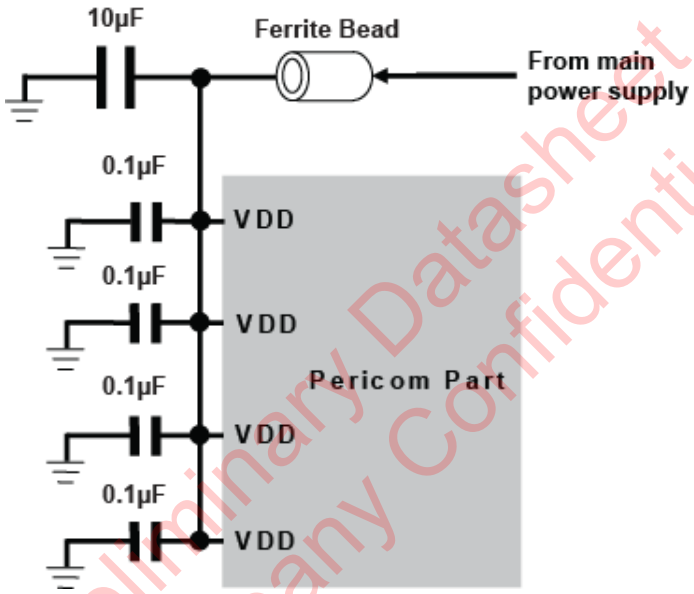
Note

1. Overshoot of output differential voltage $V_{OD(O)} = (V_{SWING(MAX)} * 2) * 15\%$
2. Undershoot of output differential voltage $V_{OD(O)} = (V_{SWING(MIN)} * 2) * 25\%$

Recommended System Design for Power Supply

Power Supply Decoupling Circuit

It is recommended to put 0.1 µF decoupling capacitors on each VDD pins of our part, there are four 0.1 µF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericom parts, the number of 0.1 µF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1 µF decoupling capacitors on each VDD pins, it is recommended to put a 10 µF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.



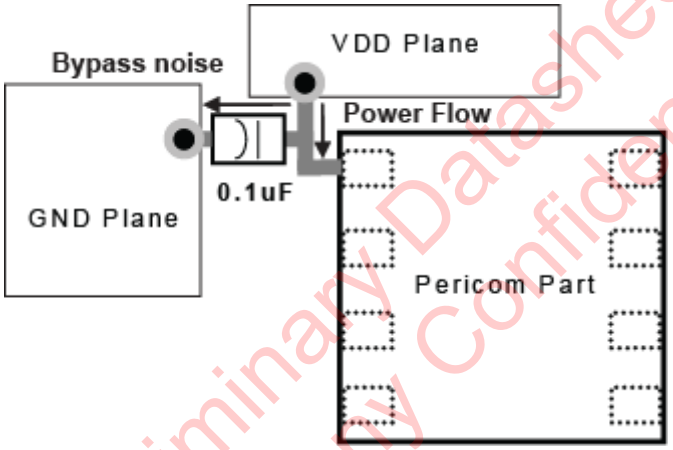
Recommended Power Supply Decoupling Capacitor Diagram

Requirements on the De-coupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

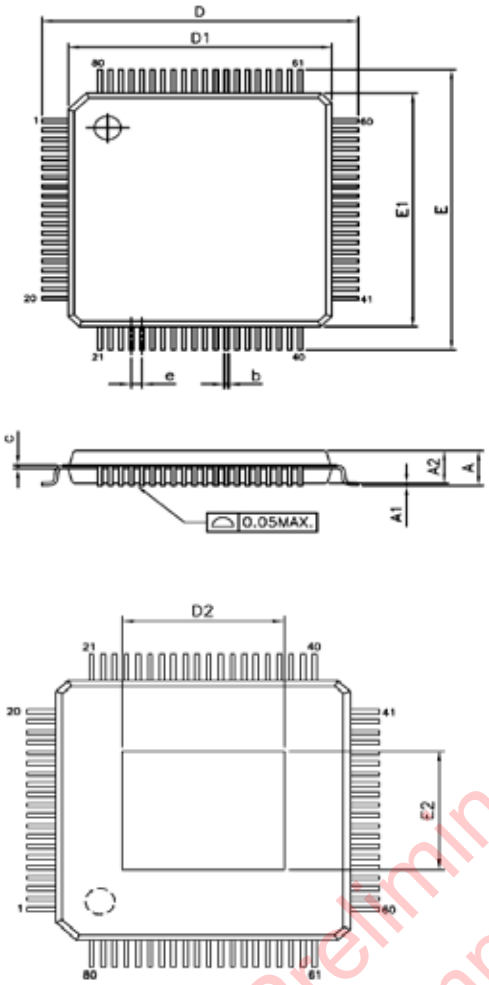
Layout and Decoupling Capacitor Placement Consideration

- ➔ Each 0.1 µF decoupling capacitor should be placed as close as possible to each VDD pin.
- ➔ VDD and GND planes should be used to provide a low impedance path for power and ground.
- ➔ Via holes should be placed to connect to VDD and GND planes directly.
- ➔ Trace should be as wide as possible
- ➔ Trace should be as short as possible.
- ➔ The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- ➔ 10 µF Capacitor should also be placed closed to our part and should be placed in the middle location of 0.1 µF capacitors.
- ➔ Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.



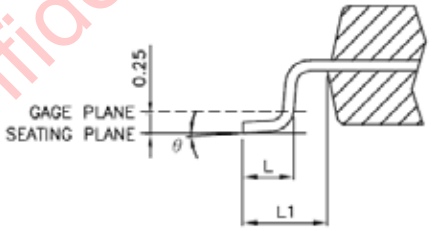
Decoupling Capacitor Placement Diagram

Package Mechanical: 80-pad, LQFP(Low Profile Quad Flat Package) Package Code: FCE80



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
D2	4.71	--	5.54
E2	3.88	--	4.57
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



Notes:
1 All dimensions are in millimeters, angles in degrees
2 Ref JEDEC: MS-026/BCE
3 Package outline exclusive of mold flash and metal burr

Note:
• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDX414FCEE	FCE80(EPAD)	Low Profile Flat Package

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel

Related Products

Part Number	Product Description
PI3HDX412BD/BO	HDMI 1.4b Splitter 1:4 with Signal Conditioning for 3.4Gb Application
PI3HDMI511A	HDMI 1.4b Redriver and DP++ Level Shifter for Source 3.4Gb Application
PI3WVR12412	Wide Voltage Range DP & HDMI Video Switch for 6 Gb application
PI3HDX1204-A	HDMI 2.0 ReDriver for Source 6Gb Application
PI3EQXDP1201	DisplayPort 1.2 ReDriver with built-in AUX listener
PI3HDMI521	HDMI 1.4b 2-to-1 Switch with Signal Conditioning for Source-side 3.4Gb Application
PI3VDP3212	2-Lane DisplayPort 1.2 Compliant Switch
PI3VDP12412	4-Lane DisplayPort 1.2 Compliant Switch
PI3HDMI412AD	HDMI 1-to-2 Splitter with Signal Conditioning for 2.5Gb Application
PI3HDMI336	HDMI 3-to-1 Switch with Signal Conditioning for 2.5Gb Application