A product Line of
Diodes Incorporated

PI3HDX711B

HDMI 1.4b 3.4Gbps Retimer Jitter Cleaner

with DP++ Level Shifter, Cable ID, DDC Buffer/Switch

Description

PI3HDX711B is the HDMI 3.4Gbps Data Rate compliant Retimer that removes both data and clock jitter, and outputs jitter-cleaned TMDS signals, supporting 4K2K resolution @ 60Hz / Color depth 8Bit / Chroma 4:2:0 format. The device also works both AC/DC-coupled signals as a DP++ level shifter and low power redriver bypass mode.

It has the built-in programming registers for VESA Dual-mode DisplayPort Type-2 Cable Adaptor ID to request source-side device to enable HDMI signal output.

The jittered high-speed TMDS input regenerate to the jitter-clean signals through the PLL-based Clock/Data Recovery circuit. Additionally signal integrity can be further optimized through the equalization and pre-emphasis control setting.

PI3HDX711B Retimer provides the robust jitter cleaning capability with cascade driving to deliver TMDS signal to the reach cable distance.

Features

- **HDMI 1.4 Compliant Retimer with 3.4 Gbps data rates with Jitter Cleaning**
- **DisplayPort++ to HDMI 1.4 Level Shifting**
- **HDMI Type ID ROM and DisplayPort++ Type-2 Cable adaptor ID registers support through DDC channel**
- **Low standby current < 1mA with DDC passive switch mode**
- **Equalization and Output Pre-emphasis controls supporting both pin-strap and I2C programming**
- **DDC function for Active buffer or passive switch selection**
- **Automatic activity detection and Power Down control**
- **Power supply: 1.2/3.3V**

Applications

- **Personal Computers (NB, Desktop, AIO and Tablet)**
- **Docking, Adaptor, Dongle and Active cables**
- **Video Switch Box, Display systems**

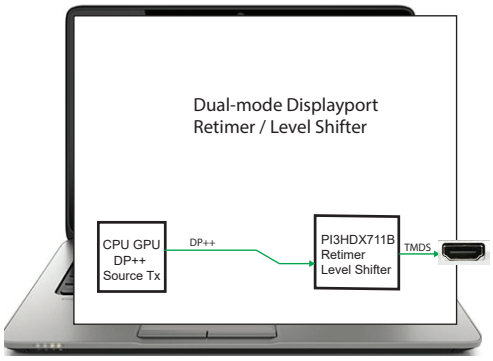


Figure 1-1 HDMI Retimer for the NB PCs

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX711B ZLAE(X)	ZLA	40-contact, Thin Fine Pitch Quad Flat No Lead Package (TQFN), 5x5mm, Tray (Tape & Reel).

Note: Suffix E = Pb-free and Green, X = Tape/Reel

2. General Information

2.1 Revision History

Date	Changes
June 2016	Preliminary release
Sep 2016	HDMI 1.4b Alt over Type-C, I2C Electrical, Diodes logo and Disclaimer add
Oct 2016	Add Ultra HD-4K Data Rate table in Ch-2 and HDMI-Alt application diagram in Ch-5
Jan 2017	Reduced Power consumption in electrical spec. Add Retimer bypass function in the related datasheet session. Add Eye diagram with insertion loss in Application.
Feb 2017	Max Power consumption numbers added
Nov 2017	Electrical spec updated with ESD changed +1.5kV/-2kV (p15). Package marking information added (p46).

2.2 Related Products

Part Numbers	Products Description
Retimers / Jitter Cleaner	
PI3HDX2711B	HDMI 2.0 and DP++ Retimer (Jitter Cleaner)
PI3HDX711B	HDMI 1.4 and DP++ ReTimer (Jitter Cleaner)
Redrivers	
PI3DPX1203B	DisplayPort 1.4 Redriver for Source/Sink/Cable Application, Linear-type
PI3HDX1204B1	HDMI 2.0 Redriver (DP++ Level Shifter), High EQ, place near to the source-side, Limiting type
PI3HDX1204E	HDMI 2.0 Linear Redriver (DP++ Level Shifter) , Link transparent, place near to the sink-side
PI3DPX1207B	DisplayPort 1.4 Alt Type-C Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3DPX1202A	Low Power DisplayPort 1.2 Redriver with built-in AUX Listener, Limiting-type
PI3HDX511F	High EQ HDMI 1.4b Redriver and DP++ Level Shifter for Sink/Source Application, Limiting-type
Active Switches & Splitters	
PI3DPX1205A	DisplayPort 1.4 Alt Type-C Mux Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3HDX231	HDMI 2.0 3:1 ports Mux Redriver, Linear-type
PI3HDX414	HDMI 1.4b 1:4 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX412BD	HDMI 1.4b 1:2 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX621	HDMI 1.4 Redriver 2:1 Active Switch with built-in ARC and Fast Switching support, Limiting-type

Contents

3. Pinout

3.1 Package Pinout

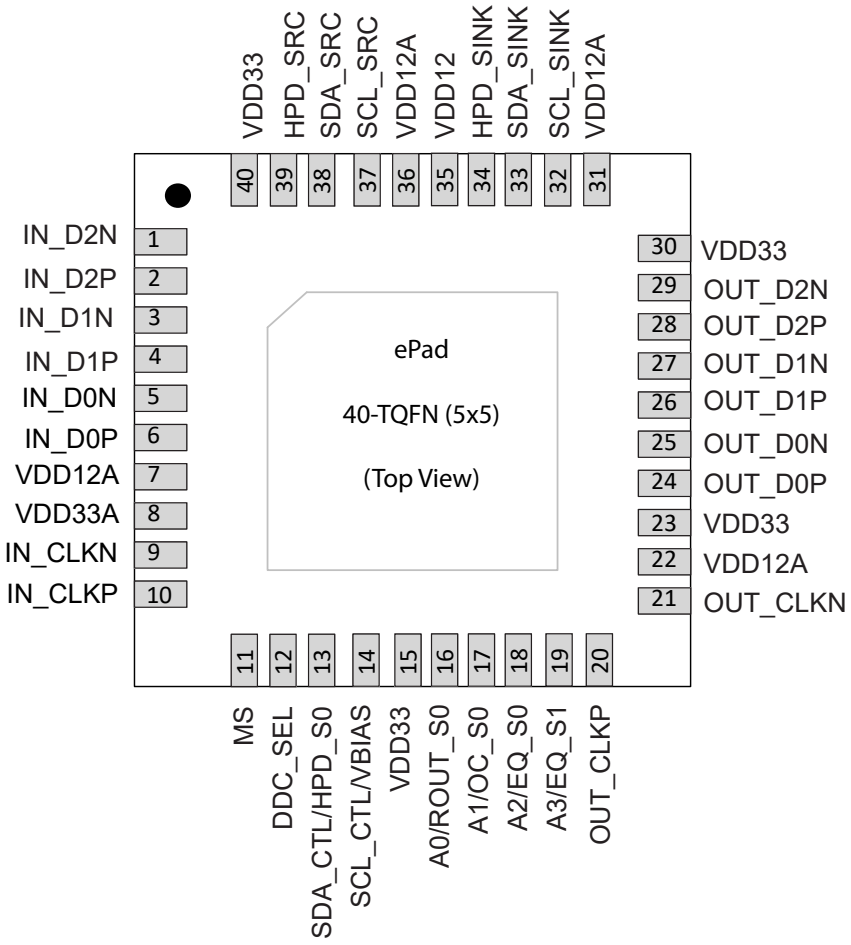


Figure 3-1 Pinout Configuration

3.2 Pin Description

Pin Name	Pin #	Type	Description
IN_D2N/P	1,2	I	TMDS Data inputs. RT=50Ω, RPD=200 KΩ.
IN_D1N/P	3,4	I	
IN_D0N/P	5,6	I	
IN_CLKN/P	9,10	I	TMDS Data output. RT=50Ω, RPD=200 KΩ.
MS	11	I	Mode Selection. Pin mode and I2C mode selection with 100KΩ pull down resistor. 1 = I2C programming mode 0 = PIN control mode
DDC_SEL	12	I	DDC Buffer or Passive switch selection. Internal 100kΩ pull-down resistor 1 = DDC Buffer 0 = Passive Switch
SDA_CTL/ HPD_S0	13	IO	Shared pin. (1) HPD_SRC output control. Pull-up: open-drain output. Pull-down: Buffer output with inverter function from HPD_SINK. (2) SDA_CTL pin for I2C mode
SCL_CTL/VBIAS	14	IO	Shared pin. (1) TMDS input termination voltage control. Pull-up: Vbias tie to VDD for HDMI signal input Pull-down: Vbias ties to GND for DP signal input (2) SCL_CTL pin for I2C mode
A0/ROUT_S0	16	I	Shared pin (1) I2C Address bit A0 (2) Data output selection pin. Internally 100kΩ pull-up to VDD. 0 = Make Rout termination resister off for open-drain output 1 = Make Rout termination resistor pull-up for double termination output.
A1/OC_S0	17	I	Shared pin (1) I2C Address Bit A1 (2) Data Output Pre-emphasis control with internal 100kΩ pull-up and pull-down 0 = 0 dB, M/Floating = 1.5 dB 1 = 2.5 dB
A2/EQ_S0	18	I	Shared pin (1) I2C Address Bit A2 (2) Data Input equalization control pin bit-0. See more in EQ_S0/EQ_S1 functional table.
A3/EQ_S1	19	I	Shared pin (1) I2C Address A3 (2) Data Input equalization control pin bit-1. See more in EQ_S0/EQ_S1 truth table.

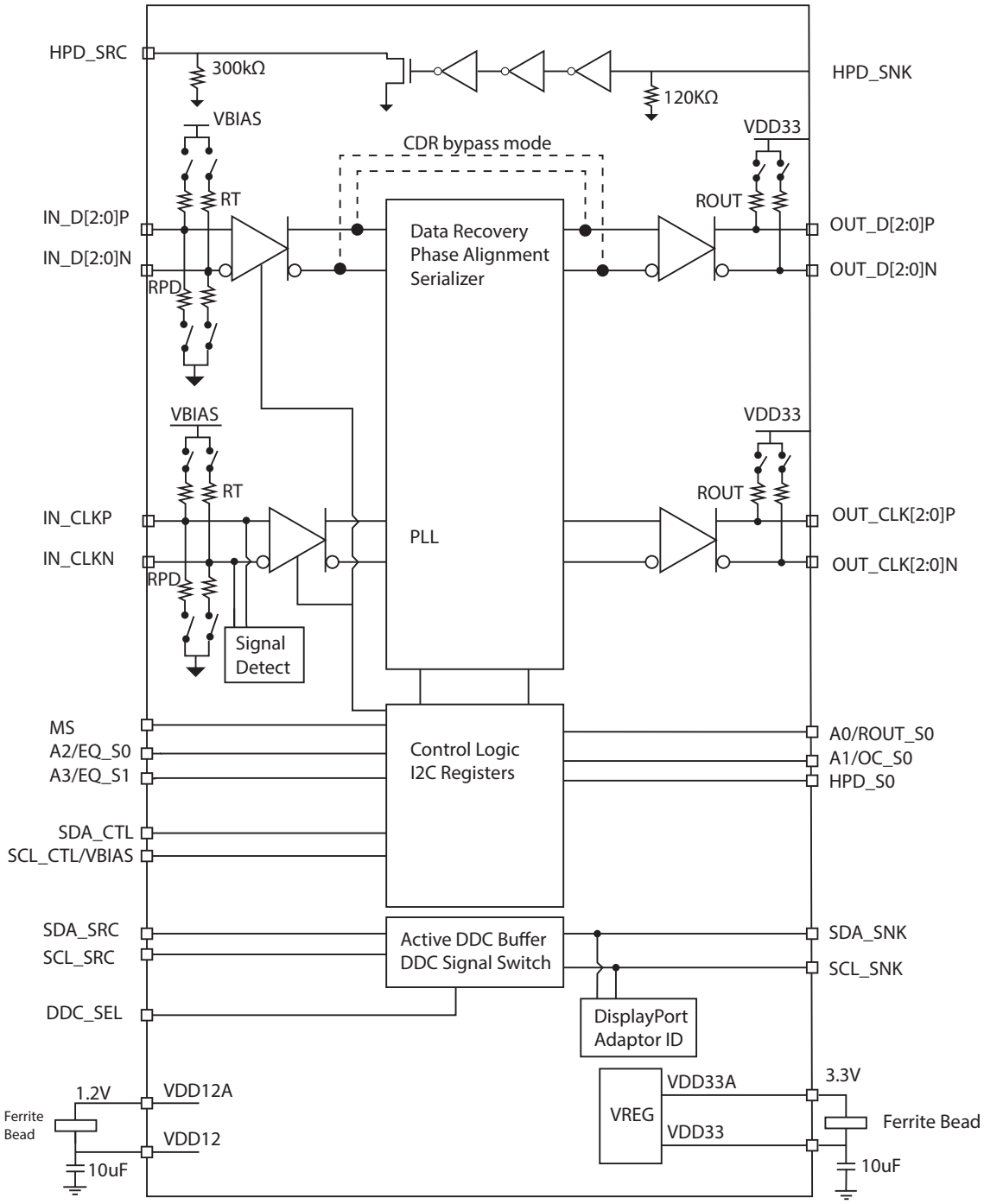
Pin Name	Pin #	Type	Description
OUT_CLKP/N	20,21	O	TMDS Clock channel outputs. ROUT_S0 = 1 : Double termination output
OUT_D0P/N	24,25	O	TMDS Data Ch 0/1/2 channels outputs. ROUT_S0 = 1 : Double termination outputs
OUT_D1P/N	26,27	O	
OUT_D2P/N	28,29	O	
SCL_SINK	32	IO	Sink side DDC clock. 5V Tolerant
SDA_SINK	33	IO	Sink side DDC data. 5V Tolerant
HPD_SINK	34	I	Sink side Hot Plug Detect pin. 5V Tolerant
SCL_SRC	37	IO	Source side DDC clock
SDA_SRC	38	IO	Source side DDC data
HPD_SRC	39	O	Source side Hot Plug Detect pin
EPAD	EPAD	G	Epad Ground pin
VDD33	15, 23, 30, 40	P	3.3V Power Supply
VDD12	35	P	1.2V Digital Power Supply
VDD33A	8	P	3.3V Analog Power Supply
VDD12A	7, 22, 31, 36	P	1.2V Analog Power Supply

Note

(1) PU: Pull-up, PD: Pull-down, P: Power, G: Ground, I: Input, O: Output, IO: Bidirectional

4. Functional

4.1 Block Diagram



4.2 Function Description

4.2.1 Phase-Locked-Loop (PLL) and Data Recovery

The clock channel has a high performance PLL to create a low jitter sampling clock for the clock and data recovery. Each TMDS Data paths have data recovery circuit, operating independently from the other channels. Each CDR aligns the sampling clock edges by digitally interpolating the clock from regenerated clock channel.

4.2.2 Squelch function

CLK squelch detector is used to control TMDS data output channels, either HIZ or Pull-Up to VDD with internal 50 Ω resistor. Squelch function is turn on in the condition of no-TMDS input clock signals around 10MHz.

4.2.3 Input termination resister RT and Power down resister RPD

The power-down resistor RPD is active at HPD_SNK = 0. When Output is disabled, TMDS channels are shut down and go to the high impedance state

4.2.4 HPD_SINK Detector

When HPD_SINK = 0, chip is stand-by mode.

HPD_ SINK	HPD_SINK low to high de-bonus time	HPD_SINK from high to low shut down delay time
t_{SETUP}	>2ms	4s max.

4.3 Control signals

TMDS Output Pre-emphasis

Rout_S0	OC_S0	Single-end Vswing (mV)	Pre-emphasis (dB)
0	0	500	0 (open drain)
0	M	500	1.5 (open drain)
0	1	500	2.5 (open drain)
1	0	500	0 (double termination)
1	M	500	1.5 (double termination)
1	1	500	2.5 (double termination)

Note
1) Open drain (Rout off); Double termination (Rout on)
2) OC_S0 is three-level inputs with internally 100kΩ Pull-up and 100kΩ Pull-down.
3) "0" ties GND, "M" is floating or VDD/2, "1" ties to VDD

EQ-pin truth table for TMDS data channels

EQ_S1	EQ_S0	Operation
0	0	3 dB compensation
0	1	6 dB compensation
1	0	9 dB compensation
1	1	12 dB compensation

Note: TMDS clock channel's EQ value is 3dB fixed without pre-emphasis and double termination.

MS pin

MS	Operation
0	Pin control setting mode
1	I2C programming control setting mode

DDC_SEL, VDDSRC_SEL pins

DDC_SEL	Operation
0	Passive switch, 3.3/2.5V interface in DDC_SRC
1	DDC buffer, 3.3/2.5V interface in DDC_SRC

Power Down blocks status

#1: When OEB=1,

All blocks are off in pin mode, BG, LDO and TypeID ROM are on, other blocks are off.

#2: When OEB=1,

I2C mode, BG, LDO, I2C control and TypeID ROM are on. All other blocks are off.

#3: When OEB=0, HPD_SINK=1,

All blocks are on, waiting for CLK detection circuit, so BG, LDO, 1MHZ OSC etc will be working.

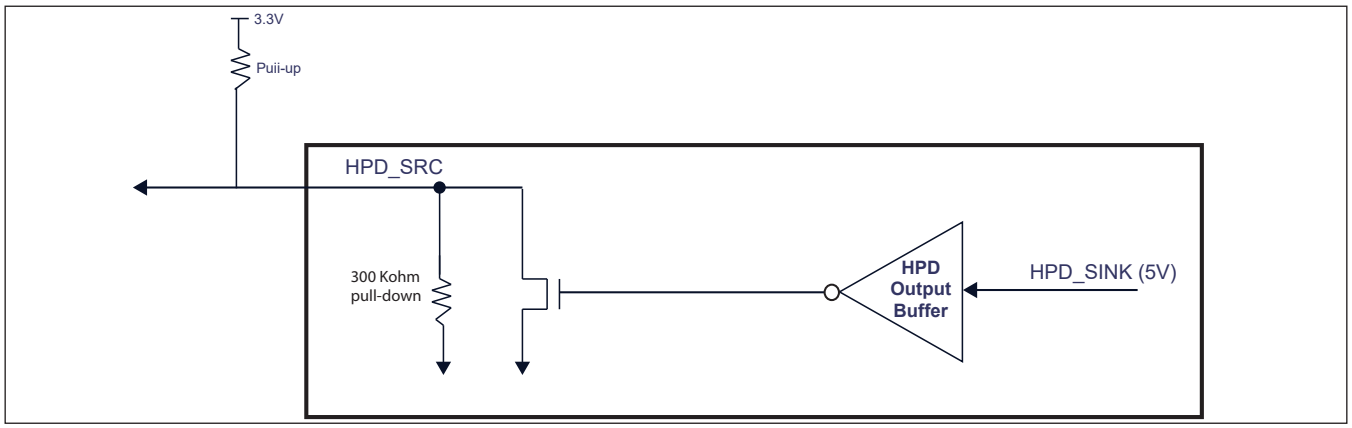
#4: When OEB=0, HPD_SINK=0 from high about 4s,

Standby condition will be same as #1 to keep low IDDQ.

#5 When OEB=0, HPD_SINK from 0 to 1,

It will be same as item b of OEB change from 1 to 0.

Source-side Hot plug Detect (HPD_SRC) Output



Note:
1) Open drain buffer is recommended with external pull-up resistor to < 4.5V power supply.

4.4 Programming Registers Details

4.4.1 DisplayPort cable adaptor ID registers

Dual-Mode DP Cable Adaptor Address Space, Device Address 80h/81h

Category	Offset	Description	Read or Write/Read
Capabilities	00h to 0Fh	16 byte DDC Buffer ID (HDMI adaptor ID)	Read
	10h to 1Fh	Cable adaptor capabilities	Read
Control	20h to 2Fh	Cable adaptor feature controls.	Read/Write
Vendor Determined	30h to 3Fh	Register definition may be determined by the cable adaptor vendor, as identified by the IEEE_OUI contained in Cable Adaptor registers offset 11h, 12h, and 13h. If these registers are not implemented they are RE-SERVED	Vendor Determined
RESERVED	40h to FFh	Reserved	

Dual-Mode DP cable Adaptor Address Space, Device Address 80h/81h

Offset	Cable Adaptor Static Capabilities: 00h to 1Fh	Read/Write
00h - 0Fh	HDMI ID (DDC Buffer ID)	Read
10h	TMDS Cable Adaptor Identifier	Read
11h	IEEE_OUI first two hex digits. Example: for IEEE OUI 00-1B-C5, this field is set to 00h	Read
12h	IEEE_OUI second two hex digits. Example: for IEEE OUI 00-1B-C5, this field is set to 1Bh	Read
13h	IEEE_OUI third two hex digits. Example: for IEEE OUI 00-1B-C5, this field is set to C5h	Read
14h-19h	Device Identification String. Identifies the adaptor. Up to six ASCII characters, starting at 14h, remaining bytes 00h if less than six characters	Read
1Ah	Hardware revision	Read
1Bh	Firmware/software major revision	Read
1Ch	Firmware/software minor revision	Read
1Dh	Maximum TMDS clock rate	Read
1Eh	I2C speed control capabilities bit map	Read
1Fh	RESERVED	Read
20h	TMDS_OE#. Enable/disable the TMDS output buffers. Default = Enabled.	Read/Write
21h	HDMI Pin Control	Read/Write
22h	I2C speed control/status bit map	Read/Write
23h to 2Fh	RESERVED	Read/Write
30h to 3Fh	Reserved for vendor-defined features	Read/Write
40h to FFh	RESERVED	Read/Write

4.5 HDMI Type ID ROM

Set I2C Byte RX_SET 0x01[1] = 0 to disable HDMI Type ID

Data Offset	Data in spec	Read/ Write	Description as in spec	Type2 for HDMI1.4
00h	44h	RO	D	D
01h	50h	RO	P	P
02h	2dh	RO	-	-
03h	48h	RO	H	H
04h	44h	RO	D	D
05h	4dh	RO	M	M
06h	49h	RO	I	I
07h	20h	RO	Space	Space
08h	41h	RO	A	A
09h	44h	RO	D	D
0Ah	41h	RO	A	A
0Bh	50h	RO	P	P
0Ch	54h	RO	T	T
0Dh	4Fh	RO	O	O
0Eh	52h	RO	R	R
0Fh	04h	RO	.	.
10h	UD	RO	Cable Adaptor Identifier [2:0] 000 type 2 [3] 0 [7:4] 1010 type 2 or above.	A0h
11h	UD	RO	IEEE OUI 1st byte	00h
12h	UD	RO	IEEE OUI 2nd byte	60h
13h	UD	RO	IEEE OUI third byte	23h
14h	UD	RO	Device Id	50h “P”
15h	UD	RO	Device Id	49h “I”
16h	UD	RO	Device Id	33h “3”
17h	UD	RO	Device Id	48h “H”
18h	UD	RO	Device Id	44h “D”
19h	UD	RO	Device Id	58h “X”
1Ah	UD	RO	Hardware (chip) revision 7:4h: major revision 3:0h: minor revision.	00h
1Bh	UD	RO	Firmware/software major revision	00h
1Ch	UD	RO	Firmware/software minor revision	00h

Data Offset	Data in spec	Read/ Write	Description as in spec	Type2 for HDMI1.4
1Dh	UD	RO	Clock rate, specified max 300MHz for HDMI [7:0]= 42h: 1.65Gbps =5Ah: 2.25Gbps =78h: 3Gbps	78h: 300MHz, (00/2.5=120 =78h)
1Eh	0Fh	RO	I2C speed control capabilities bit map with 22h.	0Fh
1Fh	00h	RW	Reserved data Address at 1fh: 1. DP source reads data address 1fh, ID register returns 00h 2. DP source writes data AAh to data address 1fh, ID register responds ACK or returns 00h.	00h, RW
20h	00h	RW	TMDS output enable or disable. 00h: enabled 01h: disabled (<=10mV Voff) [7:1] Reserved	00h, RW 00h: enabled 01h: disabled (<=10mV Voff) [7:1] Reserved
21h	00h	RW	[0]CEC_EN: Enables/disables the CEC Isolation Switch. 00h: disabled 01h: enabled [7:1] Reserved	00h, RW 00h: disabled 01h: enabled [7:1] Reserved
22h	UD	RW	I2C speed control status bit map. 01h: 1Kbps 02h: 5Kbps 04h: 10Kbps 08h: 100Kbps 10h, 20h, 40h and 80h are reserved	08h for 100KHz, RW, For the function specified as: 01h: 1Kbps 02h: 5Kbps 04h: 10Kbps 08h: 100Kbps 10h, 20h, 40h and 80h are reserved
23h-FFh	00h	R/W	Reserved data Address from 23h to FFh: 1. DP source reads data address 23h thru FFh, ID register returns 00h. 2. DP source writes data AAh to data address 23h through FFh, ID register responds ACK or returns 00h.	23h-FFh=00h, RW, reserved.

4.6 I2C Programming

I2C Address Byte

	b7 (MSB)	b6	b5	b4	b3	b2	b1	b0 (R/W)
Address Byte	1	0	1	A3	A2	A1	A0	1/0 *

Offset	Name	Description	Power Up Condition	Type
0x00	CONFIG[7:0]	[7] Enable Standby 0: normal mode 1: standby mode In standby mode, TMDS equalizer, de-jitter and output driver are powered down. [6] re-timer or bypass mode 0: re-timer 1: bypass [5] TMDS clock speed auto detection enable 0: enable 1: disable (Must set 1) [4] Mode selection when HDMI mode auto detection disable 0: HDMI 1.4 operation mode 1: Reserved [3] DDC_SRC voltage selection 0: 1.8V 1: 3.3V/2.5V [2] DDC function 0: Passive switch 1: Active buffer [1] HPD_SRC output selection 0: Open drain output (as default) 1: Buffer output [0] HPD_SRC output logic function (buffer) 0: HPD_SRC=HPDx 1: HPD_SRC=/HPDx	0x00	R/W

Offset	Name	Description	Power Up Condition	Type
0x01	RX_SET[7:0]	Receiver equalization setting [7] Disable port termination resistors at HDMI mode 0 = Rpd connected 1 = Rpd disconnected [6] TMDS input termination V-bias selection 0: Connect to GND (default) 1: Connect to VDD V-bias register selection enable [5:3] EQ programmable setting 000: 3 dB 001: 6 dB 010: 9 dB 011: 12 dB 1xx: Reserve [2] Squelch disable 0: Squelch enable (as default) 1: Squelch disable [1] HDMI type ID disable 0: Type ID enable (as default) 1: Type ID disable [0] HDMI type ID selection 0: Reserved 1: HDMI 1.4 (Must Set 1)	0x00	R/W
0x02	TX_SET[7:0]	TMDS output setting [7] TMDS output control 0: Open drain 1: Double termination [6:4] TMDS output Pre-emphasis control 000: 0 dB 001: 1.5dB 010: 2.5dB 011: 3.5dB 1xx: 6dB de-emphasis (750mV swing) [3:2] Reserved by test adjust TMDS output swing setting 00 500mV as default 01: -10% 10: +10% 11: +20% [1:0] Data slew rate control adjustment	0x00	R/W
0x03 to 0x15	Reserved	[7:0] Reserved	0x00	R/W

5. Electrical Specification

5.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential. . . . . –0.5 V to +4.0 V
Supply Voltage Range, VDD33 . . . . . -0.5V to 4.0V
Supply Voltage Range, VDD12 . . . . . -0.5V to 2.0V
Output Current . . . . . –25 mA to +25 mA
5V Tolerance I/O Pins (SDA_SINK, SCL_SINK, HPD_SINK) . . . . . -0.5V to +5.5V
Storage Temperature . . . . . –65 °C to +150 °C
Max Junction temperature T_J . . . . . 125°C
ESD, HBM . . . . . +1.5kV, -2kV
ESD, CDM . . . . . ±500V

Note:

(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect inoperability and degradation of device reliability and performance.

5.2 Recommended Operation

Parameter(1)	Min.	Typ.	Max.	Unit
3.3V Power Supply Voltage (VDD33, VDD33A)	3.0	3.3	3.6	V
1.2V Power supply (VDD12, VDD12A)	1.14	1.2	1.26	V
Power Supply Noise Tolerance up to 100MHz(2)		100		mVp-p
Operation temperature, T_A	-20		70	°C

Note
(1) Typical parameters are measured at VDD=3.3V, T_A= 25 °C. They are for reference purpose only, and are not production-tested. Parameters is specified by statistical and/or design
(2) Allow supply noise (mVp-p sine wave) at typical condition. Measured at the pin inputs after the power supply filtering.

5.3 Thermal Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Lead Temperature (Soldering, 5 sec.)				260	°C
Thermal Resistance $\theta_{JA, No\ Airflow}$	θ_{JA}			33	°C/W

5.4 Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. All parameters are specified by test, statistical analysis, or design unless otherwise specified. The specified parameters numbers inside of parenthesis ( ) are design target numbers, not silicon-tested.

5.4.1 Power Signal Sequence Requirement

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
tVDD33	3.3V supply ramp time	10% to 90% of the 3.3V supply voltage			200	ms
tVDD12	1.2V supply ramp time	10% to 90% of the 1.2V supply voltage			200	ms
tD1	Delay time	50% of 3.3V to 50% of 1.2V power rails	10			uS

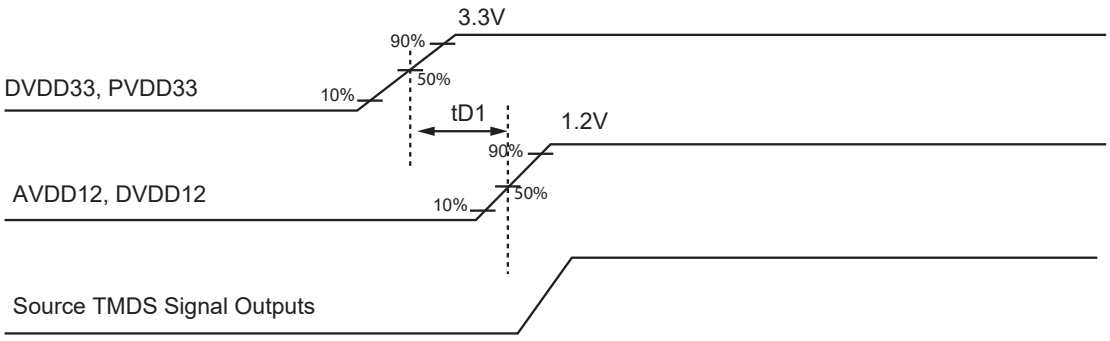


Figure 5-1 Power up sequence timing diagram

5.4.2 Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Retimer Mode Active Current (VDD33 = 3.3V, VDD12 = 1.2V. Room temperature)						
I_{DD12_DT}	AVDD12, DVDD12 Current	Device Enabled PRBS15 pattern, fCLK=340 MHz, RT=50Ω to VDD33		280	350	mA
I_{DD33_DT}	DVDD33, PVDD33 Current			100	150	mA
P_{W_DT}	Total Power with Double Termination			645		mW
Redriver mode Active Current (VDD33 = 3.3V, VDD12 = 1.2V. Room temperature)						
I_{DD12}	AVDD12, DVDD12 Current	Device Enabled PRBS15 pattern, fCLK=340 MHz, RT=50Ω to VDD		100	120	mA
I_{DD33}	DVDD33, PVDD33 Current			60	100	mA
P_{W_OD}	Total Power with Double Termination			318		mW

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Retimer Mode Standby, I2C (VDD33 = 3.3V, VDD12 = 1.2V. Room temperature)						
I_{STB_Switch}	VDD12/DVDD12 Standby Current	DDC passive switch, HPD_sink=0 (BG, LDO on)		0.4	0.5	mA
	VDD33/VDD33A Standby Current	DDC passive switch, HPD_sink=0 (BG, LDO on)		0.8	0.95	mA
I_{STB_Buffer}	VDD12/DVDD12 Standby Current	DDC active buffer , HPD_sink=0 or OEB=high		0.4	0.5	mA
	VDD33/VDD33A Standby Current	DDC active buffer , HPD_sink=0 or OEB=high		1.9	2.3	mA
I_{SQLH_Sw}	VDD12/DVDD12 Squelch current (no input detected)	DDC passive switch, HPD_sink=3.6V		0.35	0.42	mA
	VDD33/VDD33A Squelch current (no input detected)	DDC passive switch, HPD_sink=3.6V		2.7	3.3	mA
I_{SQLH_Buffer}	VDD12/DVDD12 Squelch current. (no input detected)	DDC active buffer, HPD_sink=3.6V		0.3	0.42	mA
	VDD33/VDD33A Squelch current (no input detected)	DDC active buffer, HPD_sink=3.6V		3.7	4.6	mA

5.4.3 DC Specifications

Control pin (OC_S0 with 100k pull high, 100k pull low when TMDS active)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IIH	High level digital input current	VIH = 3.3V, VDD= 3.3V	-15		50	µA
IIL	Low level digital input current	VIL = GND, VDD = 3.3V	-50		15	µA

Control pin (ROUT_S0,EQ_S0/S1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IIH	High level digital input current	VIH =VDD	-15		15	µA
IIL	Low level digital input current	VIL = GND	-50		-15	µA
VIH	High level digital input voltage		2.0			V
VIL	Low level digital input voltage		0		0.8	V

HPD_SRC

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{OL}	Buffered Output Low Voltage	IOL = 4 mA			0.4	V
	Open Drain Output Low Voltage	IOL = 4 mA	0		0.4	V
V_{OH}	Buffered Output High Voltage	IOH = 0.1 mA	VDD-1.55			V
I_{OFF}	Off leakage current	VDD=0, VIN=3.6V			30	uA
I_{OZ}	Open drain Output leakage current	VDD=3.6V, VIN=3.6V			30	

HPD_SINK

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{IH}	Input High level input current	VIH =5.5V	-10		80	µA
I_{IL}	Input Low level input current	VIL = GND	-15		15	µA
V_{IH}	Input High level input voltage	VDD=3.3V	2.0			V
V_{IL}	Input Low level input voltage		0		0.8	V

DDC Channel Buffer

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH_SRC}	Source DDC Buffer Input High Voltage		0 .8			V
V_{IL_SRC}	Source DDC Buffer Input Low Voltage				0 .3	V
V_{OL_SRC}	Source DDC Buffer Output Low Voltage	External pull-up Rup to VDD from 1.5kΩ to 10kΩ	0 .47	0 .52	0 .6	V
V_{OL_SINK}	Sink DDC Buffer Output Low Voltage	External pull-up Rup to VDD from 1.5kΩ to 10kΩ			0 .2	V
V_{IH_SINK}	Sink DDC Buffer Input High Voltage		2 .0			V
V_{IL_SINK}	Sink DDC Buffer Input Low Voltage				0 .8	V
C_{I_SRC}	Source DDC capacitance	VIpp(peak-peak) = 1V, 100 KHz		5		pF
C_{I_SINK}	Sink DDC capacitance	VIpp(peak-peak) = 1V, 100 KHz		5		pF

DDC Channel Switching

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LK}	Input leakage current	DDC switch is off, Vin = 5.5V	-10		30	µA
C_{IO}	Input/Output capacitance when passive switch on	VIpp(peak-peak) = 1V, 100 kHz		10		pF
R_{ON}	Passive Switch resistance	IO = 3mA, VO = 0.4V		30	50	Ω
V_{PASS}	Switch Output voltage	VI=3.3V, II=100uA VDD=3.3V	1.5	2.0	2.5	V
I_{OZ}	Leakage current with Hi-Z I/O	VDD = 3.6V			30	µA

TMDS Differential Pins

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VI_{DIFF}	Input differential voltage level		150		1200	mV
VI_{CM}	Input common mode voltage	VICM1	VDD33 - 700		VDD33 - 37 .5	mV
		VICM2	VDD33-10		VDD33+10	mV
VI_{OPEN}	Single-ended input voltage under high impedance or open case	IIN = 10uA	VDD33-10		VDD33+10	mV
RT_{IN}	Input termination resistance	VIN = 3.3V	45	50	55	Ω
V_{OH}	Single-ended high level output voltage.Data Channels 0,1,2		VDD33-10		VDD33+10	mV
	Single-ended high level output voltage.Clock Channels		VDD33-10		VDD33+10	mV
V_{OL}	Single-ended low level output voltage. Data Channels 0,1,2		VDD33-600		VDD33–400	mV
	Single-ended low level output voltage. Clock Channels		VDD33-600		VDD33–400	mV
V_{SWING}	Single-ended output swing voltage. Data channels 0,1,2		400	500	600	mV
	Single-ended output swing voltage. Clock channels		200	500	600	mV
$V_{OD(O)}$ (1)	Overshoot of Output differential voltage				180	mV
$V_{OD(U)}$ (2)	Undershoot of Output differential voltage				200	mV
$V_{OC(SS)}$	Change in Steady-State common- mode output voltage between logic states				5	mV
I_{OS}	Short Circuit output current at open drain mode	Short to VDD	-12		12	mA

Note:
(1) Overshoot of output differential voltage VOD(O) = (VSWING(MAX) * 2) * 15%
(2) Undershoot of output differential voltage VOD(O) = (VSWING(MIN) * 2) * 25%

5.4.4 AC Differential

TMDS Differential

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
TMDS(CML) Input						
V_{TX}	Input Voltage Swing (Launch Amplitude)	Measured differentially at TPA	800	1000	1560	mVp-p
V_{ICM_DC}	Input Common Mode Voltage	DC-coupled requirement measured at TPB, VINmin=800mV, VINmax=1200mV	VDD33-0.3		VDD33 -0.2	V
V_{IN}	Input Voltage Sensitivity	Measured differentially. 3.4Gbps, Clock Pattern	150		1560	mVp-p
R_{IN}	Diff Input Resistance	IN+ to VDD and IN- to VDD	80	100	110	Ω
$RL_{(O)}$	Differential Output return loss	100MHz - 340MHz		10		dB
V_{OFF}	Standby Output Voltage	Measured DC output at TPC, RT = 50 Ω when DUT VDD is off with OUT+/OUT- terminated by RT=50 Ω to VDD	VDD33 -10		VDD33 +10	mV
$V_{SW(O)}$	Differential Output voltage swing	External resistor = 24 Ω	800		1200	mVp-p
$V_{CM(O)}$	Output common mode voltage	Measured single-ended, 3.4Gbps	VDD33-0.35		VDD33 -0.2	V
V_{DIFF}	Differential Voltage		-780		780	mV
tCLK	TMDS Clock Rate		85		340	MHz
	Clock duty cycle		40		60	%
TMDS Differential Clock Jitter, max						
fCLK	Clock Frequency	Clock Path	25		340	MHz
bR	Bit Rate	Data Path	0.25		3.4	Gbps
tSL	SD(Signal Detect)(1) to Lock Time			4		ms
tEN	Delay from power down to normal operation				10	ms
tDIS	Delay from normal operation to power down				0.1	ms

Control and Status pins (HPD_SINK, HPD_SRC)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
tPD (HPD)	Propagation delay (from HPD_SINK to HPD_SRC, high to low)	CL = 10pF, Pull high resistor=1kΩ		10		ns

5.4.5 DDC IO Pins Passive switch / Buffer AC Differential

DDC I/O pins (Passive Switch)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
tPD (DDC)	Propagation delay from SCL_SINK/ SDA_SINK to SCL/SDA, or SCL/SDA to SCL_SINK/SDA_SINK	CL = 10pF			5	ns

DDC I/O pins (Active buffer)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
tPLH	LOW-to-HIGH propagation delay	SCL/SDA to SCL/SDA_SINK		169	255	ns
tPHL	HIGH-to-LOW propagation delay	SCL/SDA to SCL/SDA_SINK	10	103	300	ns
tPLH	LOW-to-HIGH propagation delay	SCL/SDA_SINK to SCL/SDA	25	67	110	ns
tPHL	HIGH-to-LOW propagation delay	SCL/SDA_SINK to SCL/SDA		118	230	ns

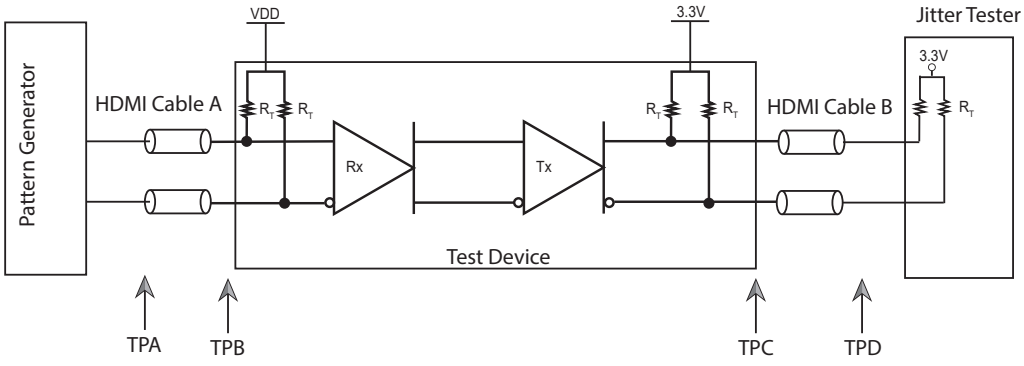


Figure 5-2 TMDS Output Transition Timing Definition

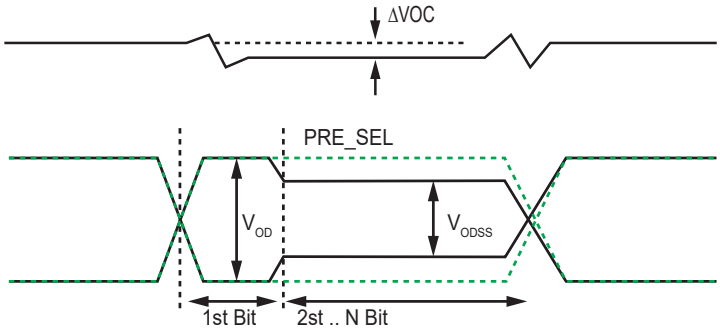


Figure 5-3 TMDS Output Transition Timing Definition

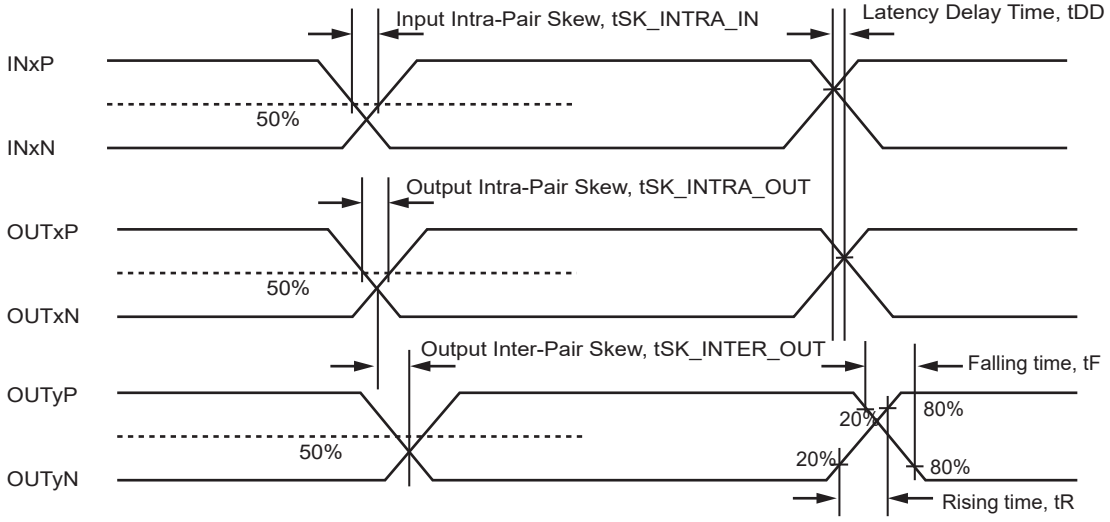
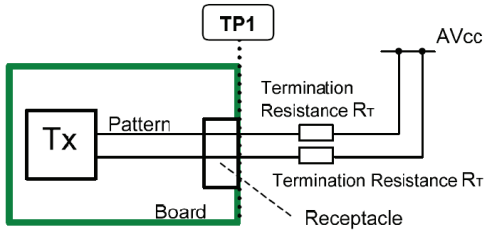
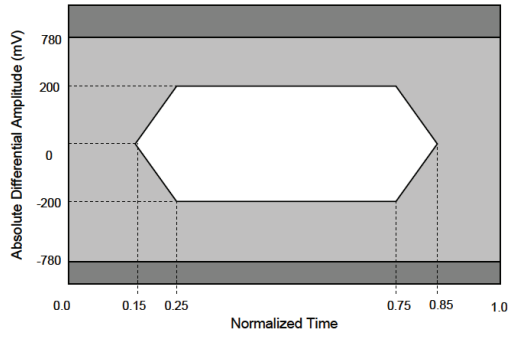


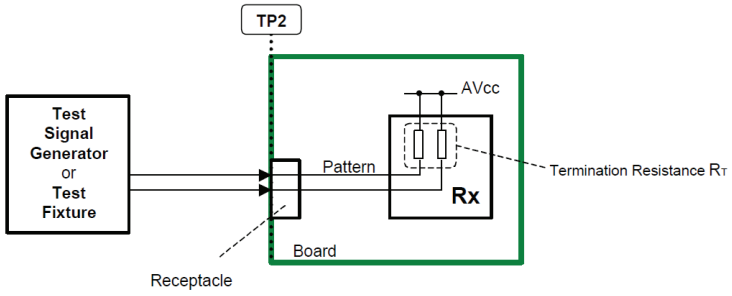
Figure 5-4 Differential Skew, Rising/Falling Time and Latency Definition



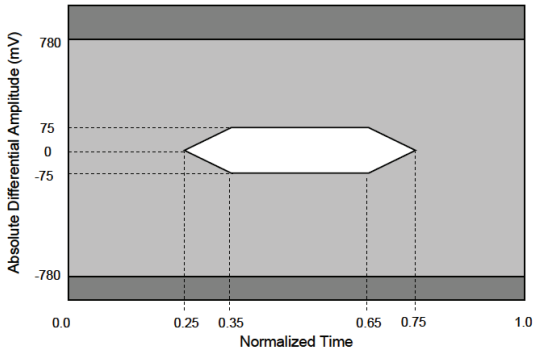
HDMI 1.4 Source Test



HDMI 1.4 Eye Diagram Mask at TP1 for Source Requirements



HDMI 1.4 Sink Test



HDMI 1.4 Eye Diagram Mask at TP1 for Sink Requirements

Figure 5-5 HDMI Source Sink Device Test Point for Eye Diagram

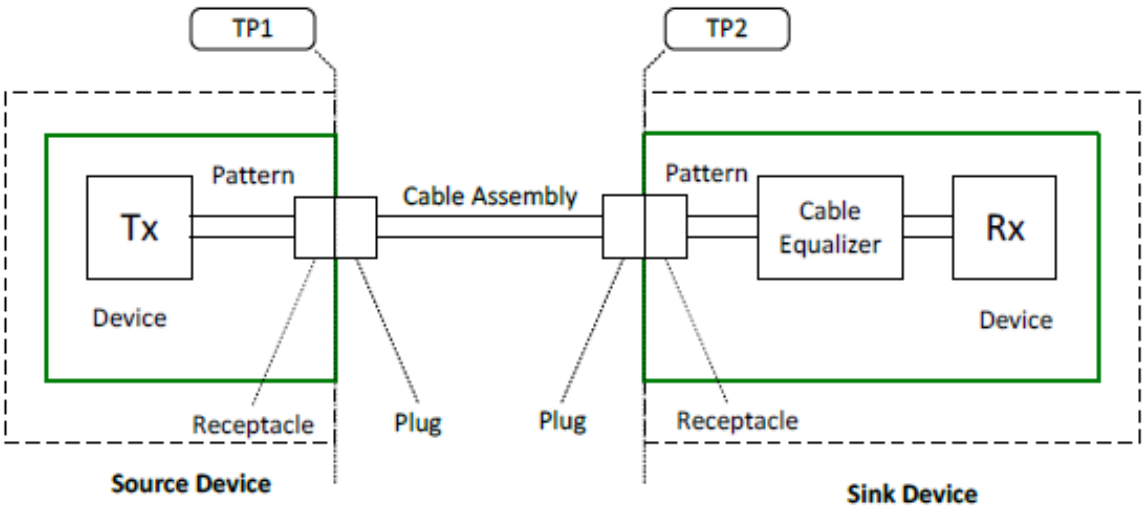


Figure 5-6 TMDS Link test point

5.5 I2C Bus SCL/SDA

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
VDD	Nominal Bus Voltage		3.0		3.6	V
Freq	Bus Operation Frequency				400	kHz
V_{IH}	DC input logic high		$V_{DD}/2$ + 0.7		V_{DD} + 0.3	V
V_{IL}	DC input logic low		-0.3		$V_{DD}/2$ - 0.7	V
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	V
Ipullup	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
Ileak-bus	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
tBUF	Bus Free Time Between Stop and Start condition		1.3			us
tHD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At pull-up, Max	0.6			us
TSU:STA	Repeated start condition setup time		0.6			us
TSU:STO	Stop condition setup time		0.6			us
THD:DAT	Data hold time		0			ns
TSU:DAT	Data setup time		100			ns
tLOW	Clock low period		1.3			us
tHIGH	Clock high period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tPOR	Time in which a device must be operation after power-on reset				500	ms

Note:
(1) Recommended maximum capacitance load per bus segment is 400pF.
(2) Compliant to I2C physical layer specification.
(3) Ensured by Design. Parameter not tested in production.

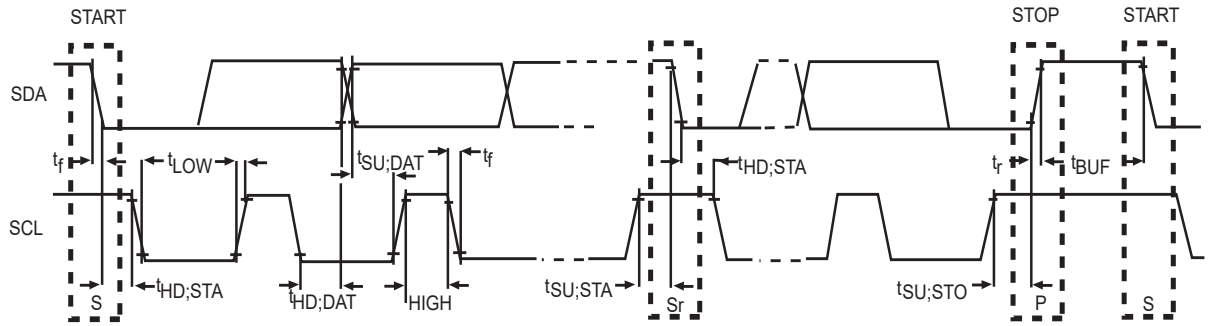


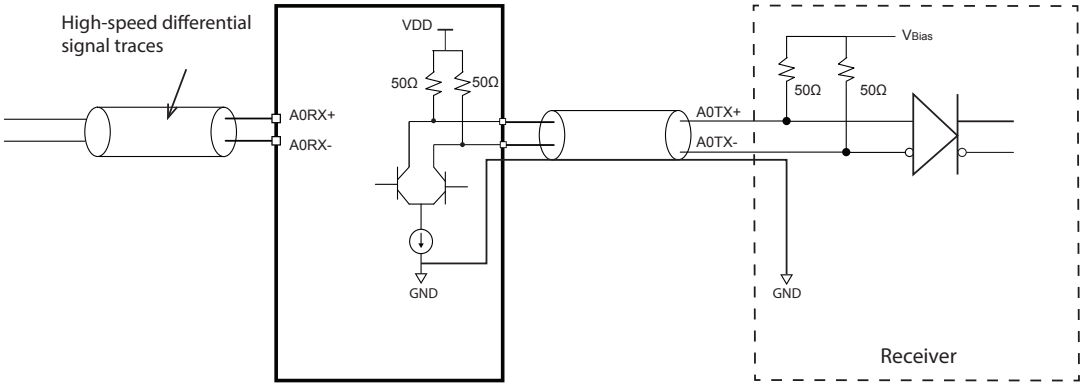
Figure 5-7 Channel-isolation test configuration

6. Application/Implementation

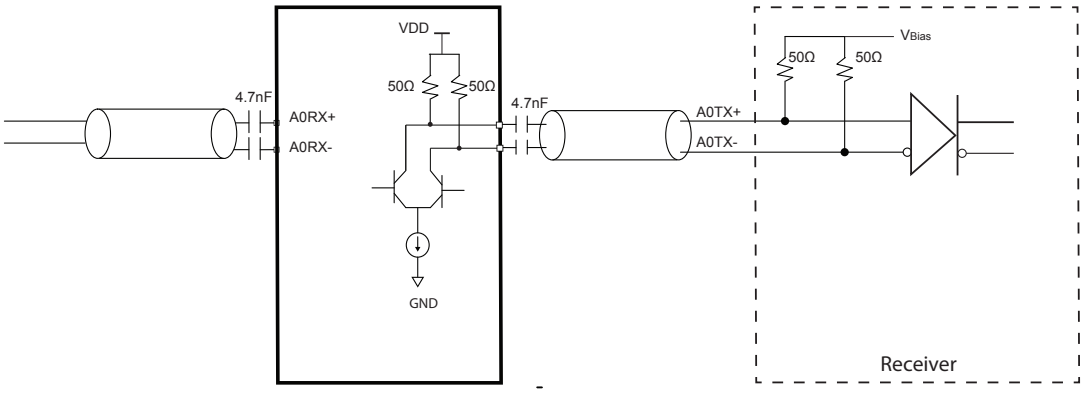
Note:
Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 DC/AC Coupled Applications

The PI3HDX711 is designed to support TMDS differential pairs with DC coupled transmission lines. It contains integrated termination resistors (50Ω), pulled up to VDD at the input stage, and Source termination output for DVI / HDMI signaling. Below Figures are shown the DC coupled connection between the HDMI Source and HDMI Sink devices. The AC coupled method connecting between the Source and the Sink devices may be preferred to eliminate the impact of the ground potential difference, or to use one CAT5/6 cable between two chassis. Note AC coupled configuration is not compliant to the HDMI specification of Source requirement.



DC-Coupled Differential Signaling Application Circuits



AC-Coupled Differential Signaling Application Circuits

Figure 6-1 AC- and DC-coupled circuit diagram

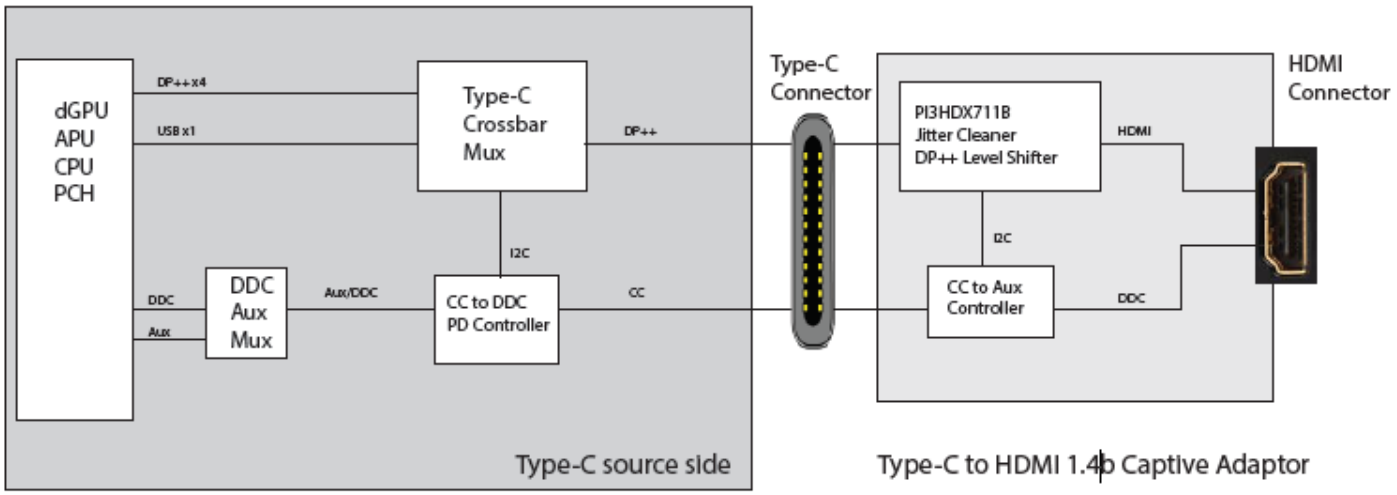
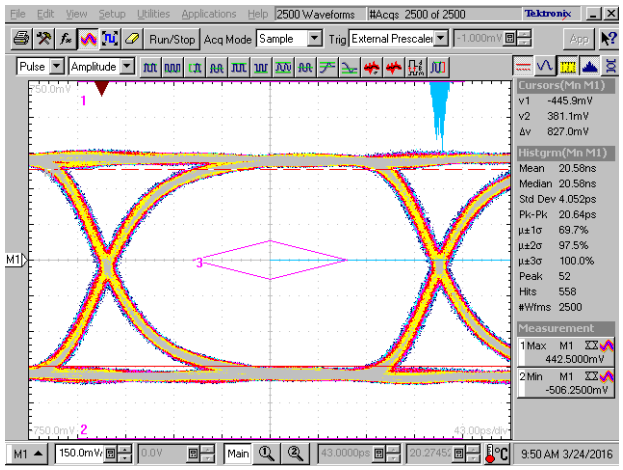
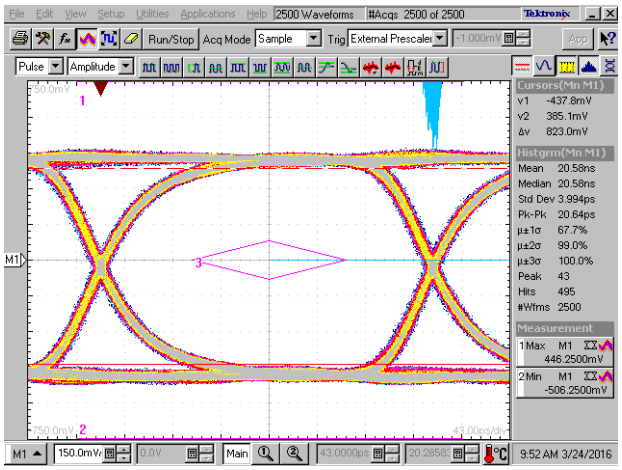
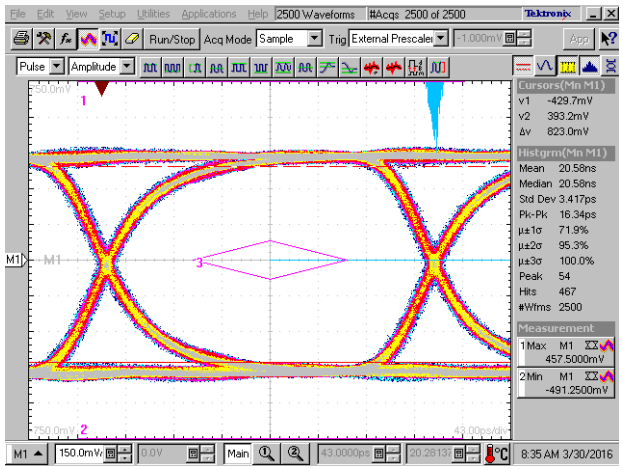
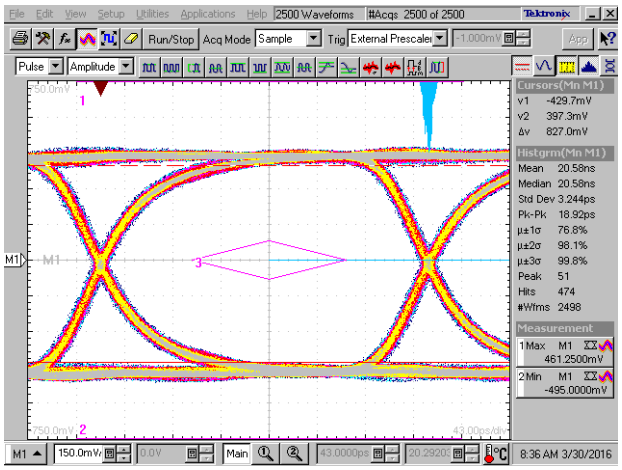


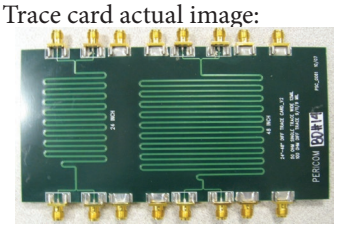
Figure 6-2 HDMI Alt Type-C Cable Application

6.2 Eyes measurement

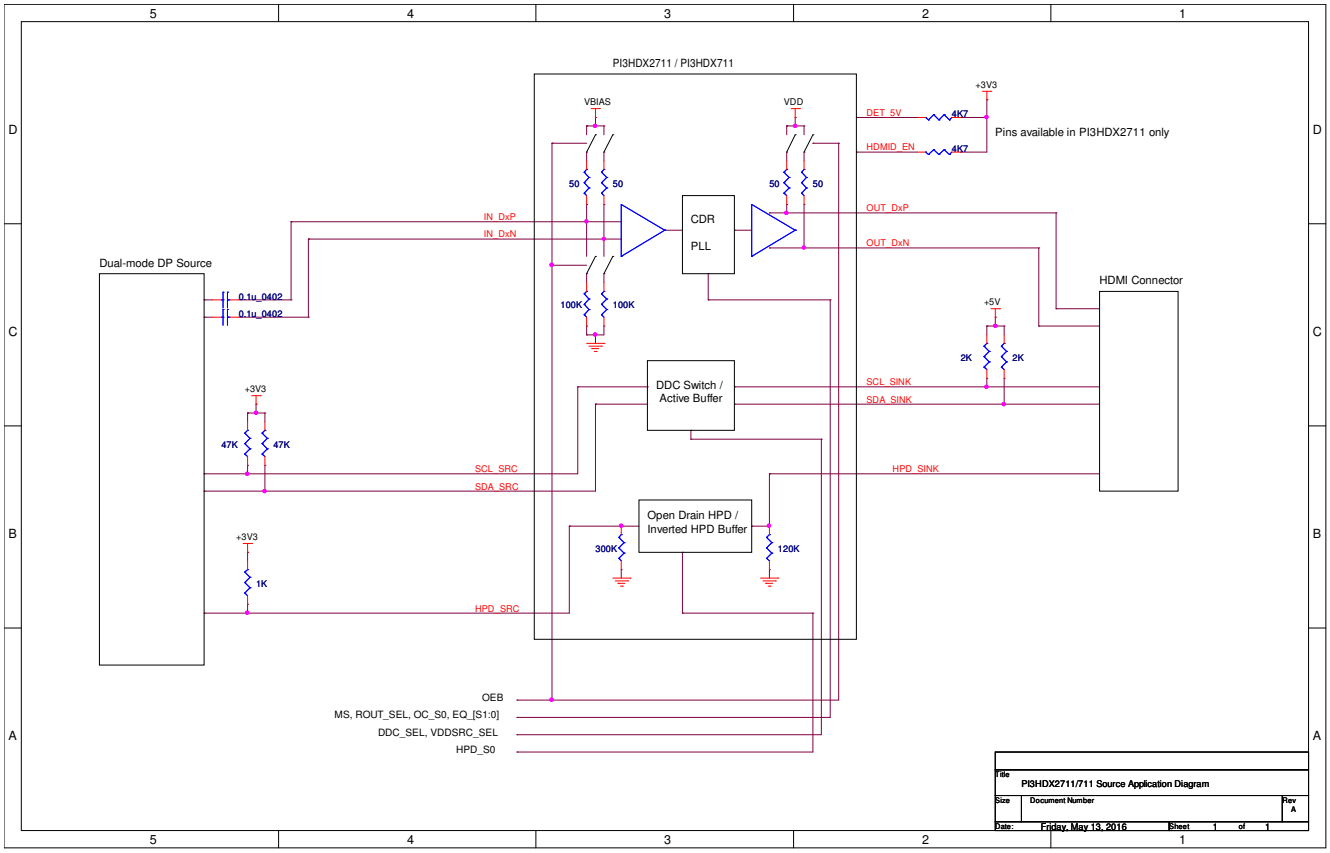
Test condition: PRBS7-1, 1.0V diff Signal Input, 500mV TMDS Out Swing, PE= 0 dB

EQ = 3 dB, PE = 0dB	EQ = 12dB, PE = 0dB
	
48-inch trace board	48-inch trace board
	
96-inch trace board	96-inch trace board

Note: Trace Card dB Loss Informations

Frequency	1.7GHz	3 GHz	Units	Comments
6 inch Input Trace	-1.34	-2.1	dB	Trace card actual image: 
12 inch Input Trace	-2.54	-4.04	dB	
18 inch Input Trace	-3.87	-6.1	dB	
30 inch Input Trace	-6.34	-10.14	dB	
36 inch Input Trace	-7.54	-12.13	dB	
48 inch Input Trace	-10.21	-16.42	dB	

6.3 Application Reference Schematics



6.4 Layout Guidelines

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

6.4.1 Power and Ground

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Pericom high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

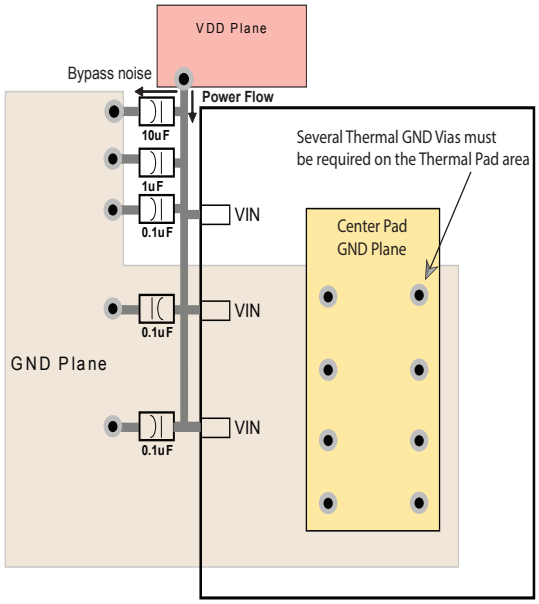


Figure 6-3 Decoupling Capacitor Placement Diagram

6.4.2 High-speed signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

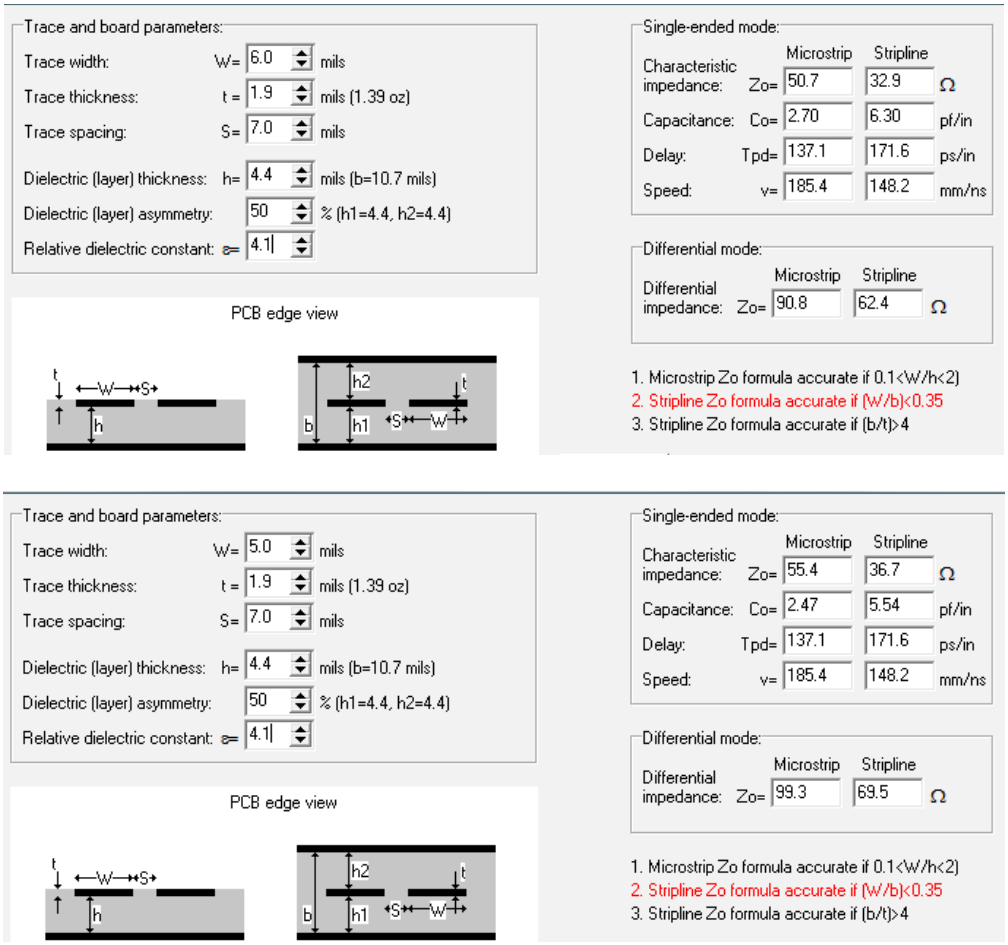


Figure 6-4 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

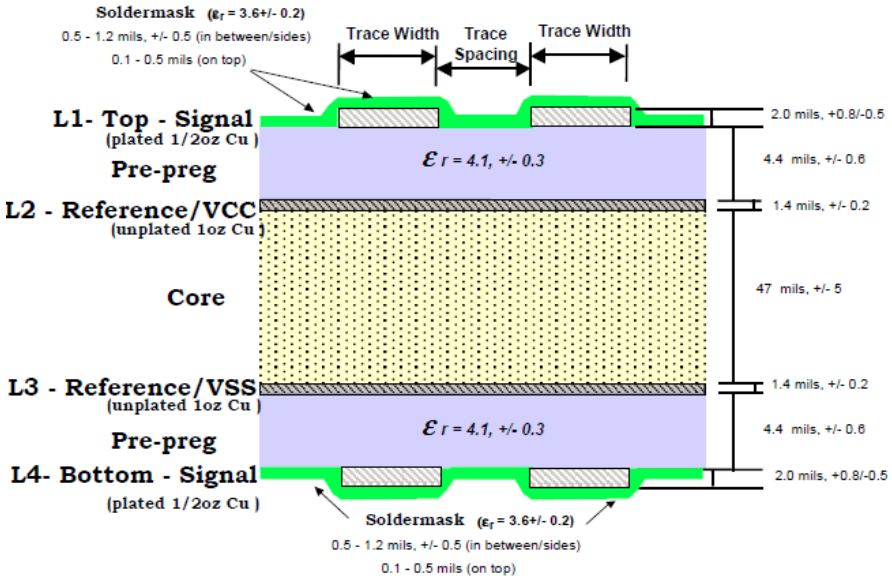


Figure 6-5 4-Layer PCB Stack-up Example

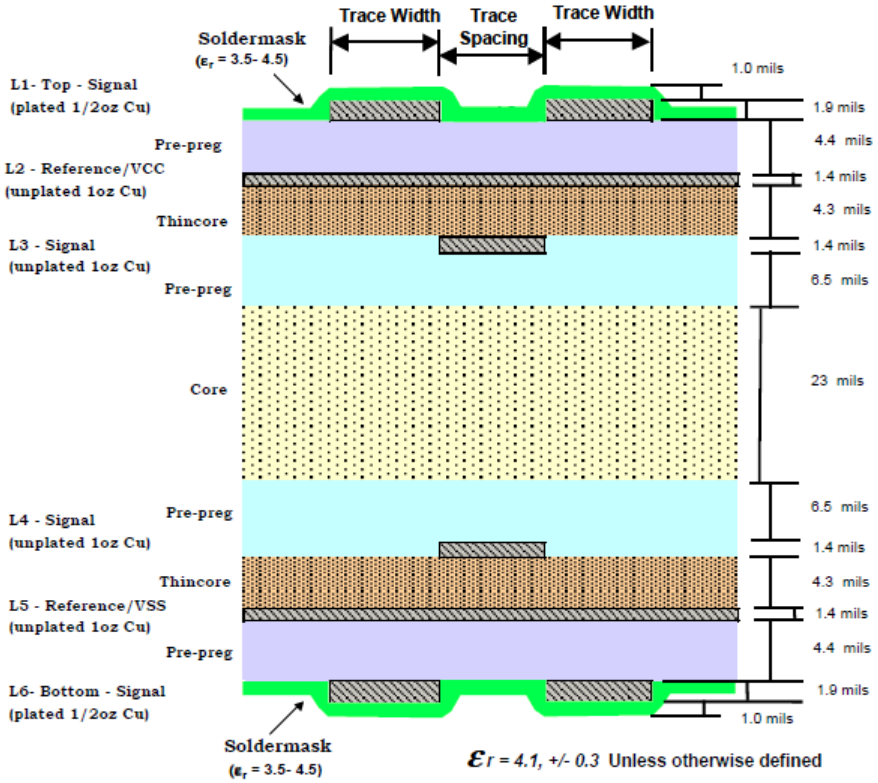


Figure 6-6 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

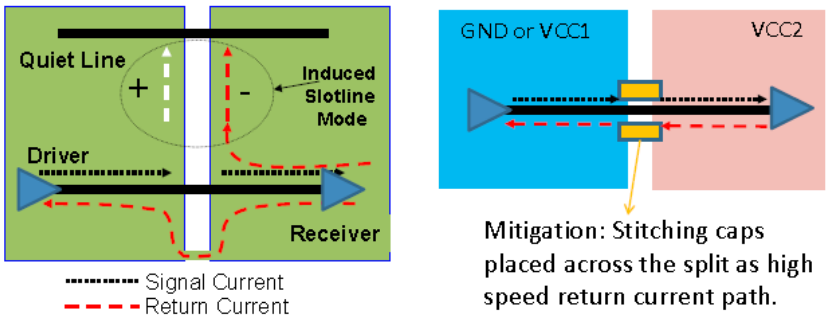


Figure 6-7 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

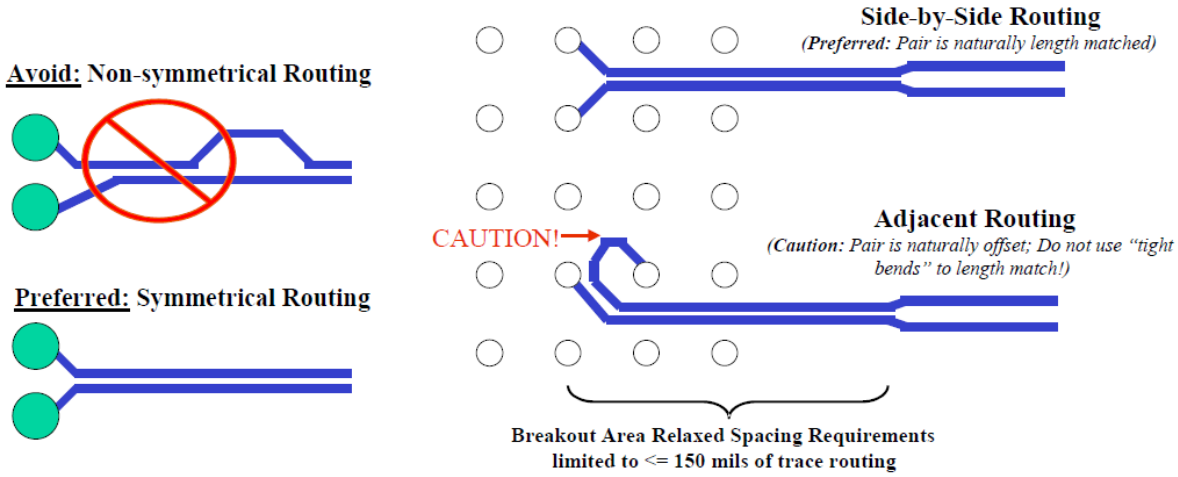


Figure 6-8 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

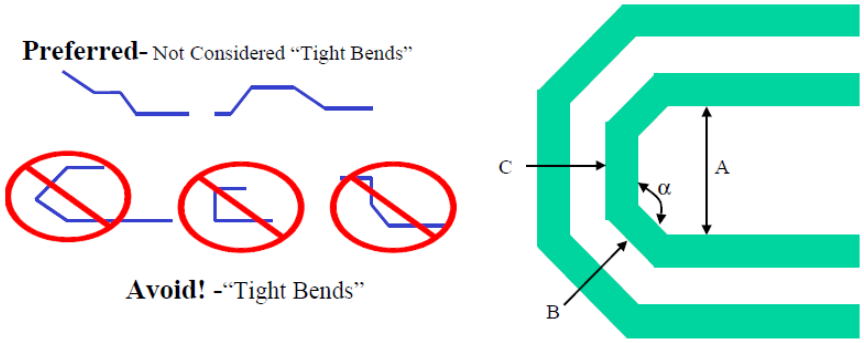


Figure 6-9 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

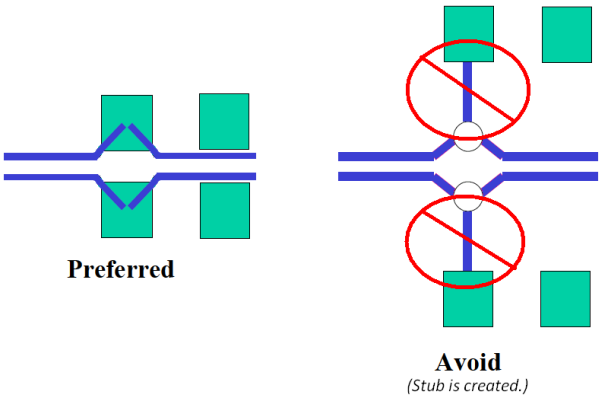


Figure 6-10 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

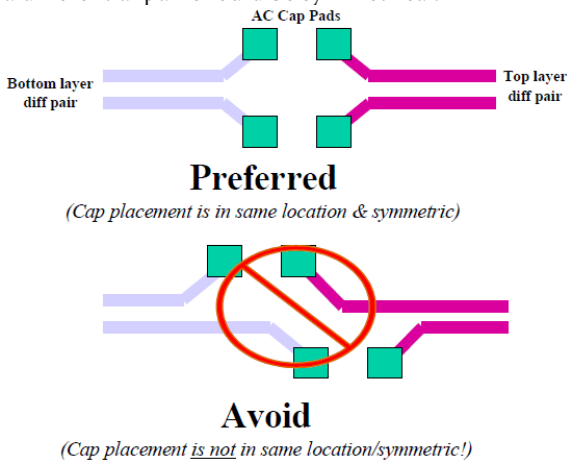


Figure 6-11 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

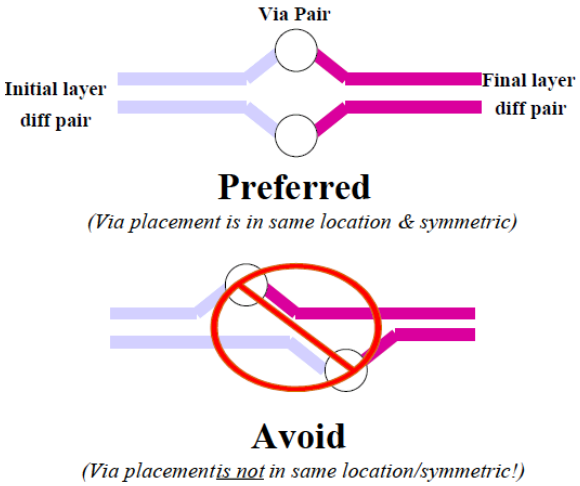


Figure 6-12 Layout Guidance of Stitching Via

6.5 HDMI 2.0 Compliance Test

6.5.1 HDMI 2.0 Compliance Test Set-up

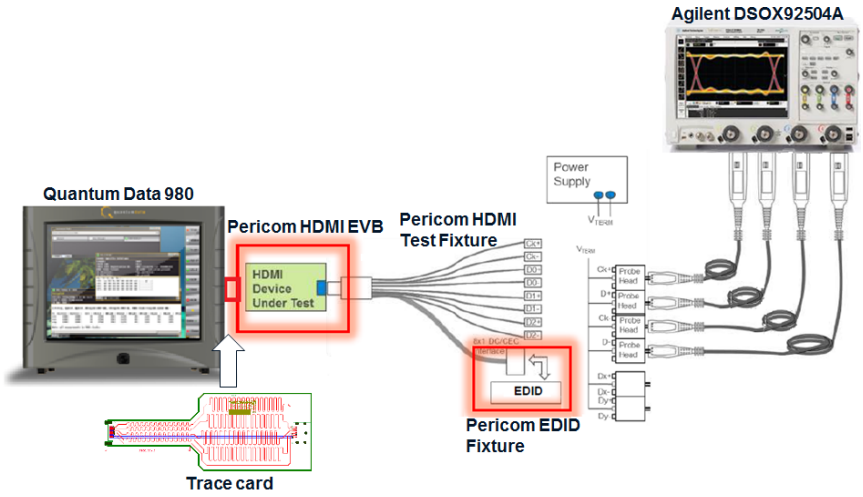


Figure 6-13 HDMI 2.0 CTS test setup*

Note: Application Trace Card Information for CTS test

HDMI FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 3Gbps	-2.96 dB	-4.88 dB	-5.24 dB	-6.53 dB	-7.94 dB	-8.49 dB	-10.60 dB

6.5.2 HDMI 1.4 CTS Test Report

HDMI Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.20.0013
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (18 FEB 2015 11:16:48), Using Cal Atten (5.7831E+000) Skew: Calibrated (18 FEB 2015 11:16:56), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (18 FEB 2015 11:19:29), Using Cal Atten (5.5882E+000) Skew: Calibrated (18 FEB 2015 11:13:57), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (18 FEB 2015 11:15:19), Using Cal Atten (5.7320E+000) Skew: Calibrated (18 FEB 2015 11:15:29), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (18 FEB 2015 11:11:30), Using Cal Atten (5.5123E+000) Skew: Calibrated (18 FEB 2015 11:12:12), Using Cal Skew
Last Test Date	2016-05-20 13:29:20 UTC +08:00

Summary of Results

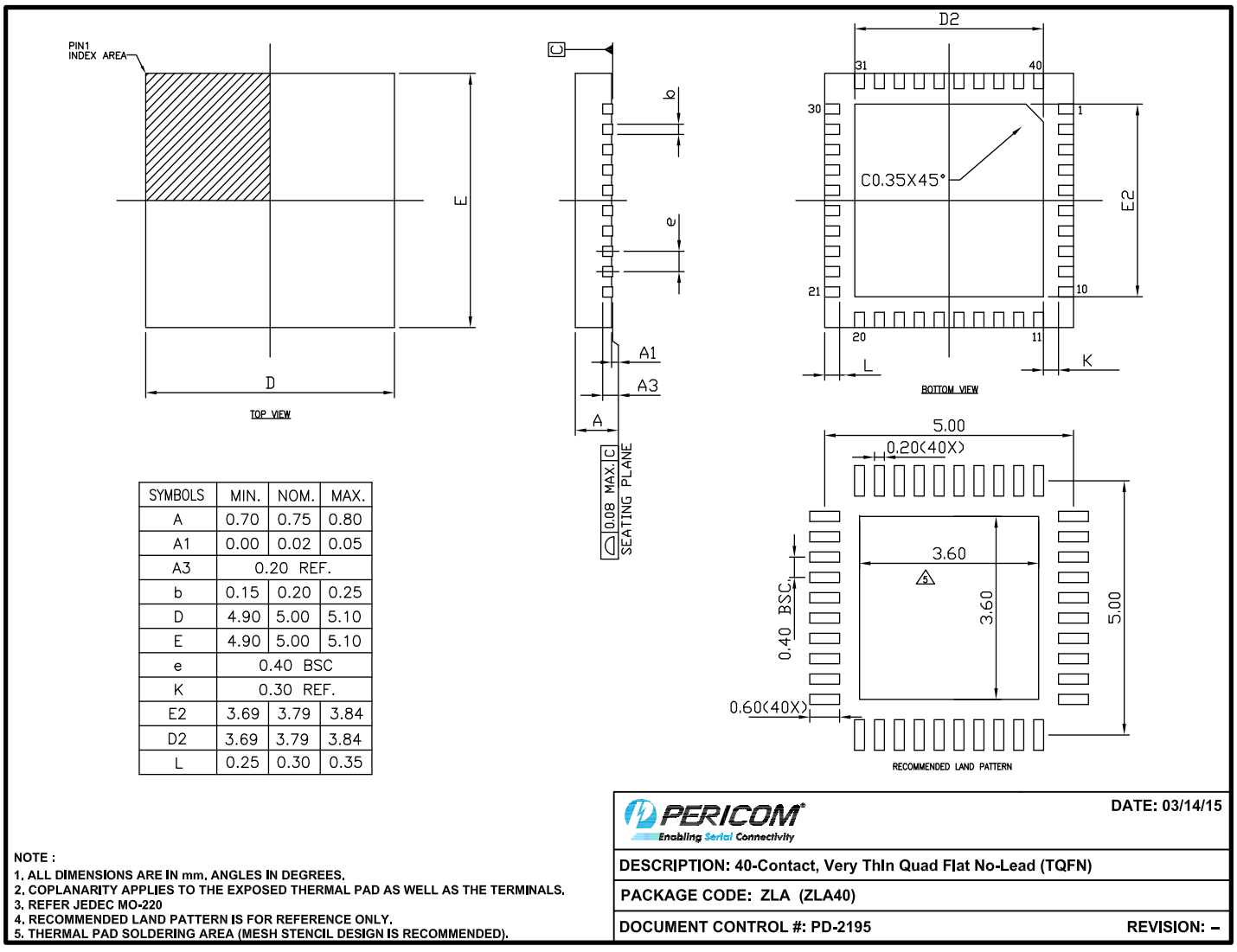
Test Statistics	
Failed	0
Passed	19
Total	19

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	7-9: Clock Jitter	125 mTbit	50.0 %	VALUE <= 250 mTbit
✓	0	1	7-4: Clock Rise Time	152.452 ps	103.3 %	VALUE >= 75.000 ps
✓	0	1	7-4: Clock Fall Time	150.827 ps	101.1 %	VALUE >= 75.000 ps
✓	0	1	7-8: Clock Duty Cycle(Minimum)	50.940	27.4 %	>=40%
✓	0	1	7-8: Clock Duty Cycle(Maximum)	51.380	14.4 %	<=60%
✓	0	1	7-10: D0 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D0 Data Jitter	149 m	50.3 %	<=0.3Tbit
✓	0	1	7-4: D0 Rise Time	110.125 ps	46.8 %	VALUE >= 75.000 ps
✓	0	1	7-4: D0 Fall Time	105.050 ps	40.1 %	VALUE >= 75.000 ps
✓	0	1	7-2: VL Clock +	2.841 V	19.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL Clock -	2.840 V	20.0 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Clock	86 mTbit	21.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-2: VL D0+	2.843 V	19.0 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D0-	2.849 V	17.0 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 0	39 mTbit	37.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-3: Voff Clock +	-2 mV	40.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff Clock -	-2 mV	40.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff D0+	-4 mV	30.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff D0-	-3 mV	35.0 %	-10 mV <= VALUE <= 10 mV

7. Mechanical, Ordering Information

7.1 Mechanical Outline



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.40 BSC	
K		0.30 REF.	
E2	3.69	3.79	3.84
D2	3.69	3.79	3.84
L	0.25	0.30	0.35

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity

DATE: 03/14/15

DESCRIPTION: 40-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZLA (ZLA40)

DOCUMENT CONTROL #: PD-2195 REVISION: –

Figure 7-1 Package Outline

7.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an “add mark” operation which places the speed code letter at the end of the complete part number.

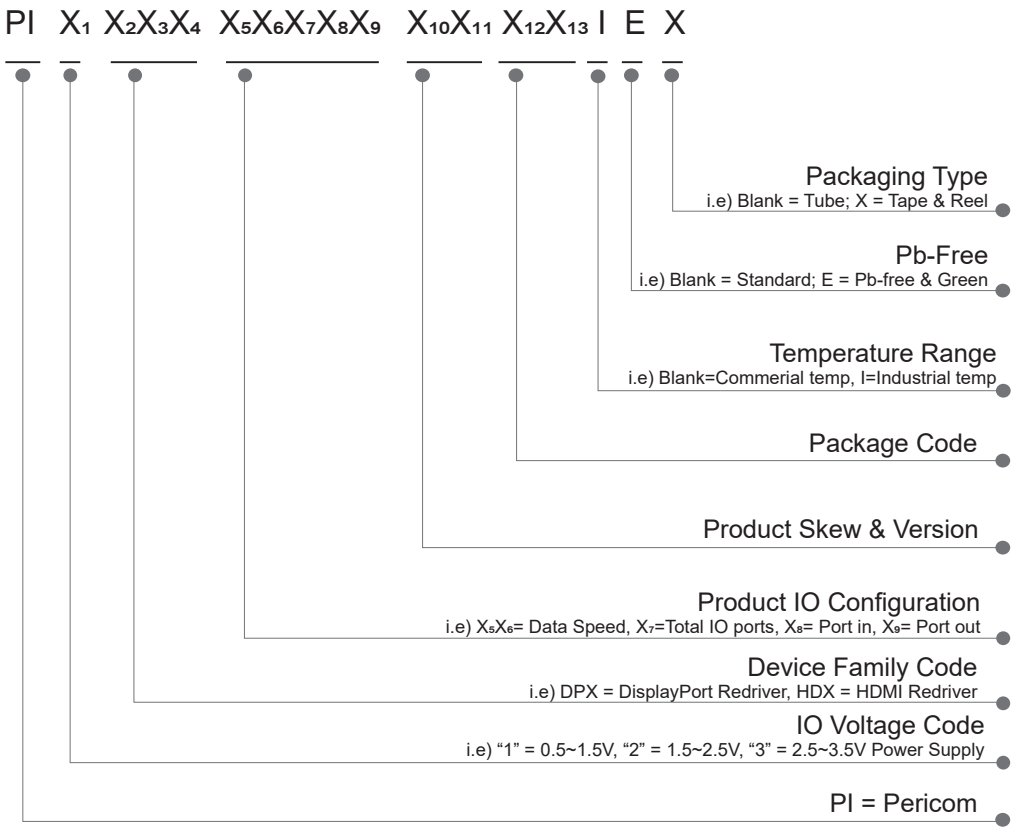


Figure 7-2 Part naming information

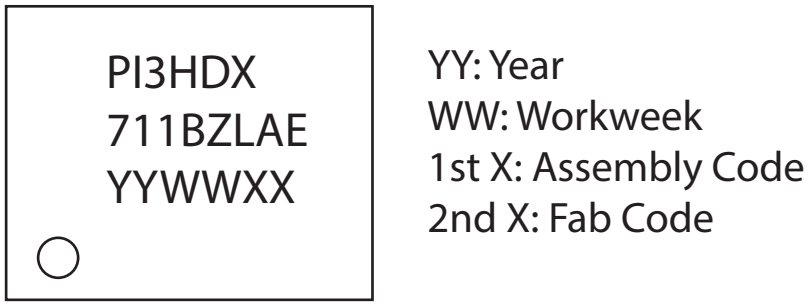


Figure 7-3 Package marking information

7.3 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film.The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

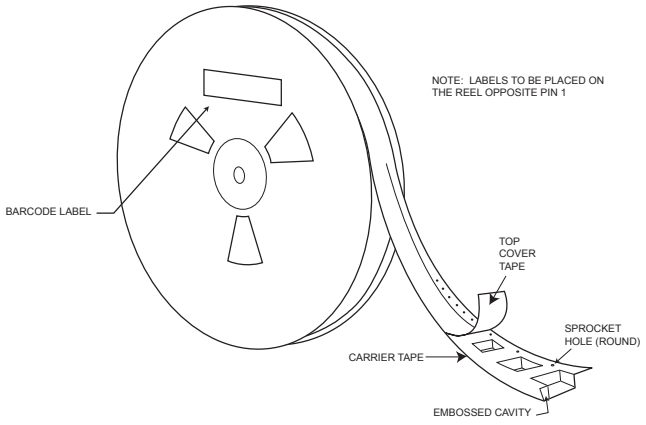


Figure 7-4 Tape & Reel label information

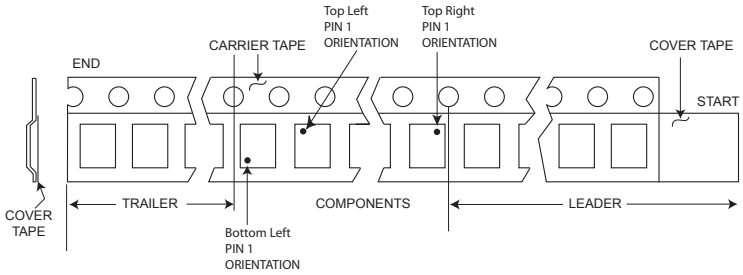


Figure 7-5 Tape leader and trailer pin 1 orientations

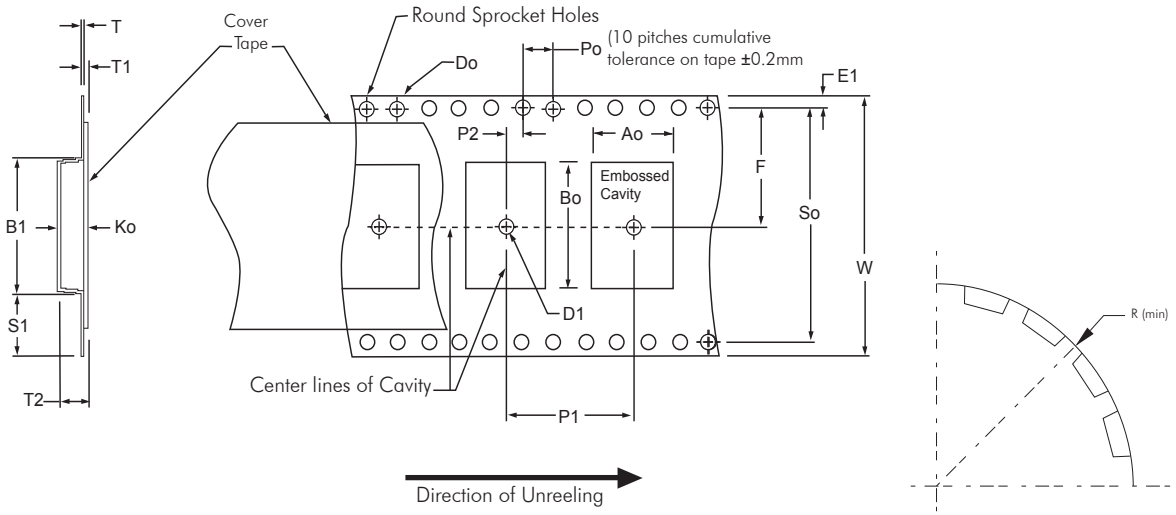


Figure 7-6 Standard embossed carrier tape dimensions

Table 7-1. Constant Dimensions

Tape Size	D0	D1 (Min)	E1	P0	P2	R (See Note 2)	S1 (Min)	T (Max)	T1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Table 7-2. Variable Dimensions

Tape Size	P1	B1 (Max)	E2 (Min)	F	So	T2 (Max.)	W (Max)	A0, B0, & K0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

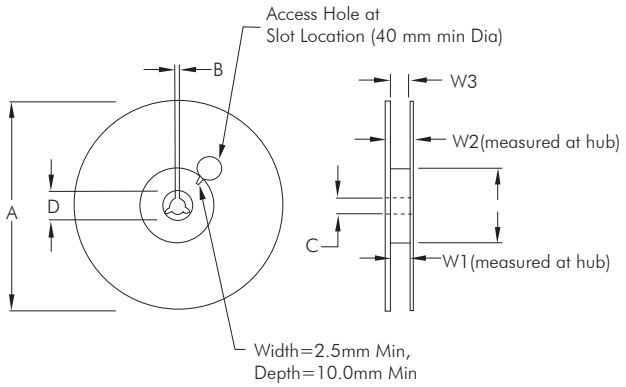


Table 7-3. Reel dimensions by tape size

Tape Size	A	N (Min) See Note A	W1	W2(Max)	W3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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