A Product Line of
Diodes Incorporated

PI3USB31532Q

10Gbps USB Type-C DP2.1/USB3 6:4 Crossbar Switch

Description

The DIODES PI3USB31532Q is a 6:4 differential channels, bidirectional, 10Gbps crossbar switch solution for routing USB 3.2 and/or DP 2.1 signals through USB Type-C® connector. It supports either one lane of USB 3.2 Gen 2, one lane of USB 3.2 Gen 2 and two channels of DP 2.1 UHBR10, or four channels of DP 2.1 UHBR10 to the USB Type-C connector.

In addition, AUX± channels are also switch to the USB Type-C sideband pins, SBU1 and SBU2. The PI3USB31532Q offers excellent signal integrity for high-speed signals and low-power dissipation.

Application(s)

- Smart Cockpit
- Rear Seat Entertainment

Application Diagram

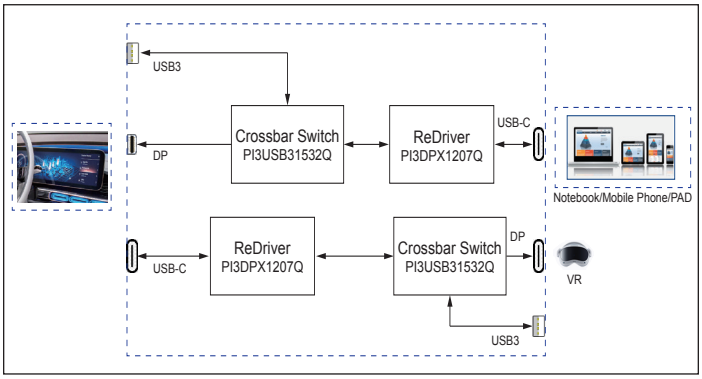


Figure 1. RSE Application

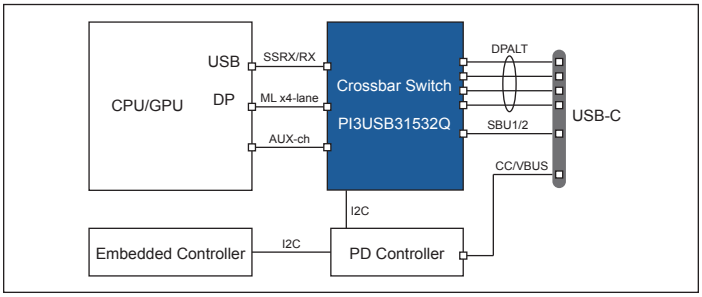


Figure 2. Smart Cockpit Application

Features

- Six Differential Channels to Two/Four Differential Channels Bidirectional Crossbar Switch
- 10Gbps USB 3.2 Gen 2 Super Speed and DP 2.1 UHBR10 Switching to USB Type-C Connector
- Supports Either Pin Control or I²C Control to Configure the Switch
- Low Insertion Loss: -1.7dB @ 10Gb/s
- Return Loss: -15dB @ 10Gb/s
- CrossTalk: -38dB @ 10Gb/s
- Off Isolation: -22dB @ 10Gb/s
- -3dB Bandwidth: 8.3GHz
- Multiplexes One of the Following to USB Type-C Connector:
  - USB 3.2 Gen 2 Signal Only
  - One Lane of USB 3.2 Gen 2 Signal and Two Channels of DP 2.1 UHBR10
  - Four Channels of DP2.1 UHBR10
- With DP 2.1 UHBR10 Operating, AUX+ and AUX- are switch to SBU Pins
- Power Supply: 3.3V
- AEC-Q100 Grade 2, -40°C to 105°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The PI3USB31532Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 40-contact, TQFN (ZLC)

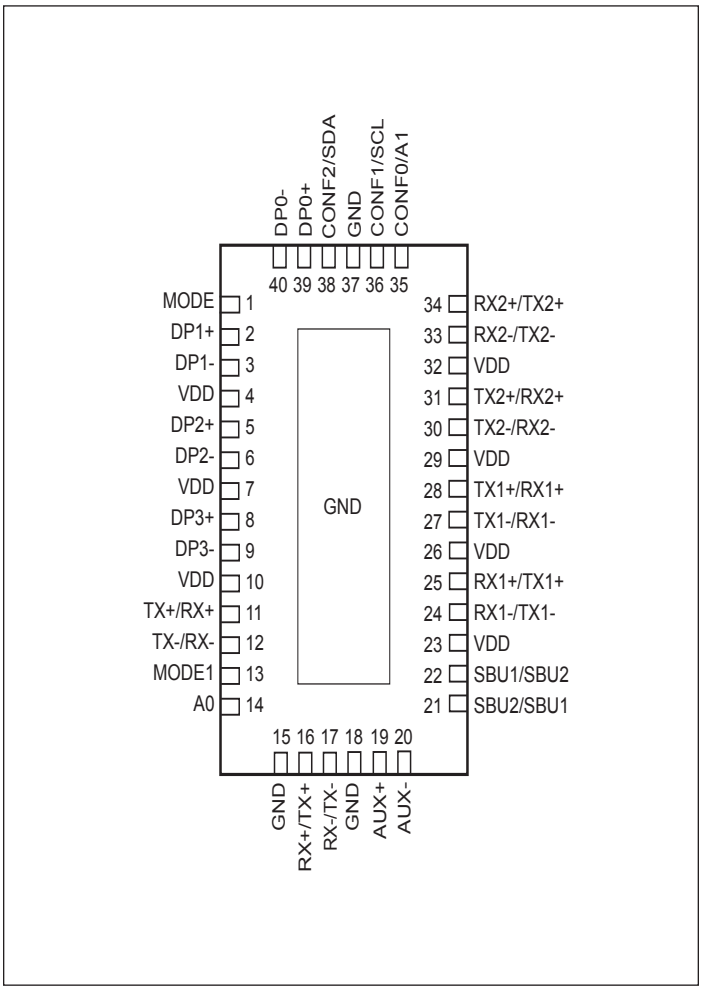
Ordering Information

Ordering Code	Packaging Code	Package Description
PI3USB31532Q2ZLCEX	ZLC	40-Pin, 3mm x 6mm (TQFN) (W-QFN3060-40)

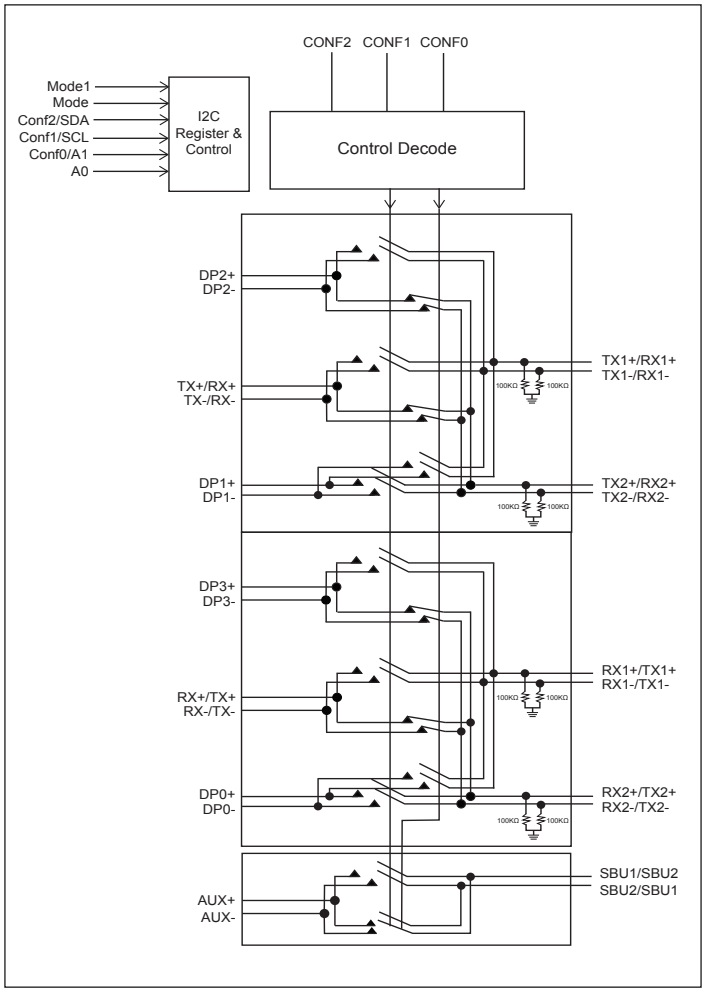
Notes:
- Q = Automotive Compliant
- 2 = AEC-Q100 Grade Level
- E = Pb-free and Green
- X suffix = Tape/Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q100 qualified and are PPAP capable. Refer to https://www.diodes.com/quality/.

Pin Configuration



Block Diagram



Note:

1. The first pinout name (such as *RX2+* in *RX2+/TX2+*) is for source reference schematic in page 4.
2. The second pinout name (such as *TX2+* in *RX2+/TX2+*) is for sink reference schematic in page 5.

Pin Description

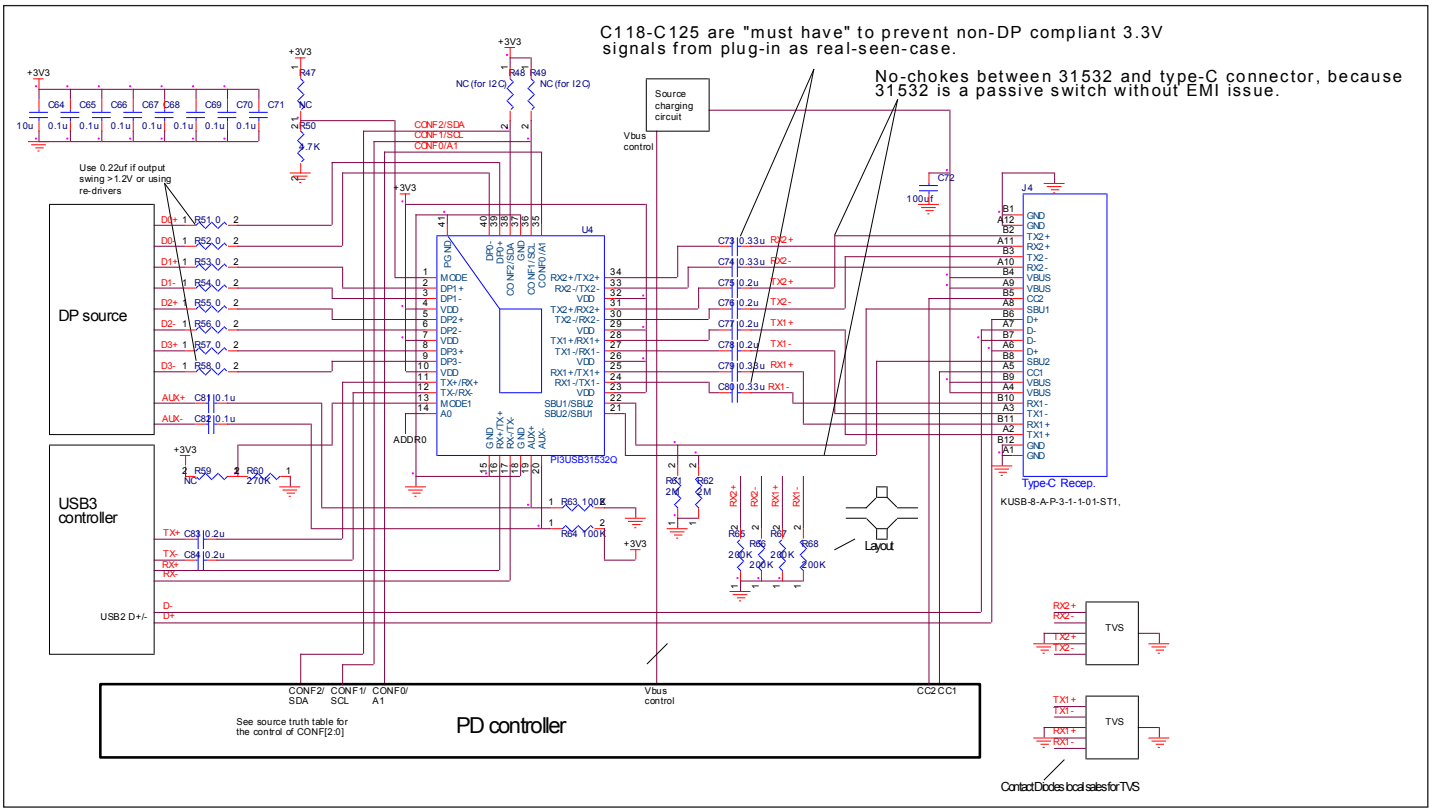
Pin#	Pin Name	Type	Description
4, 7, 10, 23, 26, 29, 32	VDD	Power	3.0V to 3.6V power supply. All V_{DD} pins must be tied to external power.
11, 12	TX+/RX+, TX-/RX-	I/O	Differential USB 3.2 Gen 2 Transmit signal (source application) or differential USB 3.2 Gen 2 Receive signal (sink application). Connected internally with 100kΩ pulldown to GND.
16, 17	RX+/TX+, RX-/TX-	I/O	Differential USB 3.2 Gen 2 Receive signal (source application) or differential USB 3.2 Gen 2 Transmit signal (sink application). Connected internally with 100kΩ pulldown to GND.
39, 40	DP0+, DP0-	I/O	Differential DP0 signal.
2, 3	DP1+, DP1-	I/O	Differential DP1 signal.
5, 6	DP2+, DP2-	I/O	Differential DP2 signal.
8, 9	DP3+, DP3-	I/O	Differential DP3 signal.
19, 20	AUX+, AUX-	I/O	Differential Auxiliary signal for DP.
22, 21	SBU1, SBU2	I/O	Sideband signal at Type-C connector.
25, 24	RX1+/TX1+, RX1-/TX1-	I/O	Differential Receive signal 1 at Type-C connector (source application) or differential Transmit signal 1 at Type-C connector (sink application).
28, 27	TX1+/RX1+, TX1-/RX1-	I/O	Differential Transmit signal 1 at Type-C connector (source application) or differential Receive signal 1 at Type-C connector (sink application).
31, 30	TX2+/RX2+, TX2-/RX2-	I/O	Differential Transmit signal 2 at Type-C connector (source application) or differential Receive signal 2 at Type-C connector (sink application).
34, 33	RX2+/TX2+, RX2-/TX2-	I/O	Differential Receive signal 2 at Type-C connector (source application) or differential Transmit signal 2 at Type-C connector (sink application).
22	SBU1/SBU2	I/O	Sideband signal 1 (source application) or side band signal 2 (sink application) at Type-C connector.
21	SBU2/SBU1	I/O	Sideband signal 2 (source application) or side band signal 1 (sink application) at Type-C connector.
1	MODE	I	Control mode selection MODE = 1, I2C control = 0, pin control through CONF[2:0]
35, 36, 38	CONF[2:0]	I	Switch configuration selection pin when MODE = 0, refer to *Switch Selection Truth Table* for detail. When MODE = 1, these pins are part of the I2C interface as SDA/SCL/A1.
38	SDA	I/O	Serial in data of I2C when MODE = 1.
36	SCL	I	I2C clock input pin when MODE = 1.
35	A1	I	A[1] of A[1:0] I2C selectable address when MODE = 1.
14	A0	I	A[0] of A[1:0] I2C selectable address when MODE = 1.
15, 18, 37, Center Pad	GND	Power	Ground supply.
13	MODE1	I	When MODE 1 = 0, I2C I/O is 1.8V interface. When MODE 1 = 1, I2C I/O is 3.3V interface.

Configuration Table for Source Application (V1.0a)

			Type-C USB 3.2 Gen 1/Gen 2 only		V1.0a DP ALT Spec Receptacle DFP_D pin Assignment			
					C, E (Table 3-1)	C, E Flip (Table 3-2)	D, F (Table 3-1)	D, F flip (Table 3-2)
Switch	**Open**	**Open**	**USB 3.2 Gen 1/Gen 2**	**USB 3.2 Gen 1/Gen 2 Flip**	**4 Lanes of DP 2.1 UHBR10**	**4 Lanes of DP 2.1 UHBR10 flip**	**USB 3.2 Gen 1/ Gen 2 +2 Lanes of DP 2.1 UHBR10**	**USB 3.2 Gen 1/Gen 2 +2 Lanes of DP 2.1 UHBR10 Flip**
Conf[2:0]	000	001	100	101	010	011	110	111
TX	x	x	TX1	TX2	x	x	TX1	TX2
RX	x	x	RX1	RX2	x	x	RX1	RX2
DP0	x	x	x	x	RX2	RX1	RX2	RX1
DP1	x	x	x	x	TX2	TX1	TX2	TX1
DP2	x	x	x	x	TX1	TX2	x	x
DP3	x	x	x	x	RX1	RX2	x	x
AUX+	x	x	x	x	SBU1	SBU2	SBU1	SBU2
AUX-	x	x	x	x	SBU2	SBU1	SBU2	SBU1

000 = switch open with power down

001 = switch open only, no power down



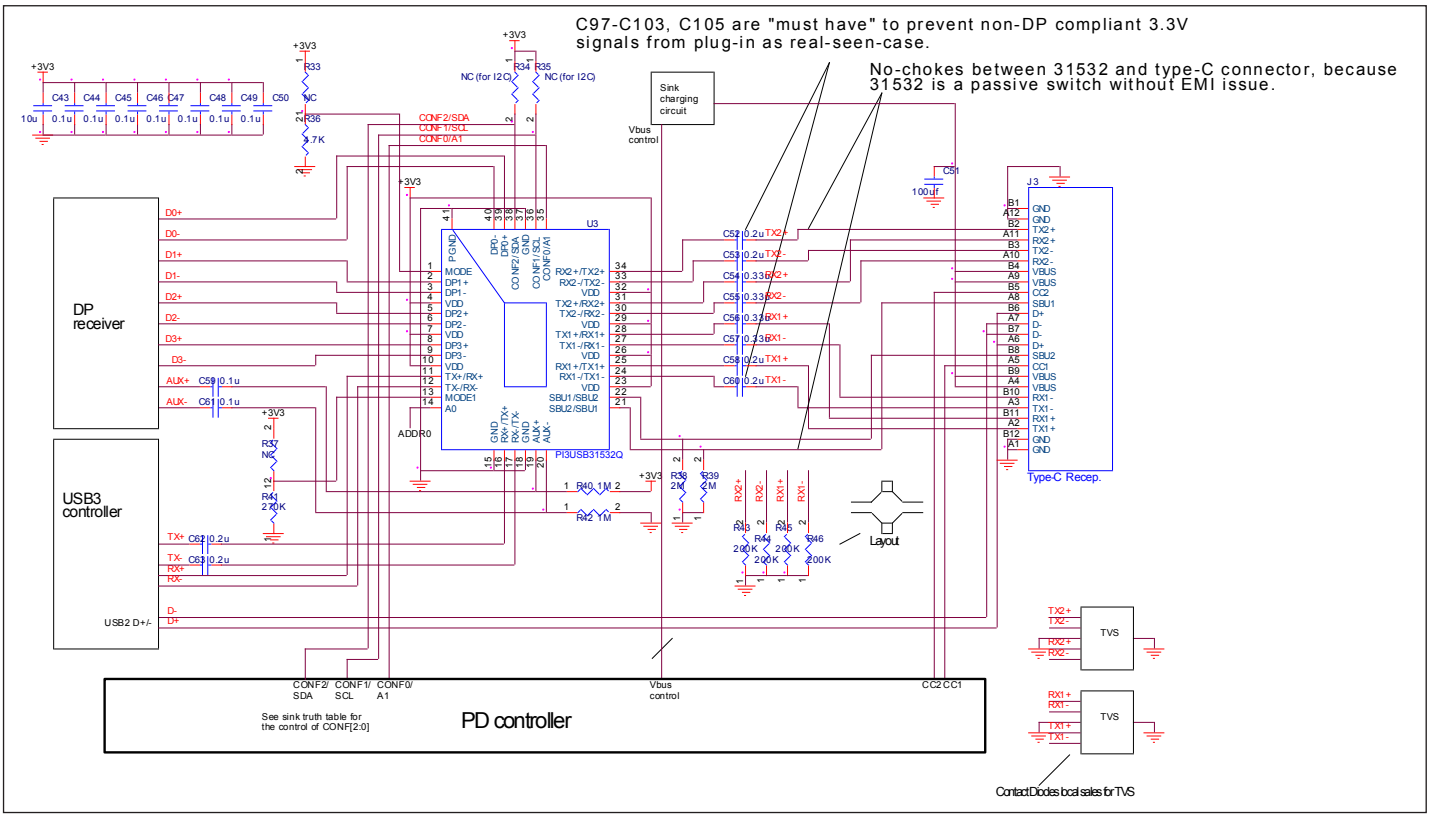
PI3USB31532Q Reference Schematic for Source Application

Configuration Table for Sink Application (V1.0a)

			Type-C USB 3.2 Gen 1/Gen 2 Only		V1.0a DP ALT Spec Receptacle UFP_D pin Assignment			
					C (Table 3-3)	C Flip (Table 3-4)	D (Table 3-3)	D Flip (Table 3-4)
Switch	Open	Open	USB 3.2 Gen 1/Gen 2	USB 3.2 Gen 1/Gen 2 Flip	4 Lanes of DP 2.1 UHBR10	4 Lanes of DP 2.1 UHBR10 flip	USB 3.2 Gen 1/ Gen 2 +2 Lanes of DP 2.1 UHBR10	USB 3.2 Gen 1/Gen 2 +2 Lanes of DP 2.1 UHBR10 Flip
Conf[2:0]	000	001	100	101	010	011	110	111
TX	x	x	TX1	TX2	x	x	TX1	TX2
RX	x	x	RX1	RX2	x	x	RX1	RX2
DP0	x	x	x	x	TX2	TX1	TX2	TX1
DP1	x	x	x	x	RX2	RX1	RX2	RX1
DP2	x	x	x	x	RX1	RX2	x	x
DP3	x	x	x	x	TX1	TX2	x	x
AUX+	x	x	x	x	SBU2	SBU1	SBU2	SBU1
AUX-	x	x	x	x	SBU1	SBU2	SBU1	SBU2

000 = switch open with power down

001 = switch open only, no power down



PI3USB31532Q Reference Schematic for Sink Application

I2C Control

** **I2C Function Reference:**

" *THE I2C-BUS SPECIFICATION, VERSION 2.1*"

I2C Control Register:

	Register Bits							
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Slave address (First byte is slave address)	1	0	1	0	1	A1	A0	0/1 (W/R)
Vendor ID (Second byte is vendor ID, read only)	0	0	0	0	0	0	0	0
Selection control (Third byte is for selection control, read/write)	0	0	0	0	0	conf[2]	conf[1]	conf[0]

Note:

1. Bit7 - Bit3 = Version ID (00000) in (01H)
2. Bit2 - Bit0 = Pericom Vendor ID (000) in (01H)
3. A0, A1 are hardware selectable (pin35, pin36)
4. conf[2]/conf[1]/conf[0] are written into the register by the master PI3USB31532Q will decode Bit2 - Bit0 in (02h) for I2C control (Pin1/MODE = 1). Default power-up state is 000.

Bus Transactions

Data transfers follow the format shown in Figure 3 After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit, which is a data direction bit (R/W)—a 'zero' indicates a transmission (WRITE), and a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (S) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

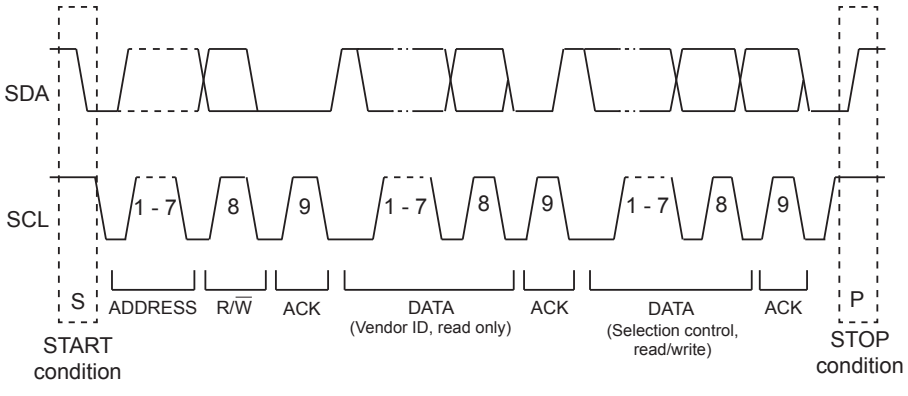


Figure 3. A Complete Data Transfer

Data is transmitted to the PI3USB31532Q registers using the Write mode as shown in Figure 4. Data is read from the PI3USB31532Q registers using the Read mode as shown in Figure A4.

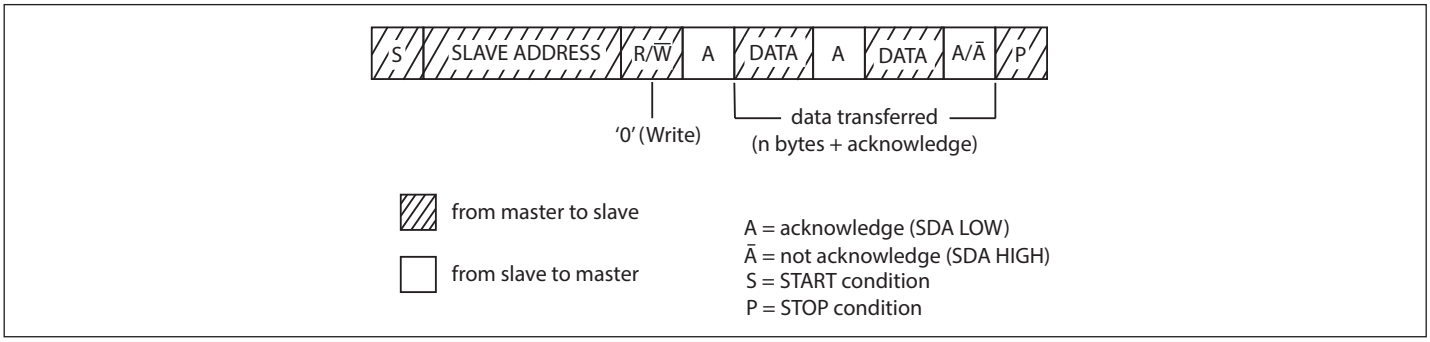


Figure 4. Write to Control Register

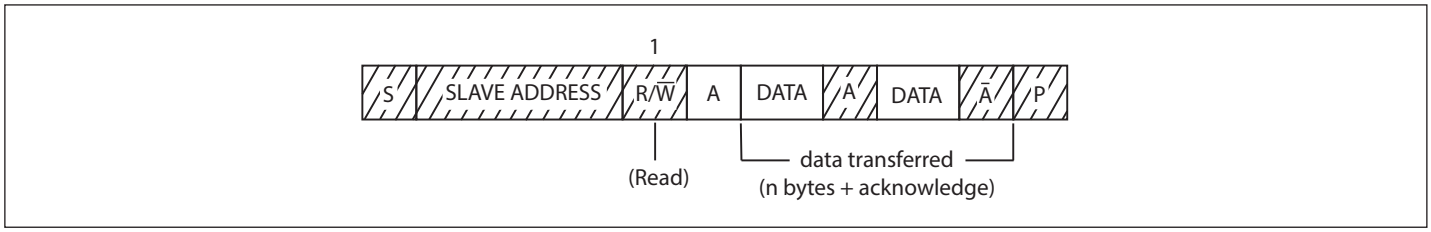


Figure A4. Read to Control Register

The example of PD-I2C Control for PI3USB31532Q, A0=0, A1=0.

	PD-I2C Controlled Registers for PI3USB31532Q		
	DP	**USB3.2**	**USB3.2 + DP**
Non Flip	Start → 10101000 → 00000000 → 00000010 → stop	Start → 10101000 → 00000000 → 00000100 → stop	Start → 10101000 → 00000000 → 00000110 → stop
Flip	Start → 10101000 → 00000000 → 00000011 → stop	Start → 10101000 → 00000000 → 00000101 → stop	Start → 10101000 → 00000000 → 00000111 → stop

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential, V_{DD} = 3.3V ..... -0.3V to 4.3V
Control DC Input ..... -0.3V to V_{DD}+0.3V
Junction Temperature ..... 125°C
Storage Temperature ..... -65°C to +150°C
Channel DC Input for USB, DP ..... -0.3V to 1.2V
Channel DC Input for AUX ..... -0.35V to VDD
ESD, HBM ..... ±2000V
ESD, CDM ..... ±1000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+105	°C
Power Supply Voltage (Measured in Respect to GND)	3.0	3.3	3.6	V

Static Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_{DD}	VDD Supply Current	VDD = 3.3V all Conf[2:0] states except [000]		350	400	µA
		VDD = 3.3V Conf[2:0] = 000		10	30	µA
I_{OFF}	I/O Leakage When Power is Off	VDD = 0V VIO(USB 3.2 Gen 2) = 0V VIO(DP 2.1) = 0V VIO(AUX) = 0V to 3.6V VIO(SBU) = 0V to 3.6V			50	µA
Control pin (MODE, MODE1)						
I_{IH}	High-Level Digital Input Current	V_{IH} = VDD VDD = 3.6V			5	µA
I_{IL}	Low-Level Digital Input Current	V_{IL} = GND VDD = 3.6V			5	µA
V_{IH}	High-Level Digital Input Voltage	VDD = 3.6V	0.75 × VDD			V
V_{IL}	Low-Level Digital Input Voltage	VDD = 3.6V			0.6	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Control/I2C pin (A0, A1, SDA, SCL, when MODE = H, MODE1 = H)						
I_{IH}	High-Level Digital Input Current	V_{IH} = VDD VDD = 3.6V			5	uA
I_{IL}	Low-Level Digital Input Current	V_{IL} = GND VDD = 3.6V			5	µA
V_{IH}	High-Level Digital Input Voltage	VDD = 3.6V	0.75 × VDD			V
V_{IL}	Low-Level Digital Input Voltage	VDD = 3.6V			0.6	V
Control/I2C pin (A0, A1, SDA, SCL, when MODE = H, MODE1 = L)						
I_{IH}	High-Level Digital Input Current	V_{IH} = VDD VDD = 3.6V			5	µA
I_{IL}	Low-Level Digital Input Current	V_{IL} = GND VDD = 3.6V			5	µA
V_{IH}	High-Level Digital Input Voltage	VDD = 3.6V	1.2			V
V_{IL}	Low-Level Digital Input Voltage	VDD = 3.6V			0.4	V
Control pin (CONF[2:0], when MODE = L)						
I_{IH}	High-Level Digital Input Current	V_{IH} = VDD VDD = 3.6V			5	µA
I_{IL}	Low-Level Digital Input Current	V_{IL} = GND VDD = 3.6V			5	µA
V_{IH}	High-Level Digital Input Voltage	VDD = 3.6V	1.2			V
V_{IL}	Low-Level Digital Input Voltage	VDD = 3.6V			0.4	V
I/O pin (TX+, TX-, RX+, RX-, TX1+, TX1-, RX1+, RX1-, TX2+, TX2-, RX2+, RX2-DP0+, DP0-, DP1+, DP1-, DP2+, DP2-, DP3+, DP3-) (AUX+, AUX-, SBU1, SBU2)						
C_{OFF}	USB 3.2 Gen 2/DP 1.4 switch OFF capacitance	VIO = GND f = 1MHz		1.2		pF
C_{ON}	USB 3.2 Gen 2/DP 1.4 switch ON capacitance	VIO = GND f = 1MHz		2.3		pF
C_{OFF}	AUX+/AUX- switch OFF capacitance	VIO = GND f = 1MHz		4.0		pF
C_{ON}	AUX+/AUX- switch ON capacitance	VIO = GND f = 1MHz		7.0		pF
I_{OZL}	I/O leakage for TX_to_TX1/TX2, RX_to_RX1/RX2 DPx_to_TX/RX(x = 0, 1, 2, 3) AUX_to_SBUy(y = 1, 2)	VDD = 3.6V, VIO (USB 3.2 Gen 2) = 0V, VIO (DP 2.1) = 0V, VIO (AUX) = 0V		1	5	µA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OZH}	I/O leakage for TX_to_TX1/TX2, RX_to_RX1/RX2 DPx_to_TX/RX(x = 0, 1, 2, 3) AUX_to_SBUy(y = 1, 2)	VDD = 3.6V, VIO (USB 3.2 Gen 2) = 1.2V, VIO (DP 2.1) = 1.2V, VIO (AUX) = 4.0V		1	15	µA
Linear Region for Analog Switch						
Vp_IO	Linear Region for Analog Switch TX_to_TX1/TX2, RX_to_RX1/RX2 DPx_to_TX/RX(x = 0, 1, 2, 3)	VDD = 3.3V, Ipass = 10mA	1.4	1.6		V
Vp_IOSB	Linear Region for Analog Switch AUX_to_SBUx(x = 1, 2)	VDD = 3.3V, Ipass = 10mA	4.0	4.2		V

Dynamic Characteristics

Min and Max apply for T_A between -40°C to 105°C. Typical values are referenced to T_A = 25°C.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
tstartup	Startup Time	Supply voltage valid or (*) the device is powered up & channel is turn on to its specified characteristics VDD = 3V		10	20	µs
trcfg	Reconfiguration Time	Conf[2:0] change to channel specified operating characteristics		1	2	
tpd	Propagation Delay 1	From input port to output port USB/DP		80		ps
tpd	Propagation Delay 2	From input port to output port AUX		150		ps
tsk	Skew Time 1	From input port to output USB/DP Bit to bit skew		10		ps
tsk	Skew Time 2	From input port to output AUX Bit to bit skew		20		ps
VI_usb_dp	USB/DP Input Signal	USB/DP switch analog signal	-0.3		1.2	V
VI_aux	AUX+/AUX- Input Signal	AUX switch analog signal	-0.35		VDD	V

* Conf[2:0] changes from [000] to [001]/[010]/[011]/[100]/[101]/[110]/[111]

Switch AC Electrical Characteristics

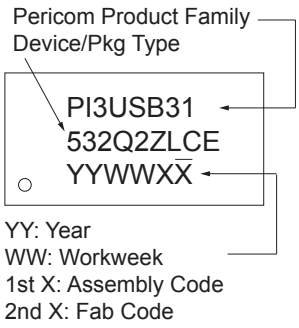
Min and Max apply for T_A between -40°C to 105°C and T_J up to +125°C (unless otherwise noted). Typical values are referenced to T_A = +25°C, V_{DD} = 3.3V.

Symbol	Parameter	Frequency/Vcom		Typ.	Units
BW_USB	-3dB bandwidth of USB 3.2 Gen 2			8.3	GHz
BW_DP	-3dB bandwidth of DP 2.1			6.9	GHz
I_L	Differential Insertion Loss	5GHz/0V	USB 3.2 Gen 2	-1.7	dB
		5Ghz/0V	DP 2.1	-2.3	
		4.05GHz/ 0V	DP 1.4	-1.6	
R_L	Differential Return Loss	5GHz/0V	USB 3.2 Gen 2	-15	
		5Ghz/0V	DP 2.1	-12	
		4.05GHz/ 0V	DP 1.4	-14	
Xtalk	Differential Crosstalk	5GHz/0V	USB 3.2 Gen 2	-38	
		5Ghz/0V	DP 2.1	-30	
		4.05GHz/ 0V	DP 1.4	-33	
Xoff	Off Isolation	5GHz/0V	USB 3.2 Gen 2/DP 2.1	-22	
		4.05GHz/ 0V	DP 1.4	-25	

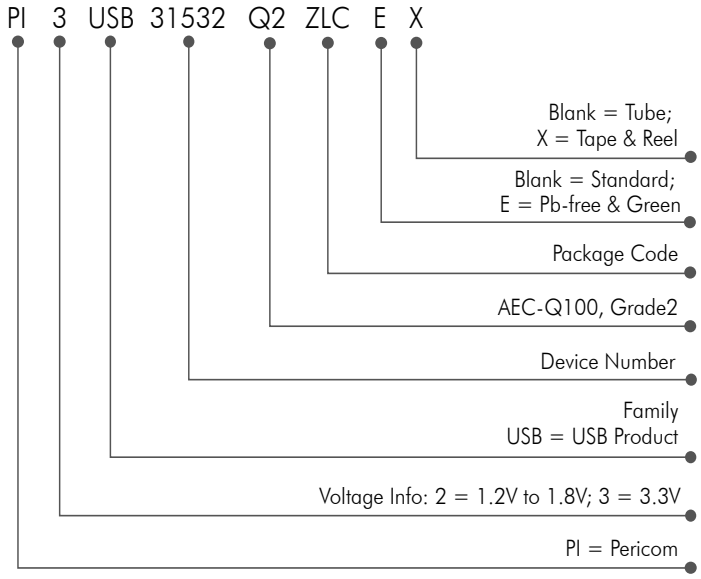
I²C Electrical Characteristics

Symbol	Parameter	Standard Mode (100kHz)		Fast Mode (400kHz)		Fast Mode Plus (1MHz)		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	kHz
$t_{HD:STA}$	Hold Time (repeated) START Condition	4.0		0.6		0.26		µs
t_{LOW}	LOW Period of the SCL Clock	4.7		1.3		0.5		µs
t_{HIGH}	HIGH Period of the SCL Clock	4.0		0.6		0.26		µs
$t_{SET:STA}$	Setup Time for a Repeated START Condition	4.7		0.6		0.26		µs
$t_{HD:DAT}$	Data Hold Time	0	3.45	0	0.9	0	0.33	µs
$t_{SET:DAT}$	Data Setup Time	250		100		50		ns
t_f	Fall Time of both SDA and SCL Signals		300		300		120	ns
t_r	Rise Time of both SDA and SCL Signals		1000		300		120	ns
$t_{SET:STO}$	Setup Time for STOP Condition	4.0		0.6		0.26		µs

Part Marking

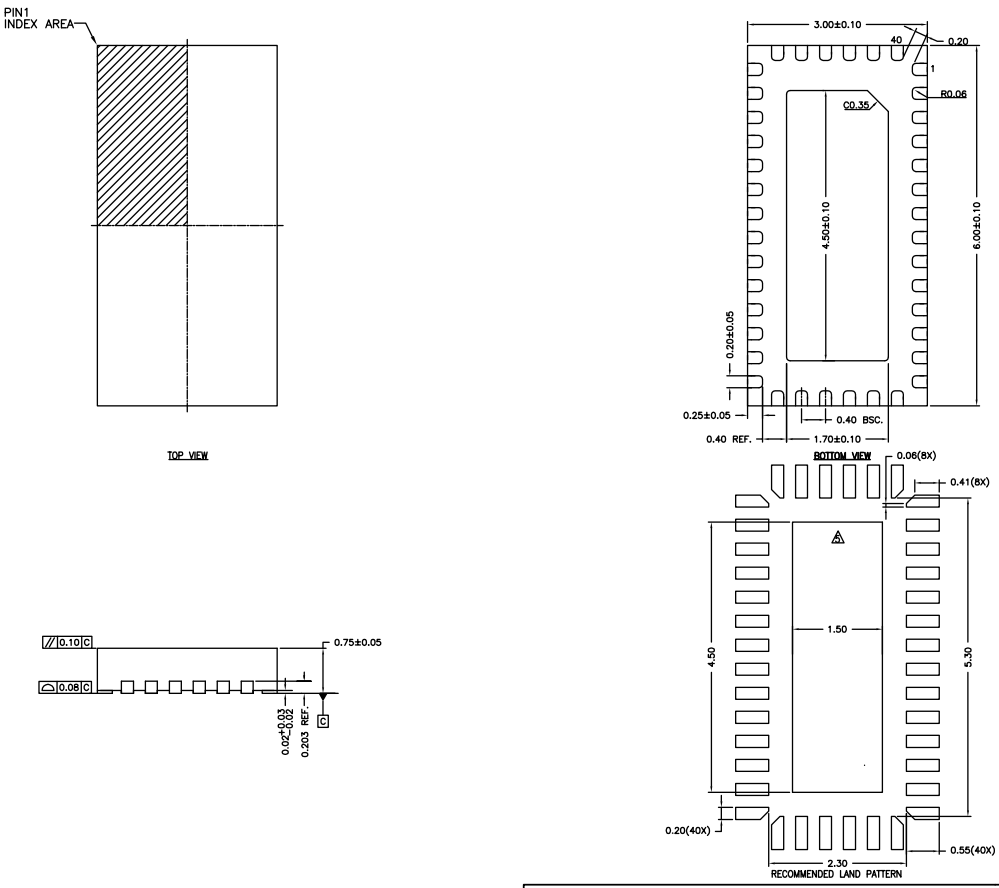


Device Naming Information



Packaging Mechanical

40-TQFN (ZLC)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

	DATE: 07/02/21
DESCRIPTION: 40-Pin, TQFN 3X6mm (W-QFN3060-40)	
PACKAGE CODE: ZLC (ZLC40)	
DOCUMENT CONTROL #: PD-2233	REVISION: A

21-1406

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