

PI3WVR13412A

6Gbps HDMI 2.0 2:1 Video Switch

Description

The PI3WVR13412A is a multi-standard video switch with wide voltage range capability. It supports HDMI 2.0 up to 4K2K@60Hz and emerging and proprietary standard.

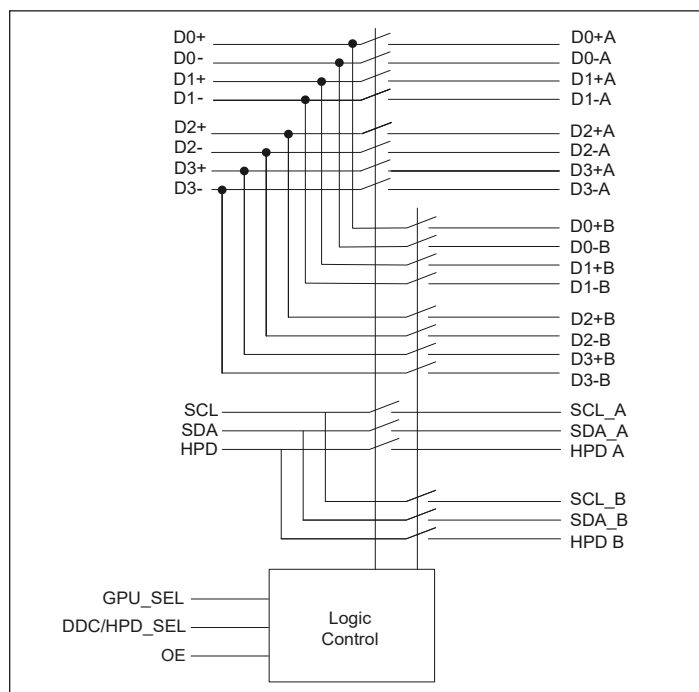
The PI3WVR13412A can pass high-speed signals up to 1.2V peak-to-peak differential with a common-mode voltage from 0 to 3.4V for TMDS signal.

The wide voltage range allows DC-coupled multi-standard operation. Eliminating AC coupling capacitors saves board space and improves signal integrity for dense PCB design. In addition to four high-speed lanes, PI3WVR13412A also switches the DDC and HPD signals using the DDC and HPD channel mux/demux.

Application(s)

- Commercial Displays
- Gaming Monitors
- Docking
- KVMs
- Laptop, AIO PCs

Block Diagram



Features

- HDMI 2.0 Electrical Standard Compatible
- 4-lane, 1:2 and 2:1 Switches
- Data Rate: 6Gbps for High-Speed Channels
- Supports DDC with HPD Channel Mux/Demux at HDMI
- -1.2dB Insertion Loss for High-Speed Channels at 3GHz
- -3dB Bandwidth for High-Speed Channels: 7GHz
- Return loss for High-Speed Channels at 3GHz: -17dB
- Low Crosstalk for High-Speed Channels: -50dB at 3GHz
- Low Off Isolation for High-Speed Channels: -22dB at 3GHz
- Low Channel-to-Channel Skew, 35ps Maximum
- Low Bit-to-Bit Skew, 5ps Typical (between '+' and '-' bits)
- V_{DD} Operating Range: 3.3V ±10%
- Packaging (Pb-free & Green):
 - 42-pin, 3.5mm x 9mm, TQFN (ZH)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.

Ordering Information

Orderable Part Number	Package Code	Package Description
PI3WVR13412AZHEX	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

- E = Pb-free and Green
- X suffix = Tape/Reel

- Notes:**
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration

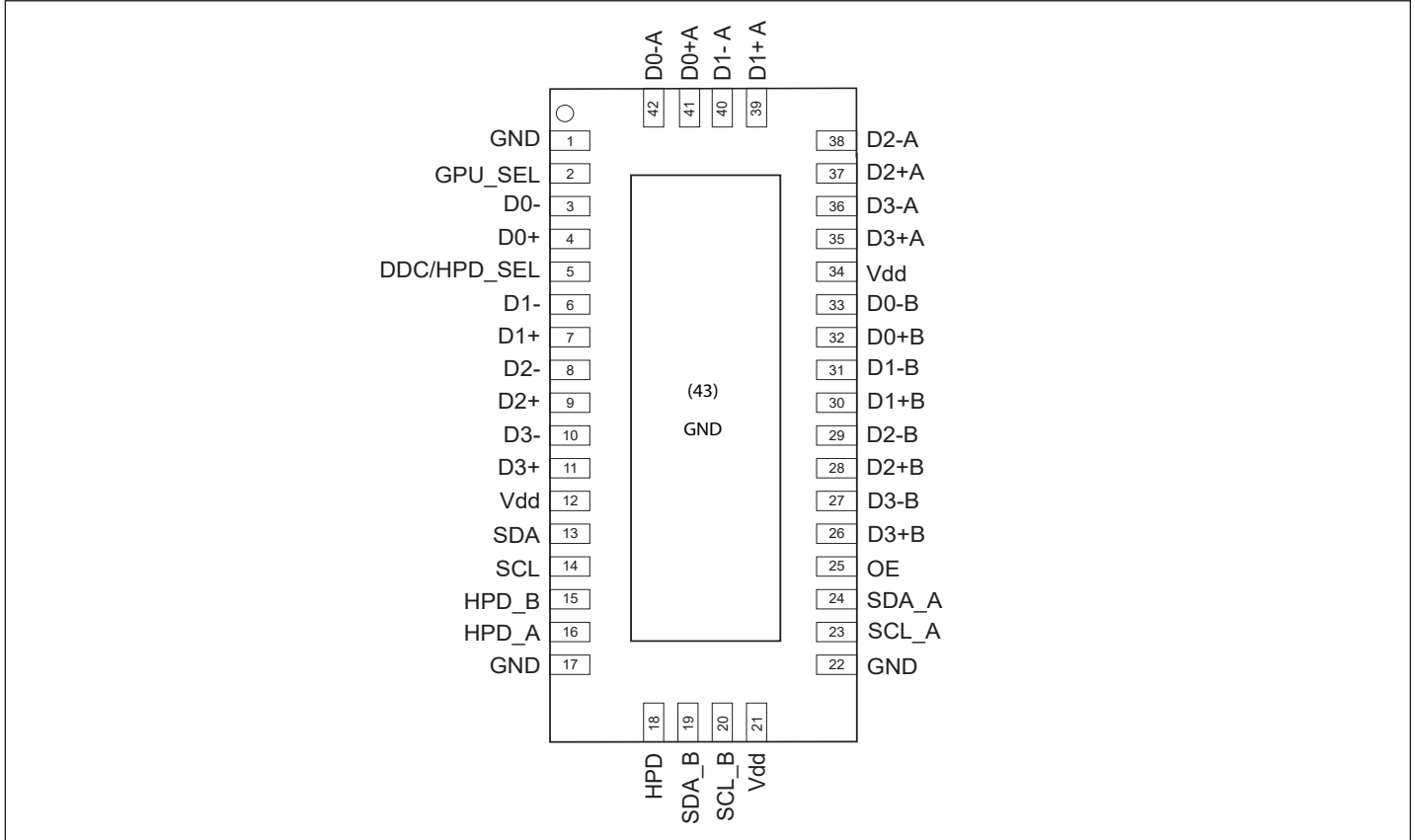


Table 1. Truth Table

Control			Switch Function		
OE	GPU_SEL	DDC/HPD_SEL	D0-D3	DDC	HPD
High	Low	Low	A	DDC A	HPD A
High	Low	High	A	DDC B	HPD B
High	High	Low	B	DDC A	HPD A
High	High	High	B	DDC B	HPD B
Low	x	x	Hi-Z	Hi-Z	Hi-Z

Pin Description

Pin Number	Pin Name	Signal Type	Description
1	GND	Ground	Ground
2	GPU_SEL	I	Switch logic control
3	D0-	I/O	Negative differential signal 0 for COM port
4	D0+	I/O	Positive differential signal 0 for COM port
5	DDC/HPD_SEL	I	Switch logic control for DDC and HPD
6	D1-	I/O	Negative differential signal 1 for COM port
7	D1+	I/O	Positive differential signal 1 for COM port
8	D2-	I/O	Negative differential signal 2 for COM port
9	D2+	I/O	Positive differential signal 2 for COM port
10	D3-	I/O	Negative differential signal 3 for COM port
11	D3+	I/O	Positive differential signal 3 for COM port
12	VDD	Power	3.3V \pm 10% power supply
13	SDA	I/O	SDA signal for DDC COM port
14	SCL	I/O	SCLl signal for DDC COM port
15	HPD_B	I/O	HPD for port B
16	HPD_A	I/O	HPD for port A
17	GND	Ground	Ground
18	HPD	I/O	HPD for COM port
19	SDA_B	I/O	SDA signal for DDC, port B
20	SCL_B	I/O	SCL signal for DDC, port B
21	VDD	Power	3.3V \pm 10% power supply
22	GND	Ground	Ground
23	SCL_A	I/O	SCL signal for DDC, port A
24	SDA_A	I/O	SDA signal for DDC, port A
25	OE	I	Output enable. If OE is high, IC is enabled. If OE is low, IC is powered down and all I/Os are Hi-Z.
26	D3+B	I/O	Positive differential signal 3 for port B
27	D3-B	I/O	Negative differential signal 3 for port B
28	D2+B	I/O	Positive differential signal 2 for port B
29	D2-B	I/O	Negative differential signal 2 for port B
30	D1+B	I/O	Positive differential signal 1 for port B
31	D1-B	I/O	Negative differential signal 1 for port B
32	D0+B	I/O	Positive differential signal 0 for port B
33	D0-B	I/O	Negative differential signal 0 for port B

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Pin Number	Pin Name	Signal Type	Description
34	VDD	Power	3.3V \pm 10% power supply
35	D3+A	I/O	Positive differential signal 3 for port A
36	D3-A	I/O	Negative differential signal 3 for port A
37	D2+A	I/O	Positive differential signal 2 for port A
38	D2-A	I/O	Negative differential signal 2 for port A
39	D1+A	I/O	Positive differential signal 1 for port A
40	D1-A	I/O	Negative differential signal 1 for port A
41	D0+A	I/O	Positive differential signal 0 for port A
42	D0-A	I/O	Negative differential signal 0 for port A
43	Center Pad	Ground	Ground

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Junction Temperature	125°C
Supply Voltage to Ground Potential	-0.5V to +3.8V
DC Input Voltage.....	-0.5V to VDD
High-Speed Channel.....	-0.5V to 4V
HPD_x, SCL_x, SDA_x	-0.5V to 5.5V
ESD: HBM.....	1.5KV
ESD: CDM.....	1KV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Parameter	Description	Min.	Typ. ⁽²⁾	Max.	Units
V _{DD}	Power Supply	3	3.3	3.6	V
V _{DX}	High-Speed Channels Voltage Range	0		4	V
V _{OTHER}	DDC/HPD Channels Voltage Range	0		5.5	V
T _A	Operating Free-air Temperature	0		70	°C

DC Electrical Characteristics for Switching over Operating Range

T_A = 0°C to +70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage (GPU_SEL & OE)	Guaranteed HIGH level	1.5			V
V _{IL}	Input LOW Voltage (GPU_SEL & OE)	Guaranteed LOW level			0.75	
V _{IH_OTHER}	Input HIGH Voltage (DDC/HPD_SEL)	Guaranteed HIGH level	2.7		VDD	V
V _{IL_OTHER}	Input LOW Voltage (DDC/HPD_SEL)	Guaranteed LOW level	-0.5		0.6	V
I _{IH}	Input HIGH Current (All Control Pins)	V _{DD} = Max., V _{IN} = V _{DD}			±1	μA
I _{IL}	Input LOW Current (All Control Pins)	V _{DD} = Max., V _{IN} = GND			±1	
I _{OFF_SB}	I/O Leakage when Part is off for Sideband Signals Only (DDC, HPD)	V _{DD} = 0, V _{INPUT} = 0 to 5.5V			10	
R _{ON_HS}	On Resistance between Input to Output for High-Speed Signals	V _{INPUT,cm} = 0 to 3.4V, V _{INPUT,diff} < 1.2V _{p-p,diff} , V _{DD} = 3.0V, I _{INPUT} = 20mA		8		Ω
R _{ON_DDC}	On Resistance between Input to Output for Sideband Signals (DDC)	V _{DD} = 3.0V, V _{INPUT} = 0 to 3.3V, I _{INPUT} = 20mA		8.8		Ω

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Parameter	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
R _{ON} _HPD	On Resistance between Input to Output for HPD Channel	V _{DD} = 3.0V, V _{INPUT} = 0 to 3.0V, I _{INPUT} = 20mA		8		Ω
I _{OZ} _SB	I/O Leakage for Sideband Signals Only (DDC, HPD)	V _{DD} = 3.6V, V _{INPUT} = 0 to 5.5V			5	μA
C _{in}	Digital input capacitance for control pin	V _{DD} = 3.3V, V _{INPUT} = 0 or V _{DD} , freq = 1MHz		3		pF
C _{on}	Switch ON capacitance	V _{DD} = 3.3V, V _{INPUT} = 0 or V _{DD} , freq = 1MHz		3		pF
C _{off}	Switch OFF capacitance	V _{DD} = 3.3V, V _{INPUT} = 0 or V _{DD} , freq = 1MHz		1.8		pF

Power Supply Characteristics

T_A = 0°C to +70°C

Parameter	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
I _{DD}	Power Supply Current	V _{DD} = 3.3V, V _{IN} = GND or V _{DD}		0.18	0.3	mA
I _{DD,Off}	Power Supply Current, Disabled	V _{DD} = 3.3V, V _{IN} = GND or V _{DD} , V _{OE} = 0		0.1	1	μA

Note:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics over Operating Range

T_A = 0°C to +70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
X _{TALK}	Crosstalk on High-Speed Channels	f = 3GHz		-50		dB
O _{IRR}	OFF Isolation on High-Speed Channels	f = 3GHz		-22		
I _{LOSS}	Differential Insertion Loss on High-Speed Channels	f = 3GHz		-1.2		dB
R _{loss}	Differential Return Loss on High-Speed Channels	f = 3GHz		-17		dB
BW_Dx±	Bandwidth -3dB for Main High-Speed Path (Dx±)			7		GHz
BW_DDC/HPD	-3dB BW for DDC and HPD Signals			2		GHz

Note:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Switching Characteristics

$T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 10\%$

Parameter	Description	Min.	Typ.	Max.	Units
T_{pd}	Propagation Delay (Input pin to Output pin) on all Channels		80	120	ps
tb-b	Bit-to-Bit Skew within the Same Differential Pair of Dx± Channels		5	7	ps
tch-ch	Channel-to-Channel Skew of Dx± Channels			35	ps
Tsw a-b	Switch Time from Port A to Port B			1	μs
Tsw b-a	Switch Time from Port B to Port A			1	μs
Tstartup	V_{DD} Valid to Channel Enable			100	μs
Twakeup	Enabling Output by Changing OE from Low to High			100	μs

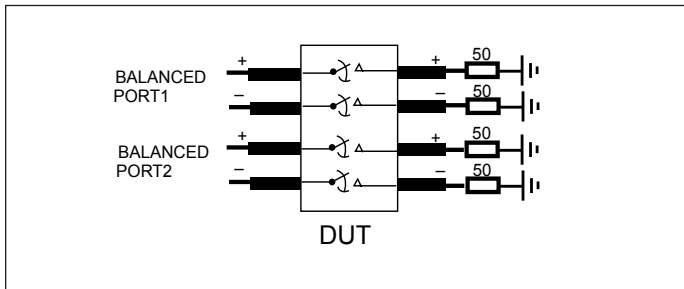


Figure 1. Crosstalk Setup

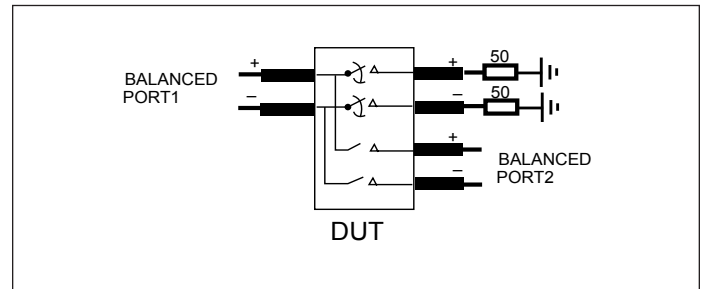


Figure 2. Off-Isolation Setup

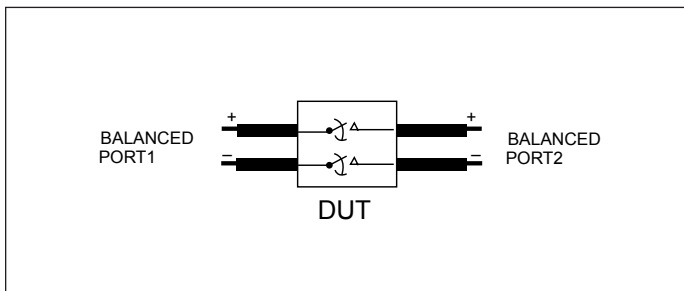


Figure 3. Differential Insertion Loss

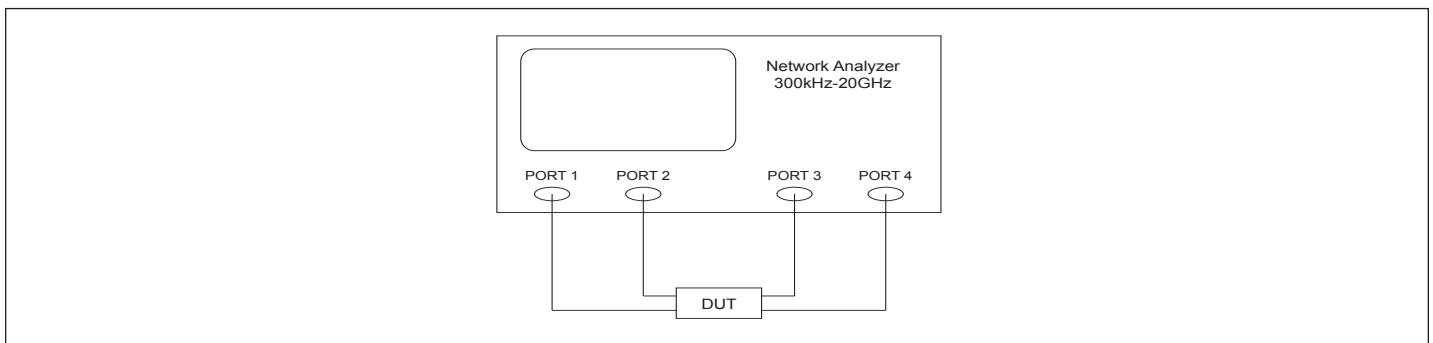
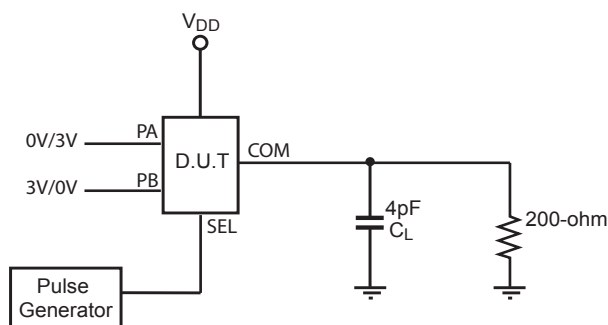


Figure 4. Test Circuit for Dynamic Electrical Characteristics



Notes:

1. C_L = Load capacitance; includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
3. All input impulses are supplied by generators having the following characteristics: $PRR \leq \text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.5\text{ns}$, $t_F \leq 2.5\text{ns}$.
4. The outputs are measured one at a time with one transition per measurement.

Figure 5. Test Circuit for Electrical Characteristics

Switching Waveforms

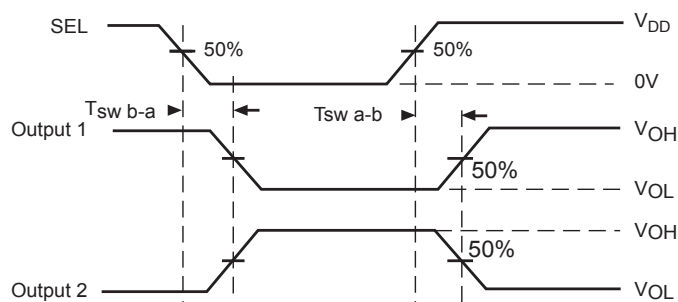


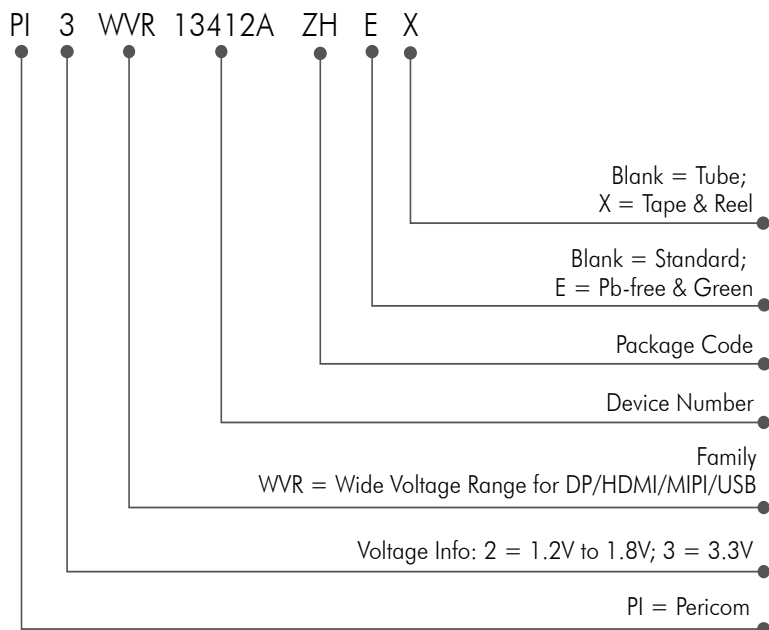
Figure 6. Voltage Waveforms for Select Timing

Table 2. Test Condition

Output 1 Test Condition	Output 2 Test Condition
PA = Low	PA = High
PB = High	PB = Low

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Device Naming Information



Part Marking

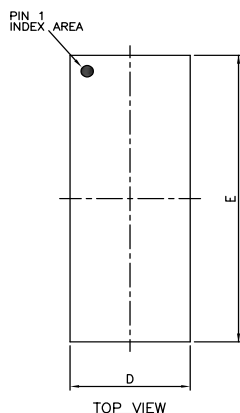


YY: Date Code (Year)
 WW: Date Code (Workweek)
 1st X: Assembly Site Code
 2nd X: Wafer Fab Site Code
 Bar above fab code means Cu wire

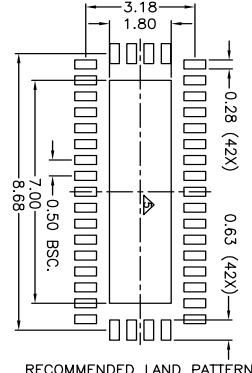
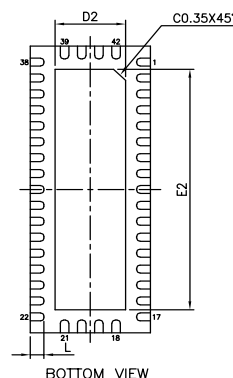
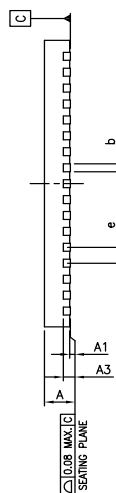
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Packaging Mechanical

42-TQFN (ZH)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	3.40	3.50	3.60
E	8.90	9.00	9.10
e	0.50 BSC		
L	0.30	0.40	0.50
D2	2.00	2.05	2.10
E2	7.50	7.55	7.60



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).
6. DEDICATED ASSEMBLY SITE


DATE: 09/11/23
DESCRIPTION: 42-Contact, Very Thin Quad Flat No-Lead (TQFN)
PACKAGE CODE: ZH (ZH42)
DOCUMENT CONTROL #: PD-2035
REVISION: J

For latest package information:

 See <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>.

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads. Solderable per MIL-STD-202, Method 208 ③
- Weight: 0.073 grams (Approximate)

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