PI3WVR31313A

DP/HDMI 1:3 De-multiplexer switches

Features

- DP/HDMI 1:3 De-multiplexer switch with 4 high speed differential channel and AUX/DDC, HPD and CAB_DET signal channels
- Two passive output ports for DP1.2 at5.4Gbps signals
- One active output port with integrated DP to HDMI re-driver (level shifter) supports HDMI 1.4 at 3.4Gbps
- Pin control mode supports auto port priority selection
- Pin control mode supports port3 with DDC bi-direction buffer switch only
- I2C control mode supports auto port priority selection
- I2C control mode supports port3 with 8 levels equalization and 5 levels pre-emphasis
- I2C control mode supports port3 with either DDC bi-direction buffer switch or DDC passive switch
- Very low operating power when passive port1 and port2 are selected
- 3.3V power supply
- 2KV HBM ESD protection for all I/O pins of port1, port2 and all control pins
- 8kV contact ESD (IEC61000-4-2) protection for all output pins in port3
- Packaging:
  60 pin TQFN package (5x9mm, 0.4mm pitch)
- Support Type2 cable ID register

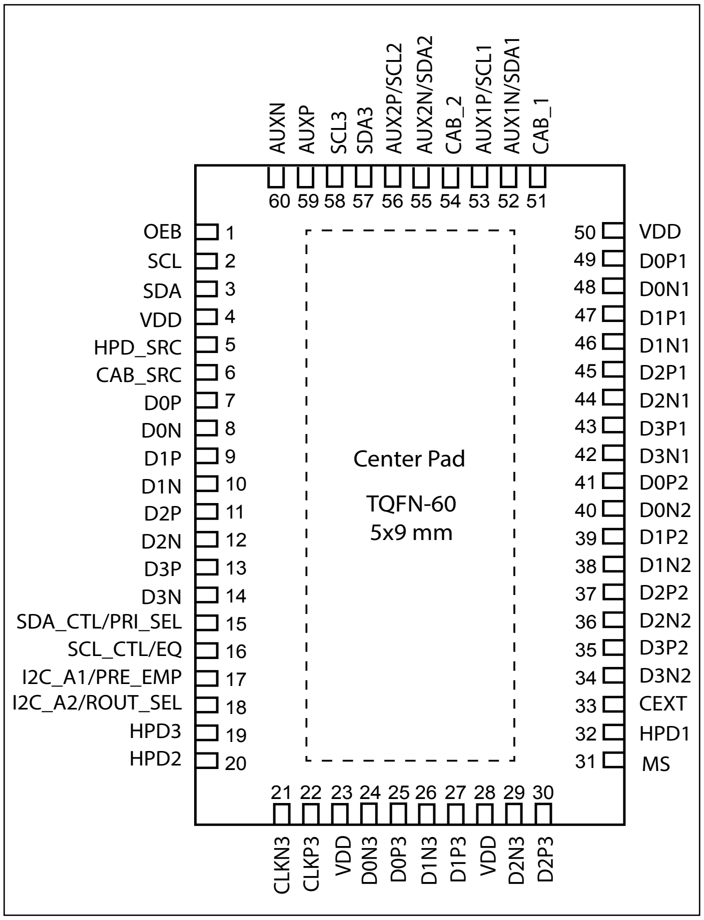
Description

PI3WVR31313A has two passive output port1 and port2, one active (DP to HDMI) output port3. Passive output ports support DP1.2 at 5.4Gbps. Active port3 support HDMI1.4b at 3.4Gbps. All three output ports support auto port priority selection. Input port accepts DP1.2 and DP++ signals associated with output ports as described above.

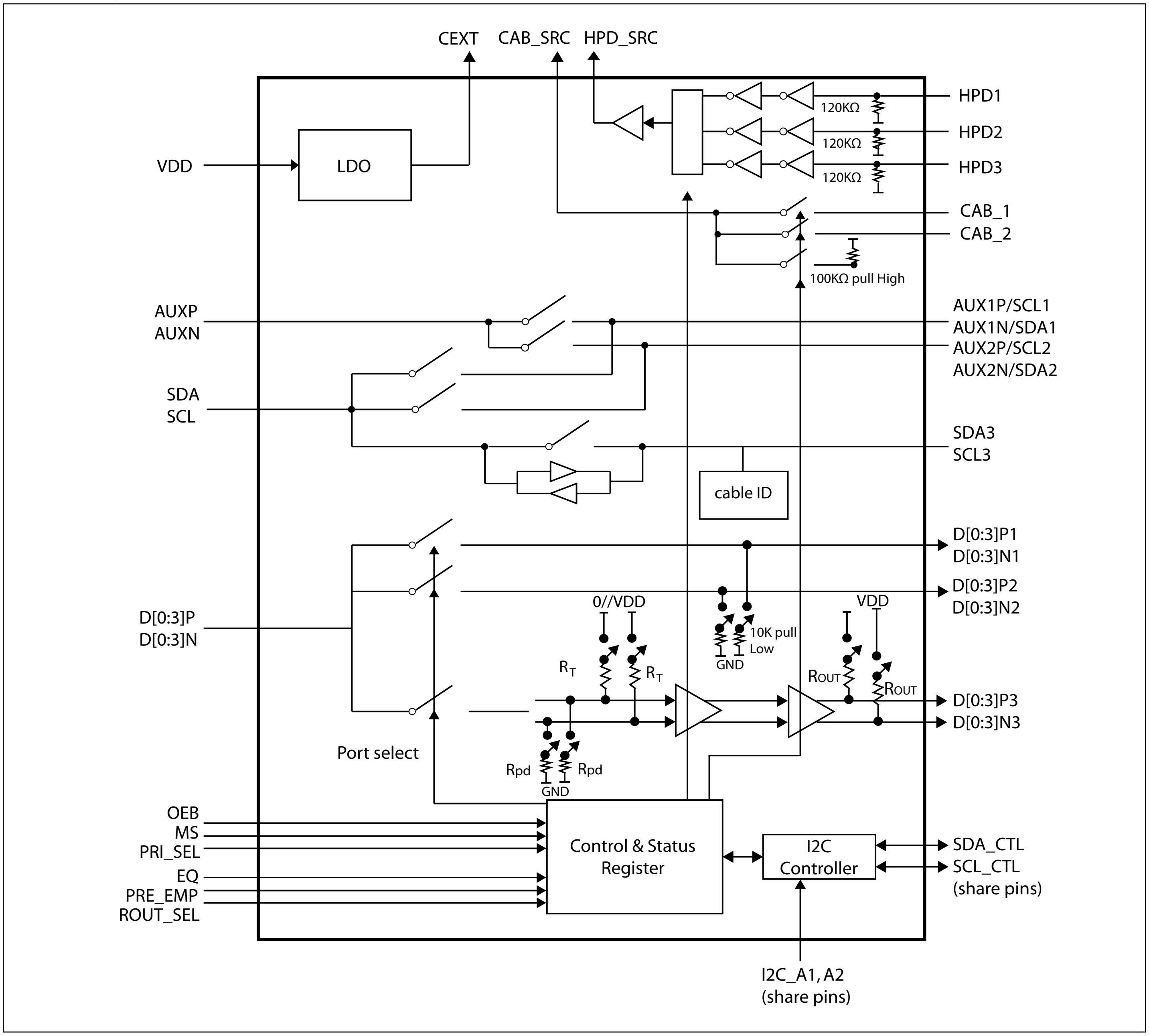
Application

- Notebook

Pin Configuration: TQFN-60



Block Diagram



Pin Description

pin#	pin Name	Signal Type	Description
7 9 11 13 8 10 12 14	D0P D1P D2P D3P D0N D1N D2N D3N	I	4 differential pair input (DP or DP++)
49 47 45 43 48 46 44 42 41 39 37 35 40 38 36 34	D0P1 D1P1 D2P1 D3P1 D0N1 D1N1 D2N1 D3N1 D0P2 D1P2 D2P2 D3P2 D0N2 D1N2 D2N2 D3N2	O	4 differential pair output (DP) for port 1 and port 2
30 27 25 29 26 24 22 21	D2P3 D1P3 D0P3 D2N3 D1N3 D0N3 CLKP3 CLKN3	O	4 differential pair output (HDMI) for port 3

pin#	pin Name	Signal Type	Description
52 55 53 56 57 58	AUX1N/SDA1 AUX2N/SDA2 AUX1P/SCL1 AUX2P/SCL2 SDA3 SCL3	IO	AUX (DP) or DDC (HDMI) to three ports
60 59	AUXN AUXP	IO	AUX to DP-source
3 2	SDA SCL	IO	DDC to DP-source
32 20 19 5	HPD1 HPD2 HPD3 HPD_SRC	I I I O	HPD1-3 for port1-3; HPD_SRC to DP-source
51 54 6	CAB_1 CAB_2 CAB_SRC	IO	CAB_1: CAB_DET to port1 CAD_2: CAB_DET to port2 CAB_SRC: CAB_DET to DP-source No CAB_DET for HDMI port3
1	OEB	I	OEB=0, device active; OEB=1, device shut down
15	SDA_CTL/PRI_SE	I	MS=0, PRI_SEL selects priority in pin control mode; MS=1, SDA_CTL as SDA in I2C control mode
16	SCL_CTL/EQ	IO	MS=0, EQ selects equalization in pin control mode; MS=1, SCL_CTL as SCL in I2C control mode
17	I2C_A1/PRE_EMP	I	MS=0, PRE_EMP selects Pre-emphasis in pin control mode; MS=1, I2C_A1 as I2C address A1 in I2C control mode
18	I2C_A2/ROUT_SEL	I	MS=0, ROUT_SEL selects source termination in pin control mode; MS=1, I2C_A2 as I2C address A2 in I2C control mode
31	MS	I	Mode Select: MS pin with weak pull low resistor > 500Kohm MS=0 or half VDD input level for pin control mode, MS=1 for I2C control mode
33	CEXT	O	Internal LDO bypass capacitance, 4.7uf to GND
4, 23, 28, 50	VDD	Power	3.3V VDD
Center Pad	GND	Ground	Bottom GND EPAD

Pin mapping for dual mode DP source DEMUX to DP output

DP mode	HDMI/DVI mode	WVR31313A input pins	WVR31313A port1 output	WVR31313A port2 output	WVR31313A port3 output
ML_lane0(P)	TX2+	D0P	D0P1	D0P2	D2P3
ML_lane0(N)	TX2-	D0N	D0N1	D0N2	D2N3
ML_lane1(P)	TX1+	D1P	D1P1	D1P2	D1P3
ML_lane1(N)	TX1-	D1N	D1N1	D1N2	D1N3
ML_lane2(P)	TX0+	D2P	D2P1	D2P2	D0P3
ML_lane2(N)	TX0-	D2N	D2N1	D2N2	D0N3
ML_lane3(P)	TXC+	D3P	D3P1	D3P2	CLKP3
ML_lane3(N)	TXC-	D3N	D3N1	D3N2	CLKN3

Function Description

The MS pin selects I2C or pin control mode.

Pin control mode has only automatic port selection. I2C control mode has automatic port selection.

In auto port selection, when only one HPD high detected, the port with HPD high will be selected. When multiple HPD high detected, the PRI_SEL pin(priority select) will determine the priority of the 3 ports.

When PRI_SEL=low, the port-priority will be port1-port2-port3 from high to low; when PRI_SEL=high, the port priority will be port1-port3-port2 from high to low; when PRI_SEL=M (open as not connected), the port priority will be port3-port1-port2 from high to low.

When port 1 (or port2) is selected and CAB_1 (or CAB_2) is low as in DP mode, the AUX/DDC channels will work as AUX channels. AUXP shall have 100Kohm external resistor to GND and AUXN shall have 100Kohm external resistor to VDD. The data rate of AUX channels will be >720Mbps.The internal DDC switch will be off.

When port 1 (or port2) is selected and CAB_1 (or CAB_2) is high when DP to HDMI adapter plugged, the AUX/DDC channels will work as DDC channels. The internal DDC channels are on and the AUX channels are off. The input of DDC channels can tolerate 5V input and voltage of DDC to source will be limited about 3.3V or below.

When port 1 or port 2 is selected (passive ports), port3 with HDMI re-driver will shut down.

When port 3 is selected, the internal DP to HDMI level shifter will be enabled. There will be 3 EQ and 3 Pre-emphasis settings in pin control mode, 8 EQ and 5 Pre-emphasis settings in I2C control mode.

When port 3 is selected, HDMI output can be standard TMDS-open-drain source, as well to be selected with internal source termination as 50 ohm pull up to 3.3V VDD, using ROUT_SEL pin control or I2C control.

When port 3 is active as DP to HDMP level shifter, the DDC channel can be selected between bi-direction DDC buffer and passive DDC switch.

HPD1, HPD2 and HPD3 are with internal CMOS buffers and can support 3.3V and 5V HPD inputs.

Squelch Mode

Squelch function will disable HDMI data output (as high impedance)when the voltage and frequency of input clock (TMDS) are below squelch threshold, which will prevent random noise presenting in HDMI data output, thereby prevent noise on sink display. Squelch function will enable-resume HDMI data output when input clock signals are above squelch threshold.

Truth Table for TMDS port3

EQ – three level pin control
PRE-EMP – three level pin control

EQ	Equalization value
0	1.5dB
open	4.0dB
1	6.5dB

PRE_EMP	TX pre-emphasis
0	0dB
open	1.5dB
1	2.5dB

ROUT_SEL

ROUT_SEL	Pull-Up Resistors on port3 D[0:3]P3, D[0:3]N3
0	No Pull-up resistors
1	50Ω Pull-up resistors to VDD

MS – three level pin control

MS	Pin mode/type cable ID
0	Pin mode for Type 2 ID
M(0.5*vdd)	Pin mode for Type 1 ID
1	I2C mode

Priority Selection Table

PRI_SEL (Priority order)	HPD1	HPD2	HPD3	HPD_SRC	CAB_SRC	AUXP/AUXN	SDA/SCL
0	0	0	0	0	Hi-Z	Hi-Z	Hi-Z
0	1	x	x	HPD1	CAB1=0	AUX1P/AUX1N	Hi-Z
					CAB1=1	Hi-Z	SDA1/SCL1
0	0	1	x	HPD2	CAB2=0	AUX2P/AUX2N	Hi-Z
					CAB2=1	Hi-Z	SDA2/SCL2
0	0	0	1	HPD3	High	Hi-Z	SDA3/SCL3
M	0	0	0	0	Hi-Z	Hi-Z	Hi-Z
M	1	x	0	HPD1	CAB1=0	AUX1P/AUX1N	Hi-Z
					CAB1=1	Hi-Z	SDA1/SCL1
M	0	1	0	HPD2	CAB2=0	AUX2P/AUX2N	Hi-Z
					CAB2=1	Hi-Z	SDA2/SCL2
M	x	x	1	HPD3	High	Hi-Z	SDA3/SCL3
1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z
1	1	x	x	HPD1	CAB1=0	AUX1P/AUX1N	Hi-Z
					CAB1=1	Hi-Z	SDA1/SCL1
1	0	1	0	HPD2	CAB2=0	AUX2P/AUX2N	Hi-Z
					CAB2=1	Hi-Z	SDA2/SCL2
1	0	x	1	HPD3	High	Hi-Z	SDA3/SCL3

Note: M=internal half VDD when input=HiZ

PRI_SEL (Priority order)	HPD1	HPD2	HPD3	D0P	D1P	D2P	D3P	D0N	D1N	D2N	D3N
0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	x	x	D0P1	D1P1	D2P1	D3P1	D0N1	D1N1	D2N1	D3N1
0	0	1	x	D0P2	D1P2	D2P2	D3P2	D0N2	D1N2	D2N2	D3N2
0	0	0	1	D2P3	D1P3	D0P3	CLKP3	D2N3	D1N3	D0N3	CLKN3
M	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M	1	x	0	D0P1	D1P1	D2P1	D3P1	D0N1	D1N1	D2N1	D3N1
M	0	1	0	D0P2	D1P2	D2P2	D3P2	D0N2	D1N2	D2N2	D3N2
M	x	x	1	D2P3	D1P3	D0P3	CLKP3	D2N3	D1N3	D0N3	CLKN3
1	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	1	x	x	D0P1	D1P1	D2P1	D3P1	D0N1	D1N1	D2N1	D3N1
1	0	1	0	D0P2	D1P2	D2P2	D3P2	D0N2	D1N2	D2N2	D3N2
1	0	x	1	D2P3	D1P3	D0P3	CLKP3	D2N3	D1N3	D0N3	CLKN3

Note: M=internal half VDD when input=HiZ

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +4.6V
High Speed Channel Input Voltage (DP Mode)	−0.5V to 2V
DDC and HPD channels Input Voltage	−0.5V to 6V
DC Output Current	180mA
Power Dissipation	0.6W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operation Conditions

V_{DD} = 3.3V ±10%, Min and Max apply for T_A between -40°C to 85°C Typical values are referenced to T_A = 25°C

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
I_{DD}	VDD supply current (Port1 or 2 active)	VDD=3.3V		1	1.8	mA
	VDD Supply Current (Port3 active)	Output Enable (open drain 500mv signal-end 0dB pre-emphasis, not including 40mA current to source)		80	100	mA
		Output Enable (double termination, 500mv signal-end 0dB pre-emphasis, not including 40mA current to source)		160	200	mA
I_{DDQ}	VDD Quiescent Supply Current (port3 active w/o TMDS input)	TMDS Output Disable		3.5	5	mA
Istb	Standby mode by I2C	VDD=3.6V, OEB = Low, Port1/2/3 selection, HPD_1,2,3=0, MS=1		0.6	1.2	mA
Isd1	Supply shut down current when OEB disable (MS=0)	V_{DD}=3.6V, OEB=high		0.1	0.2	uA
Isd2	Supply shut down current when OEB disable (MS=1)	V_{DD}=3.6V, OEB=high		0.6	1.2	mA

DC Electrical Characteristics for Switching over Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
OEB, MS, ROUT_SEL						
I_{IH}	High level digital input current	V_{IH} =VDD	-10		40	μA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	μA
V_{IH}	High level digital input voltage		2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
HPD_SRC						
$V_{OL\_HPD\_SRC}$	Buffer Output Low Voltage	I_{OL} = 4 mA			0.4	V
$V_{OH\_HPD\_SRC}$	Buffer Output Low Voltage	I_{OH} = 4 mA	2.4			V
HPD_sink						
I_{IH}	High level digital input current	V_{IH} =VDD	-10		40	μA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	μA
V_{IH}	High level digital input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
CAB						
I_{LK}	Input leakage current	Switch is off, Vin=5.5V	-50		50	uA
C_{IO}	Input/Output capacitance when-passive switch on			10		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
V_{pass}	Switch Output voltage	V_I=3.3V, I_I=100uA	1.5	3.0	3.3	V
CI(source)	Source side CAB capacitance	V_I peak-peak = 1V, 100 KHz		3.5		pF
CI(sink)	Sink side CAB capacitance when			6.5		pF
SDA/SCL, SDA1/SCL1, SDA2/SCL2						
I_{LK}	Input leakage current	DDC switch is off, Vin=5.5V	-50		50	uA
C_{IO}	Input/Output capacitance when passive switch on	V_I peak-peak = 1V, 100 KHz		8		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
Vpass	Switch Output voltage	V_I=5.0V, I_I=100uA V_{DD}=3.3V	1.5	3.0	3.6	V
CI(source)	Source side DDC capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		2.5		pF
CI(sink)	Sink side DDC capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		5		pF
SDA3/SCL3 (DDC buffer of port3 active)						
V_{IH}	High level input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level input voltage		0		0.8	V
I_{LK}	Input leakage current	DDC switch is off, Vin = 5.5V	-10		10	uA

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low level input current	V_{IL} = 0.2V	-10		10	µA
V_{OL}	Low level output voltage	I_{OL} = 4mA			0.2	V
I_{LOH}	HIGH-level output leakage current	V_O=3.6V			10	µA
C_{IO}	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V or 0V		4		pF
SDA/SCL (DDC buffer of port3 active)						
V_{IH}	High level input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level input voltage		0		0.4	V
I_{LK}	Input leakage current	DDC switch is off, Vin = 5.5V	-10		10	uA
I_{IL}	Low level input current	V_{IL} = 0.2V	-10		10	µA
V_{OL}	Low level output voltage	I_{OL} = 4mA	0.47	0.52	0.6	V
I_{LOH}	HIGH-level output leakage current	V_O=3.6V	5		10	µA
C_{IO}	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V or 0V		8		pF
AUXP, AUXN, AUXnP/SCLn, AUXnN/SDAn						
I_{LK}	Input leakage current	DDC switch is off, Vin=5.5V	-50		50	uA
C_{IO}	Input/Output capacitance when passive switch on	V_I peak-peak = 1V, 100 KHz		6		pF
R_{ON}	Passive Switch resistance	I_O = 3mA, V_O = 0.3V		5		Ω
		I_O = 3mA, V_O = 3.0V		10		Ω
V_{pass}	Switch Output voltage	V_I=5.5V, I_I=100uA V_{DD}=3.3V		3.8	4	V
CI(source)	Source side capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		2.5		pF
CI(sink)	Sink side capacitance (passive switch off.)	V_I peak-peak = 1V, 100 KHz		3.5		pF
High Speed Channel (D[0:3]P/N – D[0:3]P1N1, D[0:3]P/N – D[0:3]P2N2)						
V_{IK}	Clamp Diode Voltage (HS Channel)	V_{DD} = Max., I_{IN} = –18mA		–1.6	–1.8	V
I_{IH}	Input HIGH Current	V_{DD} = Max., V_{IN} = V_{DD}			±10	µA
I_{IL}	Input LOW Current	V_{DD} = Max., V_{IN} = GND			±10	
R_{ON_HS}	On resistance between input to out- put for high speed signals	V_{INPUT},cm = 0V to 1.2V, V_{INPUT},diff < 1.0Vp-p, diff, V_{DD} = 3.0V, I_{INPUT} = 20mA		8		Ohm
		V_{INPUT},cm = 2.2V to 3.1V, V_{INPUT},diff < 1.2Vp-p, diff, V_{DD} = 3.0V, I_{INPUT} = 20mA		8		Ohm

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
High Speed Channel Port3 (D[0:2]P3/N3, CLKP3/N3)						
V_I(open)	Single-ended input voltage under high impedance input or open input	I_L=10uA	VDD-10		VDD+10	mV
R_T	Input termination resistance	V_{IN}=2.9V	45	50	66	ohm
I_{OZ}	Leakage current resistance	V_{DD}=3.6V, OEB=High		30	100	uA
Ioff	Power off leakage current	V_{DD}=0, V_{IN}=3.6V	-100		100	uA

Dynamic Electrical Characteristics over Operating Range

(T_A = -40° to +105°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
TMDS Differential Pins						
t_{pd}	Propagation delay	V_{DD} = 3.3V, Rout = 50Ω off, open drain, 0dB pre-emphasis			2000	ps
t_r	Differential output signal rise time (20% - 80%)			120		
t_f	Differential output signal fall time (20% - 80%)			120		
t_{sk}(p)	Pulse skew			15	50	
t_{sk}(D)	Intra-pair differential skew			25	50	
t_{sk}(o)	Inter-pair differential skew(2)				100	
T_{jit_clk}(pp)	Peak-to-peak output jitter CLK residual jitter	Data Input = 3.4 Gbps HDMI data pattern from signal generation, short trace. CLK Input = 340 MHz clock		15	40	
T_{jit_dat}(pp)	Peak-to-peak output jitter DATA Residual Jitter			25	50	
t_{en}	Enable time	when channel is active			10	us
t_{dis}	Disable time				50	
SCL, SDA channel, AUX channel , CAB channel : passive switches						
t_{pd}(DDC)	Propagation delay from SCLn/SDAn to SCL/SDA or SCL/SDA to SCLn/SDAn In passive SW on.	C_L = 10pF, in passive switch			5	ns
SCL3, SDA3- SCL,SDA channel : buffers						
t_{PLH}	LOW-to-HIGH propagation delay	SCL/SDA to SCL3/SDA3	50	100	150	ns
t_{PHL}	HIGH-to-LOW propagation delay	SCL/SDA to SCL3/SDA3	10	20	40	ns
t_{PLH}	LOW-to-HIGH propagation delay	SCL3/SDA3 to SCL/SDA	50	100	150	ns
t_{PHL}	HIGH-to-LOW propagation delay	SCL3/SDA3 to SCL/SDA	10	20	40	ns

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
Control and Status Pins (HPDn, HPD_SRC)						
tpd(HPD)	Propagation delay (from HPDx to the active port of HPD_SRC, high to low)	CL = 10pF		2	4	us
tsx(HPD)	Switch time (from port select to the latest HPD , manual selection mode)			2	4	us

Dynamic Electrical Characteristics

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
High Speed Channel (D[0:3]P/N – D[0:3]Px/Nx)							
X_{TALK}	Crosstalk on High Speed Channels	See Fig. 1 for Measurement Setup	f= 2.7 GHz		-32	-30	dB
O_{IRR}	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup	f= 2.7 GHz		-19	-17	
I_{LOSS}	Differential Insertion Loss on High Speed Channels	@2.7GHZ (see figure 3)		-1.7	-1.5		dB
R_{loss}	Differential Return Loss on High Speed Channels	@ 2.7GHz (5.4Gbps)			-18	-16	dB
BW_Dx±	Bandwidth -3dB for Main high speed path (Dx±)	See figure 3		5.1	5.6		GHz
BW_AUX	Bandwidth -3dB for AUX	See figure 3		1.2	1.5		GHz
Tstartup	V_{DD} valid to channel enable				250		us
Twakeup	Enabling output by changing OEB from High to Low				250		us
T_{pd}	Propagation delay (input pin to output pin) on all channels				80		ps
t_{b-b}	Bit-to-bit skew within the same differential pair of Dx± channels				5	7	ps
t_{ch-ch}	Channel-to-channel skew of Dx± channels					35	ps

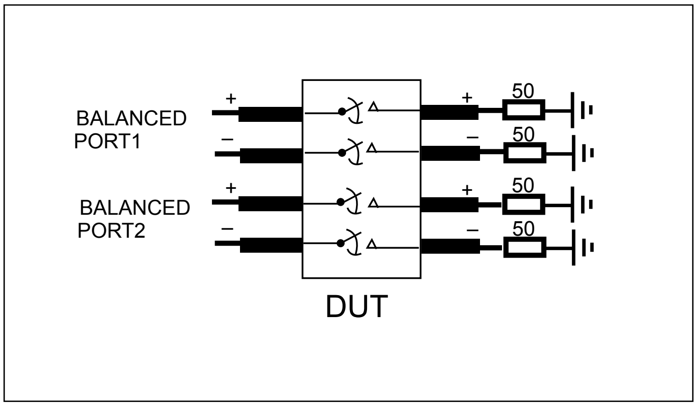


Fig 1. Crosstalk Setup

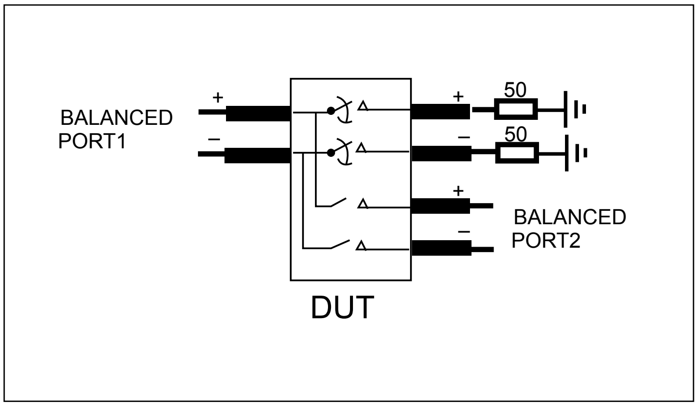


Fig 2. Off-isolation setup

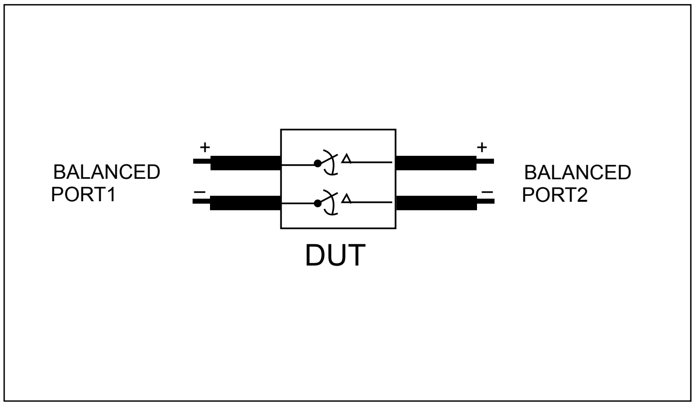
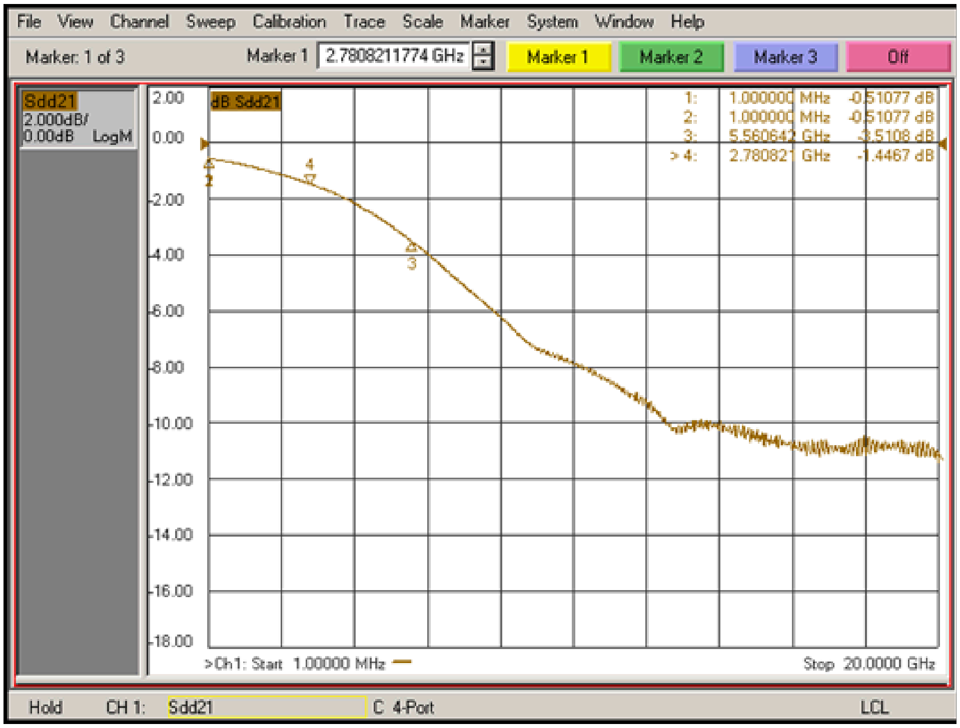


Fig 3. Differential Insertion Loss

Differential Insertion Loss , Vdd=3.3V, 25C



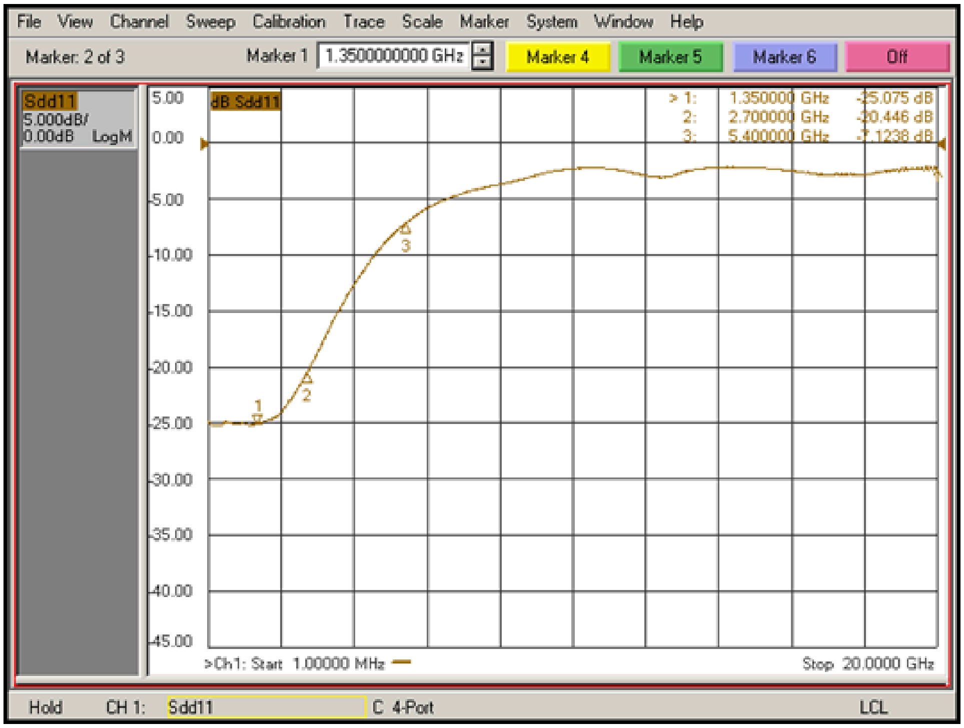
```
  1:  1.000000 MHz  -0.51077 dB
  2:  1.000000 MHz  -0.51077 dB
  3:  5.560642 GHz  -3.5108 dB
> 4:  2.780821 GHz  -1.4467 dB
```

D0 to D01 Channel

```
  1:  1.000000 MHz  -0.48516 dB
  2:  1.000000 MHz  -0.48516 dB
  3:  5.765676 GHz  -3.4852 dB
> 4:  2.883338 GHz  -1.4143 dB
```

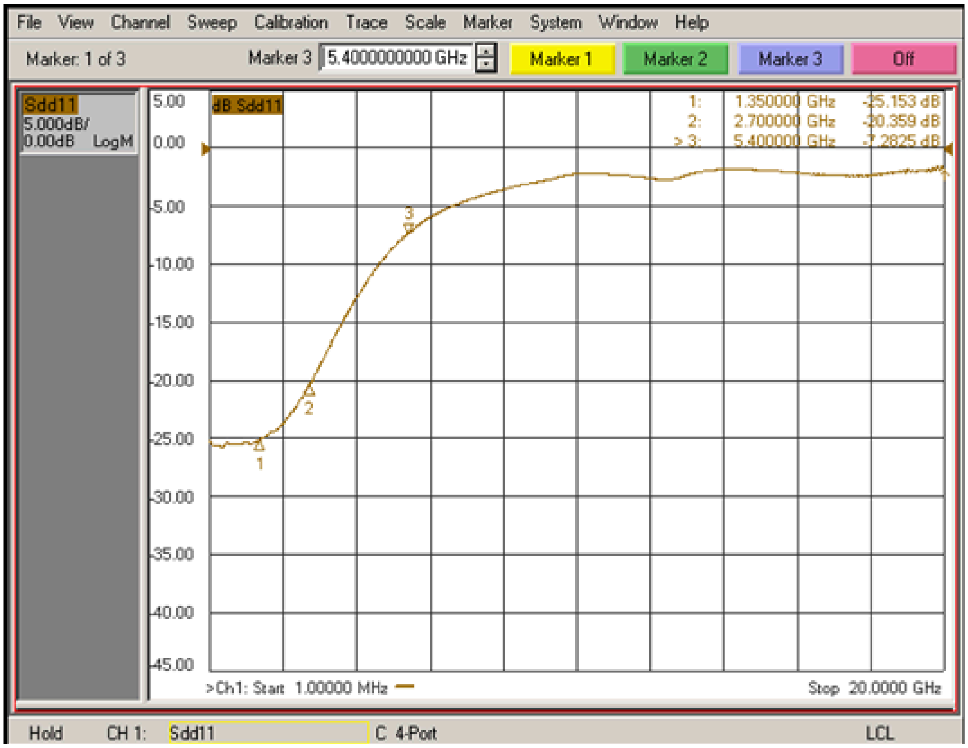
D0 to D02 Channel

Differential Return Loss , Vdd=3.3V, 25C



```
Marker 1 1.3500000000 GHz
> 1: 1.350000 GHz -25.075 dB
  2: 2.700000 GHz -20.446 dB
  3: 5.400000 GHz -7.1238 dB
CH 1: Sdd11
```

D0 to D01 Channel



```
Marker 3 5.4000000000 GHz
  1: 1.350000 GHz -25.153 dB
  2: 2.700000 GHz -20.359 dB
> 3: 5.400000 GHz -7.2825 dB
CH 1: Sdd11
```

D0 to D02 Channel

Differential Off Isolation , Vdd=3.3V, 25C

```
> 1:  1.350000 GHz  -31.216 dB
  2:  2.700000 GHz  -22.534 dB
  3:  5.400000 GHz  -18.526 dB
```

>Ch1: Start 1.00000 MHz   Stop 20.0000 GHz

Hold CH 1: Sdd21 C 4-Port LCL

HPD auto selection timing waveform

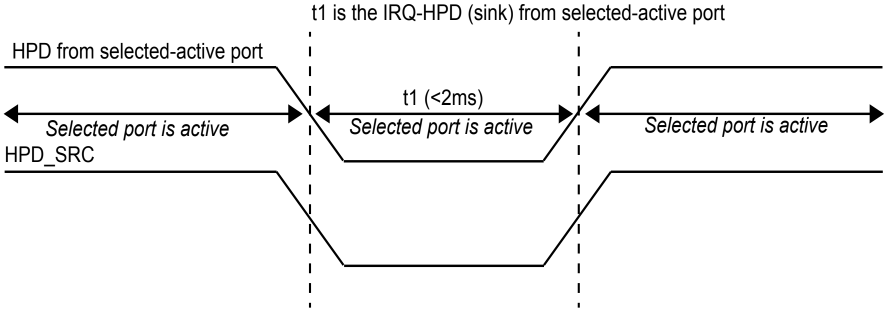


Fig 4. HPD timing t1. HPD_SRC low and the active of selected port will follow t1, if t1 further extended less than t2 (125ms)

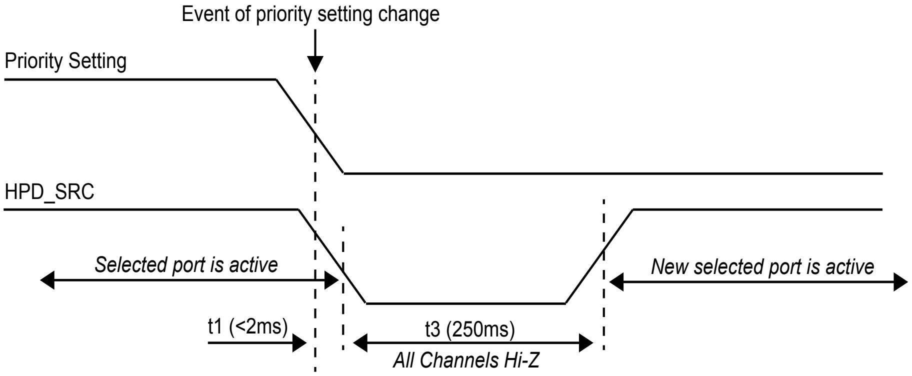


Fig 5. HPD timing t3.   All channels include DP-HDMI data, AUX, DDC, HPD and CAB_DET

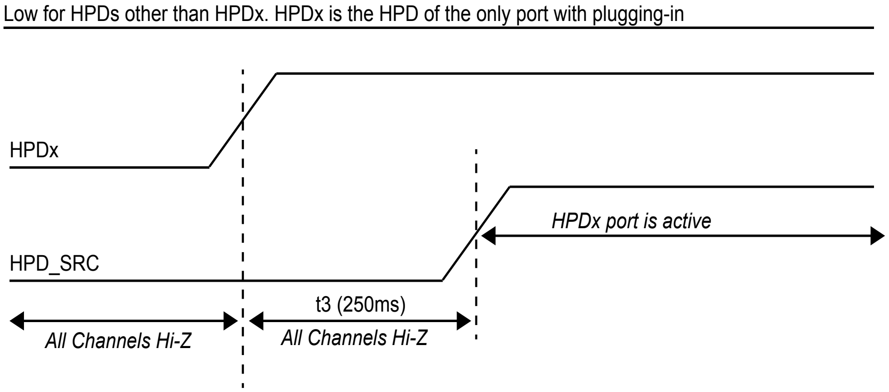


Fig 6. HPD timing t3

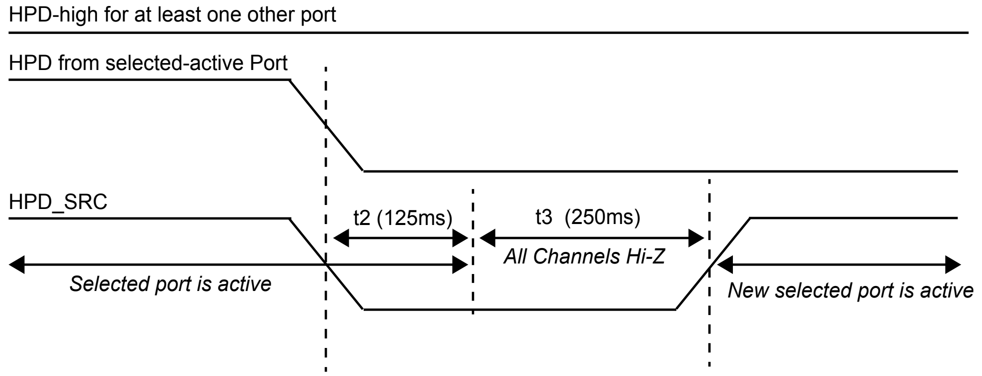


Fig 7. HPD timing.

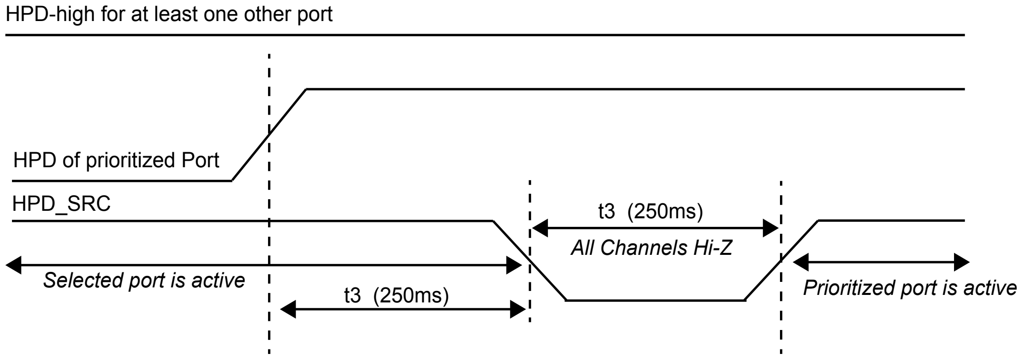


Fig 8. HPD timing

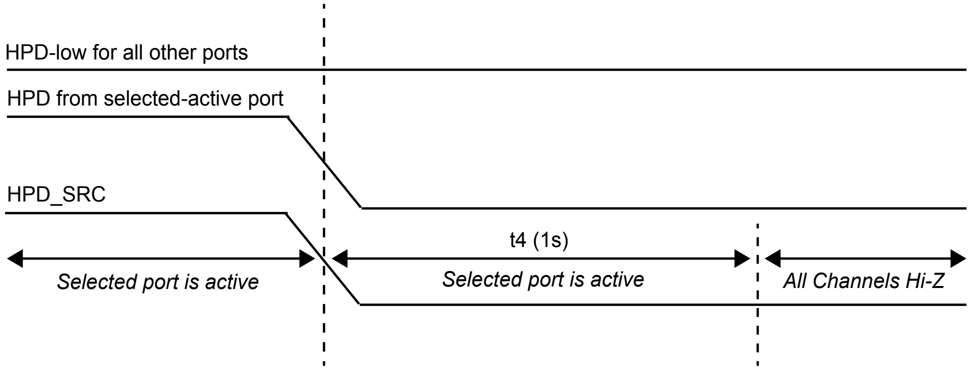


Fig 9. HPD timing t4

Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
HPD auto switching timing					
HPD pulse duration when treated as an IRQ –t1 (Figure 4)				2	ms
Propagation delay of HPDx Desertion –t2 (Figure 7)		50	125	200	ms
HPD_SRC low duration when the outputs are switched –t3(Figure 5,6,7,8); Propagation delay of HPDx assertion (Figure 8)		100	250	400	ms
Power down delay from HPDx de-assertion to chip power down –t4. (Figure 9)		400	1000	1600	ms

*Typical time can be changed by I2C Byte 0x01 bit[2:0], and Byte 0x04 bit3.

I2C Address Byte

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0 (R/W)
Address Byte	1	0	1	1	A2	A1	1	1/0*

* Read; 0:Write, A2 and A1 are two address bits setting

Data transmission format

Data is transmitted to the PI3WVR31313A registers using the Write mode as shown in Figure 1. Data is read from the PI3WVR31313A registers using the Read mode as shown in Figure 2.

Figure 1: I2C control register write condition

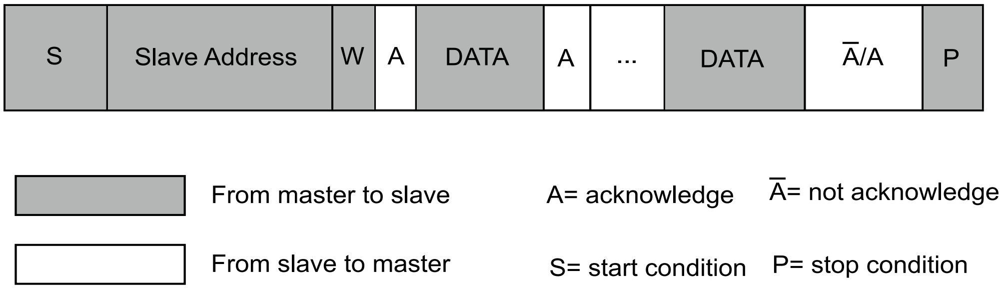


Figure 2: I2c control register read condition

I2C Control Register

The I2C control register uses index read or write for byte access.

Offset	Name	Description	Power Up Condition	Type
0x00	CONFIG[7:0]	[7] Reserved to 0 [6:5] Port SEL1/SEL0 selection control 00 port 1 (Reserved) 01 port 2 (Reserved) 10 port 3 (Reserved) 11 Auto selection mode depending on PRI_SEL below [4:2] PRI_SEL priority selection control by HPDx 000 port1/port2/port3 001 port1/port3/port2 010 port2/port1/port3 011 port2/port3/port1 1x0 port3/port1/port2 1x1 port3/port2/port1 [1] DP_HDMI selection control 0=DP input, 1=Reserved [0] Cable ID type selection 0=Type 2 cable ID 1=Type 1 cable ID	0x01	R/W

0x01	RX_SET[7:5] for port3; HPD auto selection time	[7:5] EQ programmable setting 000: 1.5 dB 001: 4 dB 010: 6.5 dB 011: 9 dB 100: 11.5 dB 101: 14 dB 110: 16.5 dB 111: 9 dB [4:3] HPD auto selection time source control 00: normal 01: -25% 10: +25% 11: test mode [2] HPD auto selection time t3 setting 0: 256ms 1: 128ms [1] HPD auto selection time t4 setting 0: 1024ms 1: 516ms [0] HPD pulse duration treated as IRQ time t1 setting 0: 2ms 1: 4ms	0x00	R/W

0x02	TX_SET[7:0] for port3	Output setting for HDMI re-driver/level shifter [7] HDMI output control 0: open drain 1: double termination [6:4] HDMI output Pre-emphasis settings 000: 0dB 001: 1.5dB 010: 2.5dB 011: 3.5dB 100: 6dB [3:2] TMDS output swing setting 00: 500mv as default 01: -10% 10: +10% 11: +20% [1] TMDS output slow rate setting 0: as default 1: +10% [0] DP1 and DP2 port 10Kohm pull low control 0=10Kohm pull low on 1=10Kohm pull low off	0x00	R/W
0x03	Pericom ID	Pericom Vendor Register ID (refer to PCIE clock buffer) [7:4] Vendor ID 0101 [3:0] device revision 0001	0x51	R

0x04	HPDx/ CABx[6:0] Read only	[7] HPD_SRC output logic function (buffer) 0: HPD_SRC=HPDx 1: HPD_SRC=/HPDx [6] DDC function for port 3 0: Active buffer 1: passive switch [5] Port switching in manual selection 1: disable T3 time pulse when port switching, Port switch immediately 0: Enable T3 time pulse when port switching [4] HPD auto selection time t2 setting 0: 128ms 1: 64ms [3] HPD3 status as read only [2] HPD2 status as read only [1] HPD1 status as read only [0] Reserved for HPD1B	0x00	R/W [7:4] R [3:0]

Table of ID registers

Data address offset	Data as in spec	Read/White as in spec	Description as in spec	WVR31313A
00h	44h	RO	D	D
01h	50h	RO	P	P
02h	2dh	RO	-	-
03h	48h	RO	H	H
04h	44h	RO	D	D
05h	4dh	RO	M	M
06h	49h	RO	I	I
07h	20h	RO	Space	Space
08h	41h	RO	A	A
09h	44h	RO	D	D
0ah	41h	RO	A	A
0bh	50h	RO	P	P
0ch	54h	RO	T	T
0dh	4fh	RO	O	O
0eh	52h	RO	R	R
0fh	04h	RO	.	.
10h	A0h	RO	Cable Adaptor Identifier	A0h
11h	UD	RO	IEEE OUI 1st byte	00h
12h	UD	RO	IEEE OUI 2nd byte	60h
13h	UD	RO	IEEE OUI third byte	23h
14h	UD	RO	Device Id	50h “P”
15h	UD	RO	Device Id	49h “I”
16h	UD	RO	Device Id	33h “3”
17h	UD	RO	Device Id	57h “W”
18h	UD	RO	Device Id	56h “V”
19h	UD	RO	Device Id	52h “R”
1ah	UD	RO	Hardware (chip) revision 7:4h: major revision 3:0h: minor revision.	00h
1bh	UD	RO	Firmware/software major revision	00h
1ch	UD	RO	Firmware/software minor revision	00h
1dh	UD	RO	Clock rate, specified max 300mhz for HDMI	78h: 300MHz (300/2.5=120=78h)
1eh	0fh	RO	I2C speed control capabilities bit map	0fh

1fh	00h	RW	Reserved data Address at 1fh: 1. DP source reads data address 1fh, ID register returns 00h 2. DP source writes data AAh to data address 1fh, ID register responds ACK or returns 00h.	1fh=00, RW, reserved
20h	00h or 01h	R/W	TMDS output enable or disable. 00h: enabled 01h: disabled (<=10mV Voff) [7:1] Reserved	00h, RW (Not Applicable for PI-3WVR31313A) 00h: enabled 01h: disabled (<=10mV Voff) [7:1] Reserved
21h	00h or 01h	R/W	Enables/disables the CEC Isolation Switch. 00h: enabled 01h: disabled [7:1] Reserved	00h, RW (Not Applicable for PI-3WVR31313A) 00h: enabled 01h: disabled [7:1] Reserved
22h	UD	R/W	I2C speed control status bit map. 01h: 1Kbps 02h: 5Kbps 04h: 10Kbps 08h: 100Kbps 10h, 20h, 40h and 80h are reserved	08h for 100Khz. (Not Applicable for PI-3WVR31313A) For the function specified as: 01h: 1Kbps 02h: 5Kbps 04h: 10Kbps 08h: 100Kbps 10h, 20h, 40h and 80h are reserved
23h-ffh	00h	R/W	Reserved data Address from 23h to ffh: 1. DP source reads data address 23h thru ffh, ID register returns 00h. 2. DP source writes data AAh to data address 23h thru ffh, ID register responds ACK or returns 00h.	23h-ffh=00h, RW, reserved.

Notes:

1. DP++ source accesses ID at device address 80h/81h with data offset from 00h-ffh.
2. UD: user dependent.
3. RO: read only.
4. OUI: IEEE Organizationally Unique Identifier.

ID Access Sequence Specified in DP Interoperability V1.1A

It is suggested that the Source-side cable adaptor have a voltage-level shifter to convert the 5-V HPD signal from a DVI/HDMI Sink Device to +2.25V ~ +3.6V voltage as specified the HPD signal input voltage range of DisplayPort Specification Ver.1.1a.

DDC Buffer ID of a Source-side HDMI Cable Adaptor

Offset	0	1	2	3	4	5	6	7	8	9	Ah	Bh	Ch	Dh	Eh	Fh
Data	44h	50h	2Dh	48h	44h	4Dh	49h	20h	41h	44h	41h	50h	54h	4Fh	52h	04h

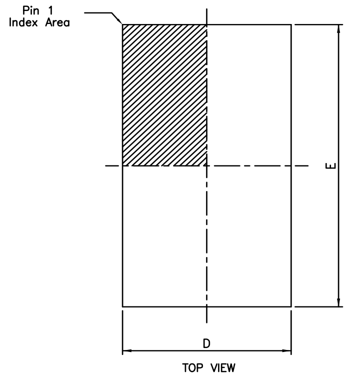
Table below shows the I2C transaction sequence for a Source Device to read the DDC Buffer ID of the Source-side HDMI cable adaptor. I2C write for setting the address offset is optional for a Dual-mode Source Device. The HDMI cable adaptor must acknowledge it when it receives this write operation. The DVI cable adaptor must NACK the I2C transaction to Device Address 80h/81h.

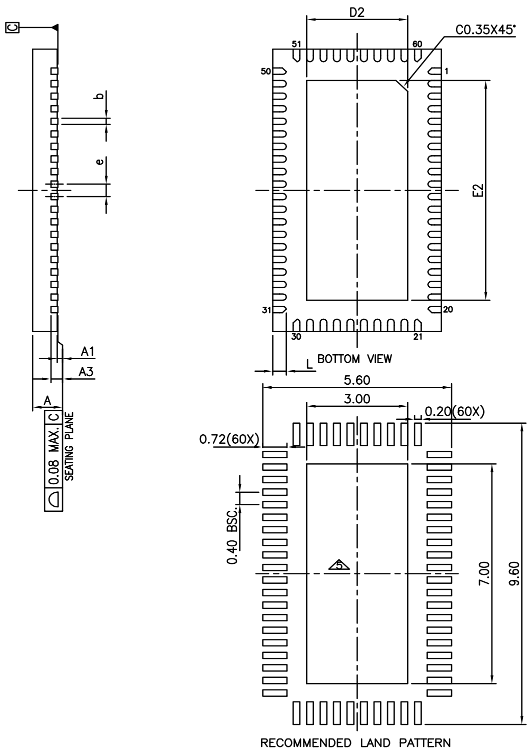
DDC Buffer ID Access Sequence

Phase	I^{2}C Transaction	Transmitting	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	R/W#	Status	
											Master	Slave
1	Start	Master									Optional	-
2	Write command	Master	1	0	0	0	0	0	0	0	Optional	-
3	Acknowledge	Slave									-	Mandatory
4	Word address offset	Master	Word address offset data byte								Optional	-
5	Acknowledge	Slave									-	Mandatory
6	Stop	Master									Optional	-
7	Start	Master									Mandatory	-
8	Read command	Master	1	0	0	0	0	0	0	1	Mandatory	-
9	Acknowledge	Slave									-	Mandatory
10	Read data	Slave	Data byte at Offset 0								-	Mandatory
11	Acknowledge	Master									Mandatory	
12	Read data	Slave	Data byte at Offset 1								-	Mandatory
13											-	...
											-	...
40	Read data	Slave	Data byte at Offset 15								-	Mandatory
41	Not acknowlegde	Master									Mandatory	-
42	Stop	Master									Mandatory	-

Note: if the Slave does not acknowledge during the above transaction sequence, the entire sequence should be retried by the source.

Packaging Mechanical: ZL60





SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	8.90	9.00	9.10
e	0.40 BSC		
L	0.30	0.40	0.50
D2	2.90	3.00	3.10
E2	6.90	7.00	7.10

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM®
Enabling Serial Connectivity

DATE: 04/08/14

DESCRIPTION: 60-Pin, TQFN 5X9mm

PACKAGE CODE: ZL (ZL60)

DOCUMENT CONTROL #: PD-2182 **REVISION: --**

14-0044

Note:

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3WVR31313AZLE	ZL	60-Pin, (TQFN) 5X9mm
PI3WVR31313AZLEX	ZL	60-Pin, (TQFN) 5X9mm, Tape & Reel

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging