

## 2-Bit Bi-directional Level Shifter with Automatic Sensing & Ultra Tiny Package

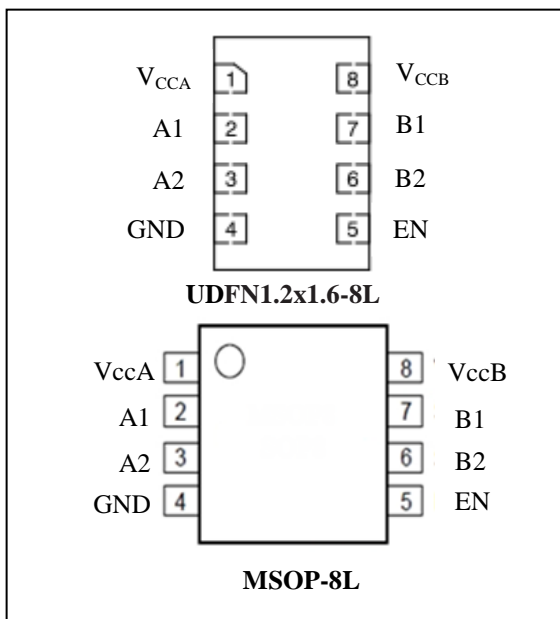
### Features

- $V_{CCA}$  can be Less than, Greater than or Equal to  $V_{CCB}$
- 1.2V to 5.5V on A Port and 1.2V to 5.5V on B Port
- High-Speed with 20 Mb/s Data Rate for push-pull application
- High-Speed with 2 Mb/s Data Rate for open-drain application
- No Direction-Control Signal Needed
- Low Bit-to-Bit Skew
- Non-preferential Power-up Sequencing
- ESD protection exceeds 8KV HBM per JESD22-A114
- Integrated 10 k $\Omega$  Pull-up Resistors
- Package: UDFN1.2x1.6-8L and MSOP-8L

### Applications

- I<sup>2</sup>C, SMBus, MDIO
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Camera

### Pin Configuration



### Description

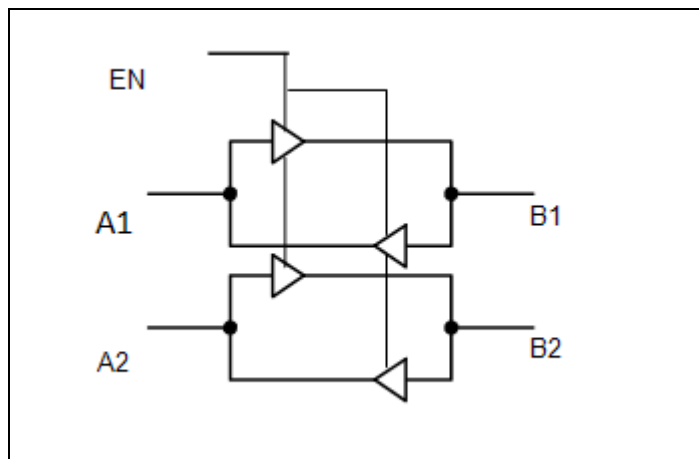
The PI4ULS5V202 is a 2-bit configurable dual supply bidirectional auto sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails,  $V_{CCA}$  and  $V_{CCB}$  respectively. Both the  $V_{CCA}$  and  $V_{CCB}$  supply rails are configurable from 1.2V to 5.5V. This allows voltage logic signals on the  $V_{CCA}$  side to be translated into lower, higher or equal value voltage logic signals on the  $V_{CCB}$  side, and vice-versa.

The translator has integrated 10 k $\Omega$  pull-up resistors on the I/O lines. The integrated pull-up resistors are used to pull-up the I/O lines to either  $V_{CCA}$  or  $V_{CCB}$ . The PI4ULS5V202 is an excellent match for open-drain applications such as the I<sup>2</sup>C communication bus.

### Pin Description

Pin No	Pin Name	Type	Description
1	$V_{CCA}$	Power	A-port supply voltage. $1.2V \leq V_{CCA} \leq 5.5V$
2	A1	I/O	Input/output A. Referenced to $V_{CCA}$ .
3	A2	I/O	Input/output A. Referenced to $V_{CCA}$ .
4	GND	GND	Ground.
5	EN	Input	Output enable (active High). Pull EN low to place all outputs in 3-state mode.
6	B2	I/O	Input/output B. Referenced to $V_{CCB}$ .
7	B1	I/O	Input/output B. Referenced to $V_{CCB}$ .
8	$V_{CCB}$	Power	B-port supply voltage. $1.2V \leq V_{CCB} \leq 5.5V$

## Block Diagram



**Figure 1: Block Diagram**

## Maximum Ratings

Storage Temperature .....	-65°C to +150°C
DC Supply Voltage port B.....	-0.3V to +5.5V
DC Supply Voltage port A .....	-0.3V to +5.5V
V <sub>i</sub> (A) referenced DC Input / Output Voltage.....	-0.3V to +5.5V
V <sub>i</sub> (B) referenced DC Input / Output Voltage.....	-0.3V to +5.5V
Enable Control Pin DC Input Voltage .....	-0.3V to +5.5V
Short circuit duration (I/O to GND) .....	40mA

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended operation conditions

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CCA</sub>	V <sub>CCA</sub> Positive DC Supply Voltage	1.2	-	5.5	V
V <sub>CCB</sub>	V <sub>CCB</sub> Positive DC Supply Voltage	1.2	-	5.5	V
V <sub>EN</sub>	Enable Control Pin Voltage	GND	-	5.5	V
V <sub>IO</sub>	I/O Pin Voltage	GND	-	5.5	V
T <sub>A</sub>	Operating Temperature Range	-40	-	+85	°C

### DC Electrical Characteristics

Unless otherwise specified,  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $1.2\text{V} \leq V_{CC} \leq 5.5\text{V}$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IHB}$	B port Input HIGH Voltage	-	$V_{CCB} - 0.2$	-	-	V
$V_{ILB}$	B port Input LOW Voltage	-	-	-	0.15	V
$V_{IHA}$	A port Input HIGH Voltage	-	$V_{CCA} - 0.2$	-	-	V
$V_{ILA}$	A port Input LOW Voltage	-	-	-	0.15	V
$V_{IH}$	Control Pin Input HIGH Voltage	-	$V_{CCA} - 0.2$	-	-	V
$V_{IL}$	Control Pin Input LOW Voltage	-	-	-	0.15	V
$V_{OHB}$	B port Output HIGH Voltage	B port source current = $-20 \mu\text{A}$	$\frac{2}{3} * V_{CCB}$	-	-	V
$V_{OLB}$	B port Output LOW Voltage	B port sink current = $1 \text{ mA}$	-	-	$\frac{1}{3} * V_{CCB}$	V
$V_{OHA}$	A port Output HIGH Voltage	A port source current = $-20 \mu\text{A}$	$\frac{2}{3} * V_{CCA}$	-	-	V
$V_{OLA}$	A port Output LOW Voltage	A port sink current = $1 \text{ mA}$	-	-	$\frac{1}{3} * V_{CCA}$	V
$I_{QVCB}$	$V_{CCB}$ Supply Current	B port and A port unconnected, $V_{EN} = V_{CCA}$	-	0.5	5.0	$\mu\text{A}$
$I_{QVCA}$	$V_{CCA}$ Supply Current	B port and A port unconnected, $V_{EN} = V_{CCA}$	-	0.3	5.0	$\mu\text{A}$
$I_{TS-V_{CCB}}$	B Tri-state Output Mode	B port and A port unconnected, $V_{EN} = \text{GND}$	-	0.1	1	$\mu\text{A}$
$I_{TS-V_{CCA}}$	A Tri-state Output Mode Supply Current	B port and A port unconnected, $V_{EN} = \text{GND}$	-	0.1	1	$\mu\text{A}$
$I_{OZ}$	I/O Tri-state Output Mode Leakage Current		-	0.1	1.0	$\mu\text{A}$
$R_{PU}$	Pull-Up Resistors I/O A and B		-	10	-	$\text{k}\Omega$

**Note:** All units are production tested at  $T_A = +25^{\circ}\text{C}$ . Limits over the operating temperature range are guaranteed by design.

Typical values are for  $V_{CCB} = +2.8 \text{ V}$ ,  $V_{CCA} = +1.8 \text{ V}$  and  $T_A = +25^{\circ}\text{C}$ .

### AC Electrical characteristics

#### Timing Characteristics – Rail-to-Rail Driving Configuration

(I/O test circuits of Figures 2, 3 and 7,  $C_{LOAD} = 15 \text{ pF}$ , driver output impedance  $\leq 50\Omega$ ,  $R_{LOAD} = 1 \text{ M}\Omega$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{CCA} = 1.8\text{V}$ , $V_{CCB} = 2.8\text{V}$						
$t_{RB}$	B port Rise Time	-	-	-	15	nS
$t_{FB}$	B port Fall Time	-	-	-	15	nS
$t_{RA}$	A port Rise Time	-	-	-	25	nS
$t_{FA}$	A port Fall Time	-	-	-	10	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	15	nS
$t_{PLH-A-B}$		-	-	-	15	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	15	nS
$t_{PLH-B-A}$		-	-	-	15	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	5	nS
MDR	Maximum Data Rate	-	20	-	-	Mbps

To be continued.

Continuously.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b><math>V_{CCA} = 2.8V, V_{CCB} = 1.8V</math></b>						
$t_{RB}$	B port Rise Time	-	-	-	25	nS
$t_{FB}$	B port Fall Time	-	-	-	10	nS
$t_{RA}$	A port Rise Time	-	-	-	20	nS
$t_{FA}$	A port Fall Time	-	-	-	15	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	15	nS
$t_{PLH-A-B}$		-	-	-	15	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	15	nS
$t_{PLH-B-A}$		-	-	-	15	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	5	nS
MDR	Maximum Data Rate	-	20	-	-	Mbps
<b><math>V_{CCA} = 2.5V, V_{CCB} = 3.6V</math></b>						
$t_{RB}$	B port Rise Time	-	-	-	15	nS
$t_{FB}$	B port Fall Time	-	-	-	10	nS
$t_{RA}$	A port Rise Time	-	-	-	15	nS
$t_{FA}$	A port Fall Time	-	-	-	10	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	15	nS
$t_{PLH-A-B}$		-	-	-	15	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	15	nS
$t_{PLH-B-A}$		-	-	-	15	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	5	nS
MDR	Maximum Data Rate	-	20	-	-	Mbps
<b><math>V_{CCA} = 3.6V, V_{CCB} = 2.5V</math></b>						
$t_{RB}$	B port Rise Time	-	-	-	15	nS
$t_{FB}$	B port Fall Time	-	-	-	10	nS
$t_{RA}$	A port Rise Time	-	-	-	15	nS
$t_{FA}$	A port Fall Time	-	-	-	15	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	15	nS
$t_{PLH-A-B}$		-	-	-	15	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	15	nS
$t_{PLH-B-A}$		-	-	-	15	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	5	nS
MDR	Maximum Data Rate	-	20	-	-	Mbps

To be continued.

Continuously.

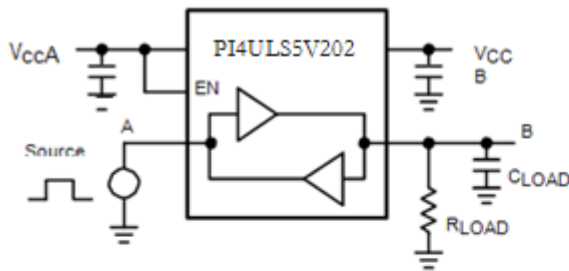
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b><math>V_{CCA} = 1.5V, V_{CCB} = 5.5V</math></b>						
$t_{RB}$	B port Rise Time	-	-	-	15	nS
$t_{FB}$	B port Fall Time	-	-	-	20	nS
$t_{RA}$	A port Rise Time	-	-	-	30	nS
$t_{FA}$	A port Fall Time	-	-	-	10	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	20	nS
$t_{PLH-A-B}$		-	-	-	20	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	20	nS
$t_{PLH-B-A}$		-	-	-	20	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	5	nS
MDR	Maximum Data Rate	-	20	-	-	Mbps
<b><math>V_{CCA} = 5.5, V_{CCB} = 1.5V</math></b>						
$t_{RB}$	B port Rise Time	-	-	-	30	nS
$t_{FB}$	B port Fall Time	-	-	-	20	nS
$t_{RA}$	A port Rise Time	-	-	-	15	nS
$t_{FA}$	A port Fall Time	-	-	-	40	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	20	nS
$t_{PLH-A-B}$		-	-	-	20	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	20	nS
$t_{PLH-B-A}$		-	-	-	20	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	5	nS
MDR	Maximum Data Rate	-	20	-	-	Mbps
<b><math>V_{CCA} = 1.2V, V_{CCB} = 5.5V</math></b>						
$t_{RB}$	B port Rise Time	-	-	-	15	nS
$t_{FB}$	B port Fall Time	-	-	-	30	nS
$t_{RA}$	A port Rise Time	-	-	-	30	nS
$t_{FA}$	A port Fall Time	-	-	-	15	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	20	nS
$t_{PLH-A-B}$		-	-	-	15	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	15	nS
$t_{PLH-B-A}$		-	-	-	15	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	5	nS
MDR	Maximum Data Rate	-	20	-	-	Mbps
<b><math>V_{CCA} = 5.5V, V_{CCB} = 1.2V</math></b>						
$t_{RB}$	B port Rise Time	-	-	-	30	nS
$t_{FB}$	B port Fall Time	-	-	-	15	nS
$t_{RA}$	A port Rise Time	-	-	-	15	nS
$t_{FA}$	A port Fall Time	-	-	-	30	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	15	nS
$t_{PLH-A-B}$		-	-	-	15	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	20	nS
$t_{PLH-B-A}$		-	-	-	15	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	5	nS
MDR	Maximum Data Rate	-	20	-	-	Mbps

**Timing Characteristics – Open Drain Driving Configuration**

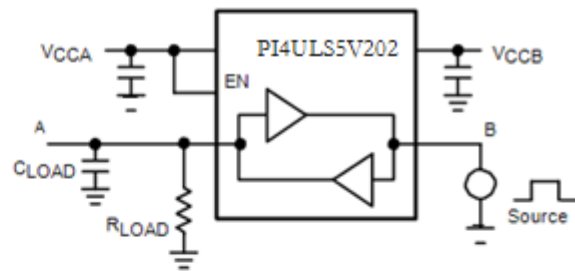
(I/O test circuits of Figures 4, 5 and 7,  $C_{LOAD} = 15\text{ pF}$ , driver output impedance  $\leq 50\Omega$ ,  $R_{LOAD} = 1\text{ M}\Omega$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b><math>1.2 \leq V_{CCA} \leq V_{CCB} \leq 5.5\text{V}</math></b>						
$t_{RB}$	B port Rise Time	-	-	-	450	nS
$t_{FB}$	B port Fall Time	-	-	-	30	nS
$t_{RA}$	A port Rise Time	-	-	-	450	nS
$t_{FA}$	A port Fall Time	-	-	-	30	nS
$t_{PHL-A-B}$	Propagation Delay (Driving A)	-	-	-	300	nS
$t_{PLH-A-B}$		-	-	-	300	nS
$t_{PHL-B-A}$	Propagation Delay (Driving B)	-	-	-	300	nS
$t_{PLH-B-A}$		-	-	-	300	nS
$t_{PPSKEW}$	Part-to-Part Skew	-	-	-	50	nS
MDR	Maximum Data Rate	-	2	-	-	Mbps

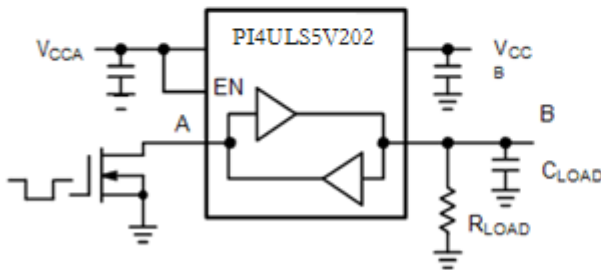
**Test Circuits**



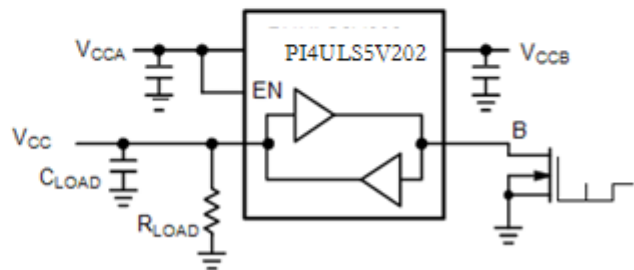
**Figure 2. Rail-to-Rail Driving A**



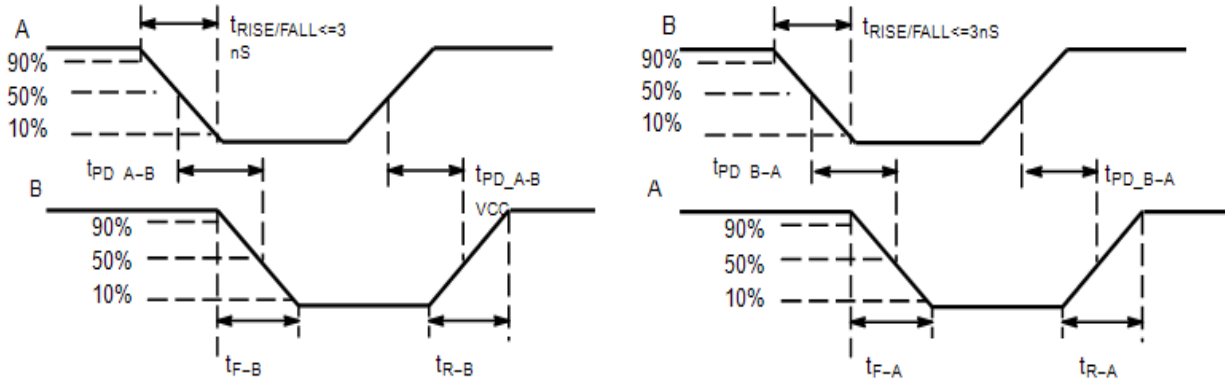
**Figure 3. Rail-to-Rail Driving B**



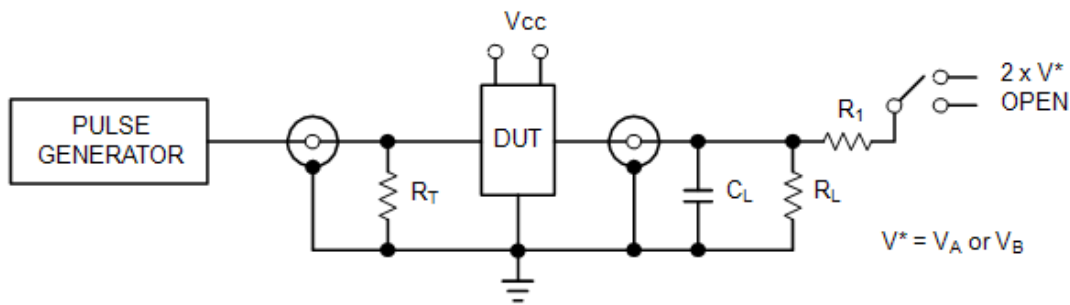
**Figure 4. Open-Drain Driving A**



**Figure 5. Open-Drain Driving B**



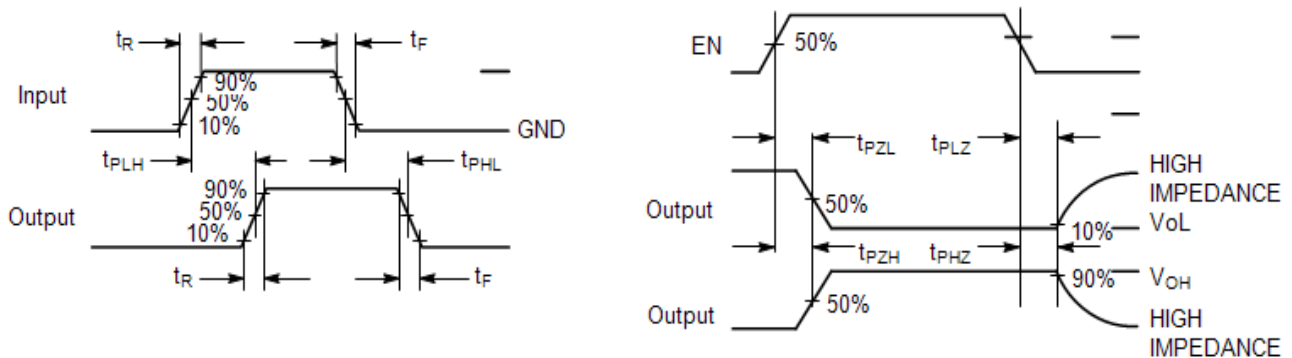
**Figure 6. Definition of Timing Specification Parameters**



Test	Switch
$t_{PZH}, t_{PHZ}$	Open
$t_{PZL}, t_{PLZ}$	$2 \times V^*$

$C_L = 15 \text{ pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 50 \text{ k}\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )  
 $V^* = V_A \text{ or } V_B$  for A or B measurements, respectively.

**Figure 7. Test Circuit for Enable/Disable Time Measurement**



**Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement**

## Functional Description

The PI4ULS5V202 is a 2-bit configurable dual supply bidirectional auto sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails,  $V_{CCA}$  and  $V_{CCB}$  respectively. Both the  $V_{CCA}$  and  $V_{CCB}$  supply rails are configurable from 1.2 V to 5.5 V. This allows voltage logic signals on the  $V_{CCA}$  side to be translated into lower, higher or equal value voltage logic signals on the  $V_{CCB}$  side, and vice-versa.

The translator has integrated 10 k $\Omega$  pull-up resistors on the I/O lines. The integrated pull-up resistors are used to pull-up the I/O lines to either  $V_{CCA}$  or  $V_{CCB}$ . The PI4ULS5V202 is an excellent match for open-drain applications such as the I<sup>2</sup>C communication bus.

## Application Information

### Level Translator Architecture

The PI4ULS5V202 auto sense translator provides bidirectional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages,  $V_{CCA}$  and  $V_{CCB}$ , which set the logic levels on the input and output sides of the translator. When used to transfer data from A port to B port, input signals referenced to the  $V_{CCA}$  supply are translated to output signals with a logic level matched to  $V_{CCB}$ . In a similar manner, translation shifts input signals with a logic level compatible to  $V_{CCB}$  to an output signal matched to  $V_{CCA}$ . The PI4ULS5V202 consists of two bidirectional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high-to-low and low-to-high transitions. Each input/output channel has an internal 10 k $\Omega$  pull. The magnitude of the pull-up resistors can be reduced by connecting external resistors in parallel to the internal 10 k $\Omega$  resistors.

### Input Driver Requirements

The rise ( $t_R$ ) and fall ( $t_F$ ) timing parameters of the open drain outputs depend on the magnitude of the pull-up resistors. In addition, the propagation times ( $t_{PD}$ ), skew ( $t_{PSKEW}$ ) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 k $\Omega$ .

### Enable Input (EN)

The PI4ULS5V202 has an Enable pin (EN) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O  $V_{CCB}$  and I/O  $V_{CCA}$  pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the  $V_{CCA}$  supply and has overvoltage tolerant protection.

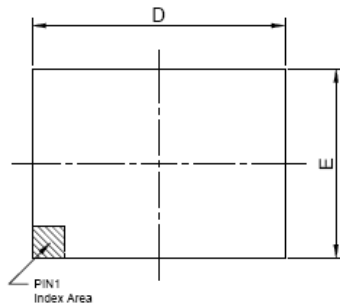
### Power Supply Guidelines

During normal operation, supply voltage  $V_{CCA}$  can be greater than, less than or equal to  $V_{CCB}$ . The sequencing of the power supplies will not damage the device during the power up operation. For optimal performance, 0.01  $\mu$ F to 0.1  $\mu$ F decoupling capacitors should be used on the  $V_{CCA}$  and  $V_{CCB}$  power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

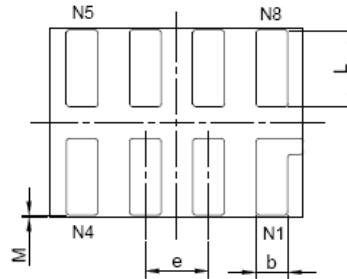


## Mechanical Information

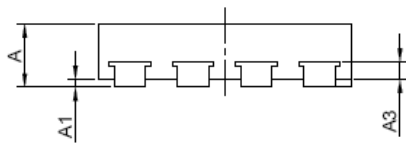
UDFN1.2x1.6-8L



TOP VIEW



BOTTOM VIEW



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.11 REF	
D	1.55	1.65
E	1.15	1.25
b	0.15	0.25
e	0.40 TYP	
L	0.45	0.55
M	0.00	0.03

Note:  
 1. Ref: JEDEC MO-287A



DATE: 06/18/13

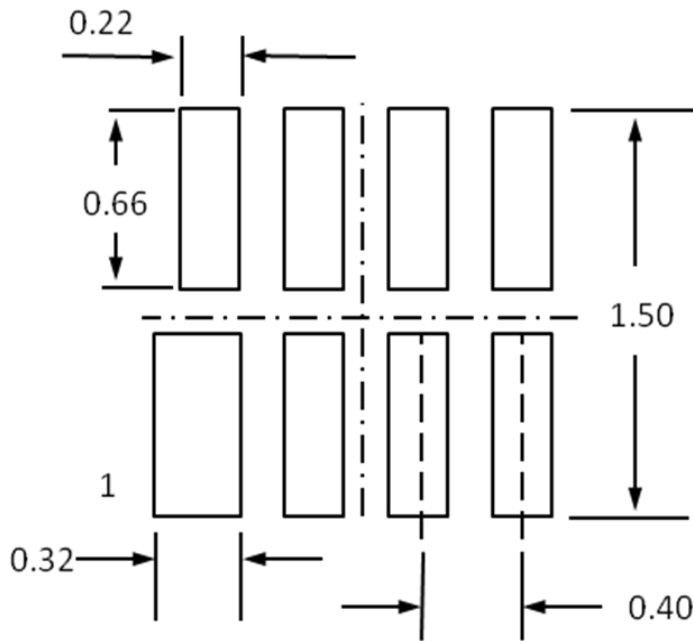
DESCRIPTION: 8-Pin, UDFN, 1.2X1.6, MIS

PACKAGE CODE: XV (XV8)

DOCUMENT CONTROL #: PD-2131

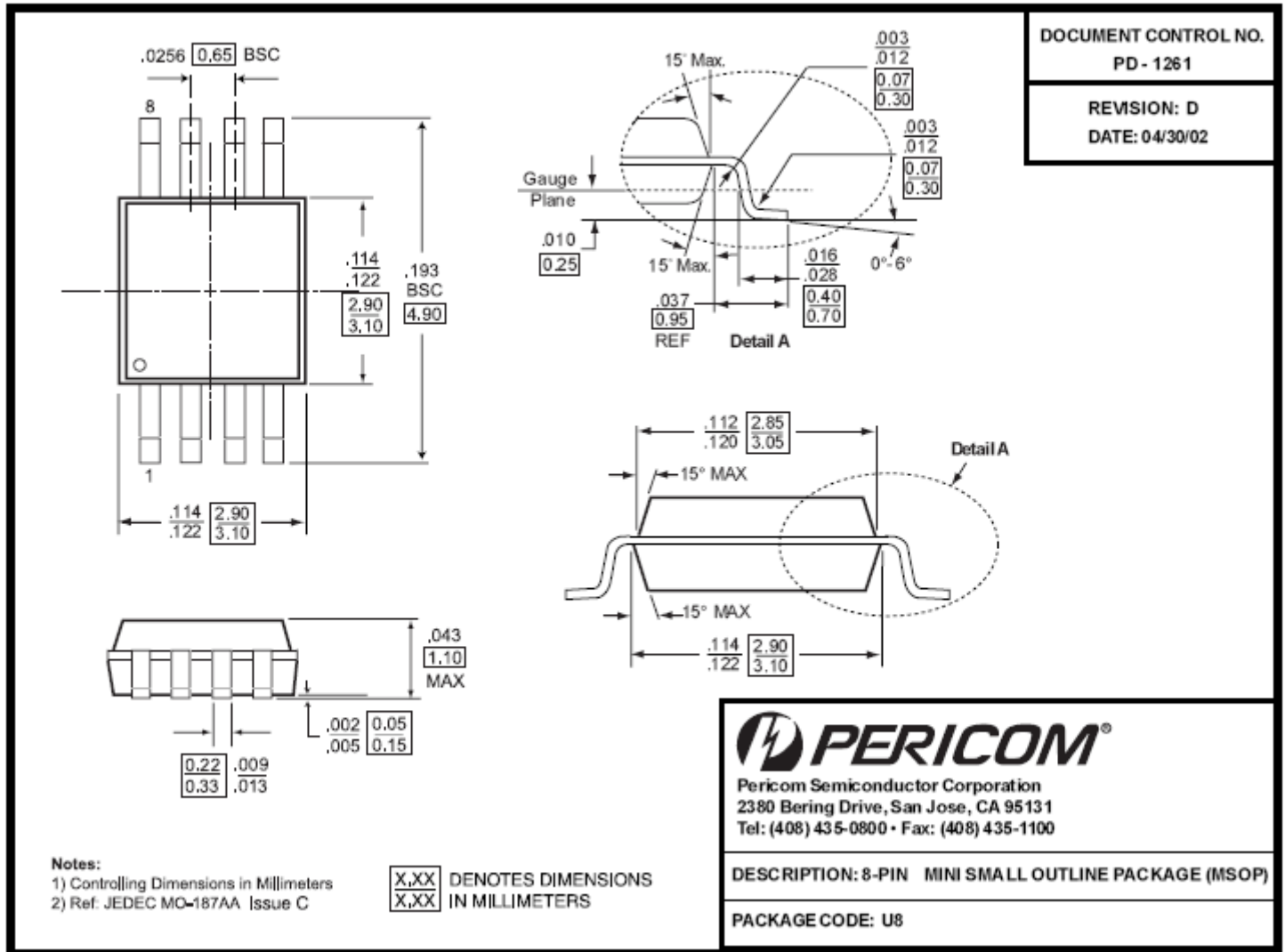
REVISION: --

**Recommended Land pattern for DFN1.6\*1.2-8L**



Note:  
All linear dimensions are in millimeters

MSOP-8



## Ordering Information

Part No.	Package Code	Package
PI4ULS5V202XVE	XV	Lead free and Green 8-pin UDFN1.2x1.6
PI4ULS5V202UE	U	Lead free and Green 8-pin MSOP

**Note:**

- E = Pb-free
- Adding X Suffix= Tape/Reel

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