Crystal Image through Imaging Innovation

PIXELPLUS

Surround View Monitoring Processor with 4CH HDR ISP

PI5008KA

Preliminary Datasheet

Rev 0.32

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1. General Description

1.1. Product Overview

The PI5008 is a high performance SVM (Surround View Monitoring) processor for automotive application. A surround view monitor system stitches multi-view from several cameras and helps to figure out where other cars and pedestrians around. Up to 4-channel video inputs can be processed to compose a surround view and outputs with user overlaid data. To reduce overall system cost, PI5008 integrates four HDR ISP in it. Four lane MIPI Rx and conventional two parallel ports with multiplexed mode are supported for video input interfaces. Digital output supporting various standard formats also can be configured to interconnect with external display devices. Dual CPU and VPU (Video Processing Unit) enables the user to implement specific functions such as object detection and some automotive related algorithms.

1.2. Features

- **CPU**
  - ✓ 32-bit Andes D10 RISC, Dual-Core
    - *Max 250MHz each, 8K/8K Cache*
  - ✓ DSP, FPU(Floating Point Unit) Embedded, 128-bit AXI Bus
- **Video Input**
  - ✓ Digital
    - 4 Lane MIPI Interface
    - Parallel 2Ch Digital Video Input: BT.1120/601, 12-bit Bayer
- **Video Output**
  - ✓ Digital
    - BT.1120 8/16-bit, BT.601 8-bit Interface
    - RGB 565/666/888
    - 4Ch Multiplexed Parallel Output for Recoding
    - Bayer Parallel Output for UVC Interface
- **DDR Interface**
  - ✓ DDR2/DDR3/LPDDR2
    - 400/500MHz, 16-bit Interface for 720p@60fps, 960p@30fps
    - 400/500MHz, 32-bit Interface for 1080p@30fps
- **4Ch ISP**
  - ✓ Input Format

  - Up to 20-bit combined raw bayer format
  - 12-bit compressed combined raw bayer format
  - 10-bit non-HDR raw bayer format
- ✓ Auto Exposure/Auto White Balance
- ✓ Color Interpolation, Spatial Noise Reduction
- ✓ Auto Defect Pixel Correction
- ✓ Edge Enhancement
- ✓ Saturation/Hue/Contrast Enhancement

◆ **Automotive Specific Functions**

- ✓ SVM/AVM
  - 2D/3D Surround View Monitoring
  - Dynamic Blending for Blind Spot
  - Brightness Control between Cameras
- ✓ VPU(Vision Processing Unit) for Optical Flow and Canny Edge Detection

◆ **Display Control**

- ✓ OSD
  - 5-BMP/RLE Overlay Layer
  - Supports 8/16/24/32(ARGB)-bit per Pixel BMP Mode

◆ **Diagnosis**

- ✓ Video Input/Output: No Video, Format Error, Freeze, Genlock Error Detection
- ✓ Flash Memory Error Detection

◆ **Peripherals**

- ✓ UART 3 ports, QSPI 1 port, SPI 3 ports, I^2C 2 ports, I^2S 1 port
- ✓ Timers, Watch Dog Timer, GPIO, General ADC 2 port, PWM

◆ **Operating Temperature/Package**

- ✓ -40~105 °C
- ✓ 369 FBGA Package

1.3. Block Diagram

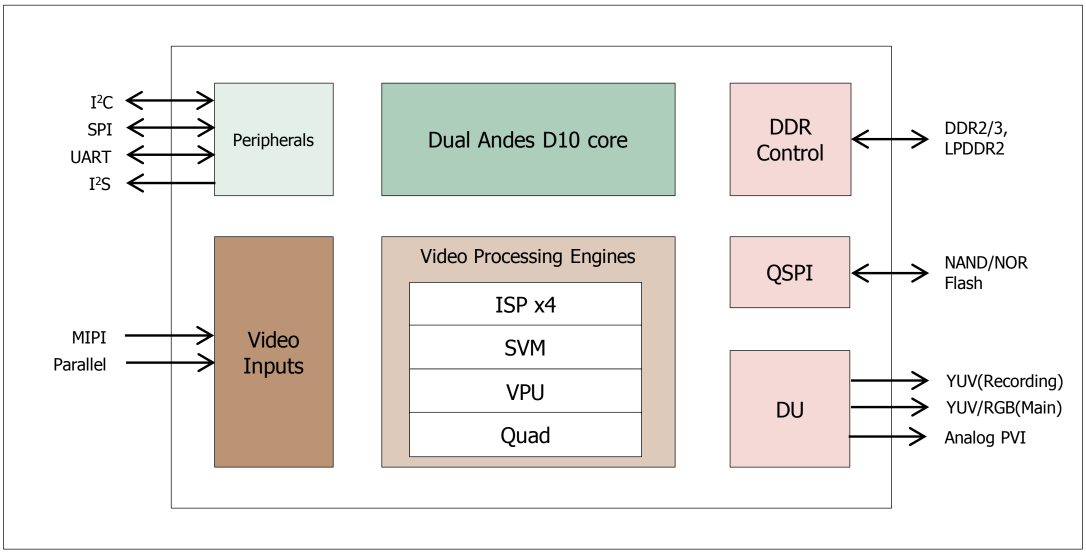


Fig 1. Functional Block Diagram

2. Pin Information

2.1. Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11
A	SPI1_MISO	SPI1_MOSI	SPI1_SS	SPI0_MOSI	SPI0_SS	VOEN	VODATA[20]	VODATA[17]	VODATA[12]	VODATA[6]	VODATA[4]
B	QSPI_SS	QSPI_SCK	SPI1_SCK	SPI0_MISO	SPI2_SS	VOCLK	VODATA[21]	VODATA[18]	VODATA[13]	VODATA[7]	VODATA[5]
C	QSPI_D0	QSPI_D1	VSS		SPI0_SCK	VSS	VODATA[22]		VSS	VODATA[8]	
D	QSPI_D2	QSPI_D3				I2C1_DAT	VODATA[23]		VODATA[14]	VODATA[9]	
E	VSS	VDD3AR0	VSS				VOHSYNC		VODATA[15]	VODATA[10]	
F	NC	NC	NC	VDD1AR0		I2C1_CLK	VOVSYNC	VODATA[19]	VODATA[16]	VODATA[11]	
G	VSS	VDD3AR1	NC	NC	NC	VSS	VDD1AR1	VDDIO3	VDDIO3	VSS	VSS
H	NC	NC				NC	VSS	VDDIO3	VDDIO3	VSS	VDDI_CORE
J	VSS	VDD3AR2	NC	NC	NC	VSS	VDD1AR2	VSS	VSS	VDDI_CORE	VDDI_CORE
K	NC	NC	NC	VSS	VDD3AR3	VDD1AR3	VSS	VSS	VSS	VDDI_CORE	VDDI_CORE
L	VSS	VDD3AT					VDD1AP0	VSS	VSS	VDDI_CORE	VDDI_CORE

Fig 2. Pin Diagram of Top/Left

12	13	14	15	16	17	18	19	20	21	
RO1_DATA[7]	RO1_DATA[2]	RO0_CLK	RO0_DATA[2]	VSS	DDR_DQ[27]	DDR_DQ[25]	DDR_DQ[31]	DDR_DQSB[3]	DDR_DQS[3]	A
RO1_CLK	RO1_DATA[3]	RO1_DATA[0]	RO0_DATA[3]	VSS	DDR_DQ[29]	DDR_DQM[3]	DDR_DQ[24]	VSS	VSS	B
VODATA[0]	VSS		RO0_DATA[4]	RO0_DATA[0]	VSS		DDR_DQ[28]	DDR_DQ[26]	DDR_DQ[30]	C
VODATA[1]	RO1_DATA[4]		RO0_DATA[5]	RO0_DATA[1]				DDR_VREF[3]	DDR_DQ[21]	D
VODATA[2]	RO1_DATA[5]		RO0_DATA[6]				DDR_DQ[19]	DDR_DQSB[2]	DDR_DQS[2]	E
VODATA[3]	RO1_DATA[6]	RO1_DATA[1]	RO0_DATA[7]	VDDI_CORE		DDR_DQM[2]	DDR_DQ[17]	VSS	VSS	F
VSS	VDDIO2	VDDIO2	VDDIO2	VDDI_CORE	DDR_DQ[23]	DDR_DQ[16]	DDR_DQ[20]	DDR_DQ[18]	DDR_DQ[22]	G
VSS	VSS	VDDIO2	VDDIO2	DDR_VREF[2]				DDR_DQ[13]	DDR_DQ[11]	H
VDDI_CORE	VSS	VSS	VDDI_DDRPHY	VDDI_DDRPHY	DDR_DQM[1]	DDR_DQ[9]	DDR_DQ[15]	DDR_DQSB[1]	DDR_DQS[1]	J
VDDI_CORE	VSS	VSS	VDDI_DDRPHY	VDDI_DDRPHY	DDR_DQ[8]	DDR_DQ[12]	DDR_DQ[10]	VSS	VSS	K
VDDI_CORE	VSS	VSS	VDDO_DDR					DDR_DQ[14]	DDR_VREF[1]	L

Fig 3. Pin Diagram of Top/Right

M	ADC_0	ADC_1	VSS	VDD3AG	VSS	VDD1AP1	VSS	VSS	VSS	VDDI_CORE	VDDI_CORE
N	VSS	VDD1AM	GPIO[0]	GPIO[5]	UART0_TX	TCK	VDD1AP2	VSS	VSS	VDDI_CORE	VDDI_CORE
P	MIPI_DATAP 0	MIPI_DATAN 0				TRSTN	VSS	VDDIO0	VDDIO0	VSS	VDDI_CORE
R	MIPI_DATAP 1	MIPI_DATAN 1	VSS	GPIO[4]	UART0_RX	SRSTN	TMS	VDDIO0	VDDIO0	VSS	VSS
T	MIPI_CLKP	MIPI_CLKN	VDD1AM	GPIO[3]		UART2_TX	TDI	VI0_D[5]	VI0_D[10]	VI1_D[1]	
U	MIPI_DATAP 2	MIPI_DATAN 2	VSS				TDO		VI0_D[9]	VI1_D[0]	
V	MIPI_DATAP 3	MIPI_DATAN 3				UART2_RX	VI0_D[2]		VI0_D[8]	VI1_PCLK	
W	VSS	VDD1AM	VSS		GPIO[7]	VSS	VI0_D[1]		VSS	VI0_VSYNC	
Y	XTALI	BOOT_MD[0]	BOOT_MD[2]	GPIO[2]	GPIO[6]	UART1_TX	VI0_D[0]	VI0_D[4]	VI0_D[7]	VI0_HSYNC	VI1_D[3]
AA	XTALO	TEST	BOOT_MD[1]	GPIO[1]	RSTB	UART1_RX	VI0_PCLK	VI0_D[3]	VI0_D[6]	VI0_D[11]	VI1_D[2]
	1	2	3	4	5	6	7	8	9	10	11

Fig 4. Pin Diagram of Bottom/Left

VDDI_CORE	VSS	VSS	VDDO_DDR	VDDO_DDR	DDR_DQ[5]	DDR_DQ[3]	DDR_DQM[0]	DDR_DQ[1]	DDR_DQ[7]	M
VDDI_CORE	VSS	VSS	VDDO_DDR	VDDO_DDR	DDR_RDRVDN	DDR_RDRVUP	DDR_DQ[0]	DDR_DQSB[0]	DDR_DQS[0]	N
VSS	VDDIO1	VDDIO1	VSS	VSS				VSS	VSS	P
VDDIO1	VDDIO1	VDDIO1	VSS	VDDO_DDR	DDR_ODT[1]	DDR_ODT[0]	DDR_DQ[4]	DDR_DQ[2]	DDR_DQ[6]	R
VI1_D[9]	I2C0_DAT	I2C0_CLK	VDDO_DDR	VDDO_DDR		DDR_VREF[0]	DDR_RASN	DDR_CASN	DDR_WEN	T
VI1_D[8]	VI1_VSYNC		DDR_BA[1]				DDR_CKE	DDR_CKB	DDR_CK	U
VI1_D[7]	VI1_HSYNC		DDR_ADDR[4]	DDR_ADDR[12]				VSS	VSS	V
VI1_D[6]	VSS		DDR_ADDR[6]	DDR_ADDR[1]	DDR_ADDR[10]		DDR_BA[2]	DDR_ADDR[3]	DDR_CSN[1]	W
VI1_D[5]	VI1_D[11]	VSS	DDR_ADDR[8]	DDR_ADDR[11]	DDR_ADDR[9]	VSS	DDR_ADDR[0]	DDR_ADDR[5]	DDR_CSN[0]	Y
VI1_D[4]	VI1_D[10]	VSS	DDR_RESETN	DDR_ADDR[14]	DDR_ADDR[13]	VSS	DDR_ADDR[2]	DDR_ADDR[7]	DDR_BA[0]	AA
12	13	14	15	16	17	18	19	20	21	

Fig 5. Pin Diagram of Bottom/Right

2.2. Pin Description

2.2.1. System pins

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
AA2	TEST	I	3.3V	VDDO0 (3.3V)	Test enable 0: Normal mode 1: Test mode	-
AA5	RSTB	I	3.3V		Main reset, Active Low	-
Y1	XTALI	I	3.3V		Crystal clock input	-
AA1	XTALO	O	3.3V		Crystal clock output	-
Y2	BOOT_MODE[0]	I	3.3V		Boot mode[2:0] 0: NOR flash boot 1: SD card boot 2: External SPI boot 3: Reserved 4: NAND flash boot Others are reserved	-
AA3	BOOT_MODE[1]	I	3.3V			
Y3	BOOT_MODE[2]	I	3.3V			
N6	TCK	I	3.3V		JTAG clock input	-
U7	TDO	O	3.3V		JTAG data output	-
T7	TDI	I	3.3V		JTAG data input	-
R7	TMS	I	3.3V		JTAG mode select	-
P6	TRSTn	I	3.3V		JTAG reset input	-
R6	SRSTn	I	3.3V		JTAG system reset input	-

2.2.2. GPIO

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
N3	GPIO[0]	B	3.3V	VDDO0 (3.3V)	General purpose IO[0]	I^2C Slave SCL
AA4	GPIO[1]	B	3.3V		General purpose IO[1]	I^2C Slave SDA
Y4	GPIO[2]	B	3.3V		General purpose IO[2]	PWM[0] I^2S Master clock
T4	GPIO[3]	B	3.3V		General purpose IO[3]	PWM[1]

R4	GPIO[4]	B	3.3V		General purpose IO[4]	HD_PTZ0 I²S CLK
N4	GPIO[5]	B	3.3V		General purpose IO[5]	HD_PTZ1 I²S SYN
Y5	GPIO[6]	B	3.3V		General purpose IO[6]	HD_PTZ3 I²S DAT
W5	GPIO[7]	B	3.3V		General purpose IO[7]	HD_PTZ3 GENLOCK_P

2.2.3. UART

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
R5	UART0_RX	I	3.3V	VDDO0 (3.3V)	UART 0 RX port	-
N5	UART0_TX	O	3.3V		UART 0 TX port	-
AA6	UART1_RX	B	3.3V		UART 1 RX port	HD_PTZ0 I²S CLK
Y6	UART1_TX	B	3.3V		UART 1 TX port	HD_PTZ1 I²S SYN
V6	UART2_RX	B	3.3V		UART 2 RX port	GPIO2[30] HD_PTZ2 I²S DAT
T6	UART2_TX	B	3.3V		UART 2 TX port	GOIO2[31] HD_PTZ3

2.2.4. Digital Video Input

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
Y7	VI0_D[0]	B	1.8/3.3V	VDDO1 (1.8/3.3V)	Parallel video 0 input data[0]	GPIO2[2] I²C Slave SCL
W7	VI0_D[1]	B	1.8/3.3V		Parallel video 0 input data[1]	GPIO2[3] I²C Slave SDA
V7	VI0_D[2]	B	1.8/3.3V		Parallel video 0 input data[2]	GPIO2[4] PWM[0]
AA8	VI0_D[3]	B	1.8/3.3V		Parallel video 0 input data[3]	GPIO2[5]

						PWM[1]
Y8	VI0_D[4]	B	1.8/3.3V		Parallel video 0 input data[4]	GPIO2[6] HD_PTZ0
T8	VI0_D[5]	B	1.8/3.3V		Parallel video 0 input data[5]	GPIO2[7] HD_PTZ1
AA9	VI0_D[6]	B	1.8/3.3V		Parallel video 0 input data[6]	GPIO2[8] HD_PTZ2
Y9	VI0_D[7]	B	1.8/3.3V		Parallel video 0 input data[7]	GPIO2[9] HD_PTZ3
V9	VI0_D[8]	B	1.8/3.3V		Parallel video 0 input data[8]	GPIO2[10] I^2S CLK
U9	VI0_D[9]	B	1.8/3.3V		Parallel video 0 input data[9]	GPIO2[11] I^2S SYN
T9	VI0_D[10]	B	1.8/3.3V		Parallel video 0 input data[10]	GPIO2[12] I^2S DAT
AA10	VI0_D[11]	B	1.8/3.3V		Parallel video 0 input data[11]	GPIO2[13]
Y10	VI0_HSYNC	B	1.8/3.3V		Parallel video 0 input hsync	GPIO2[14]
W10	VI0_VSYNC	B	1.8/3.3V		Parallel video 0 input vsync	GPIO2[15] GENLOCK_P
AA7	VI0_PCLK	B	1.8/3.3V		Parallel video 0 input clock	-
U10	VI1_D[0]	B	1.8/3.3V		Parallel video 1 input data[0]	GPIO2[16] HD_PTZ0
T10	VI1_D[1]	B	1.8/3.3V		Parallel video 1 input data[1]	GPIO2[17] HD_PTZ1
AA11	VI1_D[2]	B	1.8/3.3V		Parallel video 1 input data[2]	GPIO2[18] HD_PTZ2
Y11	VI1_D[3]	B	1.8/3.3V		Parallel video 1 input data[3]	GPIO2[19] HD_PTZ3
AA12	VI1_D[4]	B	1.8/3.3V		Parallel video 1 input data[4]	GPIO2[20] I^2C Slave SCL
Y12	VI1_D[5]	B	1.8/3.3V		Parallel video 1 input data[5]	GPIO2[21] I^2C Slave SDA
W12	VI1_D[6]	B	1.8/3.3V		Parallel video 1 input data[6]	GPIO2[22] PWM[0]
V12	VI1_D[7]	B	1.8/3.3V		Parallel video 1 input data[7]	GPIO2[23] PWM[1]

U12	VI1_D[8]	B	1.8/3.3V		Parallel video 1 input data[8]	GPIO2[24] I^{2}S CLK
T12	VI1_D[9]	B	1.8/3.3V		Parallel video 1 input data[9]	GPIO2[25] I^{2}S SYN
AA13	VI1_D[10]	B	1.8/3.3V		Parallel video 1 input data[10]	GPIO2[26] I^{2}S DAT
Y13	VI1_D[11]	B	1.8/3.3V		Parallel video 1 input data[11]	GPIO2[27]
V13	VI1_HSYNC	B	1.8/3.3V		Parallel video 1 input hsync	GPIO2[28]
U13	VI1_VSYNC	B	1.8/3.3V		Parallel video 1 input vsync	GPIO2[29] GENLOCK_P
V10	VI1_PCLK	B	1.8/3.3V		Parallel video 1 input clock	-

2.2.5. Digital Main Video Output

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
C12	VO_DATA[0]	O	1.8/3.3V	VDDO2	Video main out data[0]	-
D12	VO_DATA[1]	O	1.8/3.3V	(1.8/3.3V)	Video main out data[1]	-
E12	VO_DATA[2]	O	1.8/3.3V		Video main out data[2]	-
F12	VO_DATA[3]	O	1.8/3.3V		Video main out data[3]	-
A11	VO_DATA[4]	O	1.8/3.3V		Video main out data[4]	-
B11	VO_DATA[5]	O	1.8/3.3V		Video main out data[5]	-
A10	VO_DATA[6]	O	1.8/3.3V		Video main out data[6]	-
B10	VO_DATA[7]	O	1.8/3.3V		Video main out data[7]	-
C10	VO_DATA[8]	O	1.8/3.3V		Video main out data[8]	-
D10	VO_DATA[9]	O	1.8/3.3V		Video main out data[9]	-
E10	VO_DATA[10]	O	1.8/3.3V		Video main out data[10]	-
F10	VO_DATA[11]	O	1.8/3.3V		Video main out data[11]	-
A9	VO_DATA[12]	O	1.8/3.3V		Video main out data[12]	-
B9	VO_DATA[13]	O	1.8/3.3V		Video main out data[13]	-
D9	VO_DATA[14]	O	1.8/3.3V		Video main out data[14]	-
E9	VO_DATA[15]	O	1.8/3.3V		Video main out data[15]	-
F9	VO_DATA[16]	O	1.8/3.3V		Video main out data[16]	-
A8	VO_DATA[17]	O	1.8/3.3V		Video main out data[17]	-
B8	VO_DATA[18]	O	1.8/3.3V		Video main out data[18]	-

F8	VO_DATA[19]	O	1.8/3.3V		Video main out data[19]	-
A7	VO_DATA[20]	O	1.8/3.3V		Video main out data[20]	-
B7	VO_DATA[21]	O	1.8/3.3V		Video main out data[21]	-
C7	VO_DATA[22]	O	1.8/3.3V		Video main out data[22]	-
D7	VO_DATA[23]	O	1.8/3.3V		Video main out data[23]	-
E7	VO_HSYNC	O	1.8/3.3V		Video main out hsync	-
F7	VO_VSYNC	O	1.8/3.3V		Video main out Vsync	-
A6	VO_EN	O	1.8/3.3V		Video main out enable(valid)	-
B6	VO_CLK	O	1.8/3.3V		Video main out clock	-

2.2.6. Digital Recording Video Output

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
C16	RO0_DATA[0]	O	1.8/3.3V	VDDO2	Video recording out 0 data[0]	-
D16	RO0_DATA[1]	O	1.8/3.3V	(1.8/3.3V)	Video recording out 0 data[1]	-
A15	RO0_DATA[2]	O	1.8/3.3V		Video recording out 0 data[2]	-
B15	RO0_DATA[3]	O	1.8/3.3V		Video recording out 0 data[3]	-
C15	RO0_DATA[4]	O	1.8/3.3V		Video recording out 0 data[4]	-
D15	RO0_DATA[5]	O	1.8/3.3V		Video recording out 0 data[5]	-
E15	RO0_DATA[6]	O	1.8/3.3V		Video recording out 0 data[6]	-
F15	RO0_DATA[7]	O	1.8/3.3V		Video recording out 0 data[7]	-
A14	RO0_CLK	O	1.8/3.3V		Video recording out 0 clock	-
B14	RO1_DATA[0]	O	1.8/3.3V		Video recording out 1 data[0]	-
F14	RO1_DATA[1]	O	1.8/3.3V		Video recording out 1 data[1]	-
A13	RO1_DATA[2]	O	1.8/3.3V		Video recording out 1 data[2]	-
B13	RO1_DATA[3]	O	1.8/3.3V		Video recording out 1 data[3]	-
D13	RO1_DATA[4]	O	1.8/3.3V		Video recording out 1 data[4]	-
E13	RO1_DATA[5]	O	1.8/3.3V		Video recording out 1 data[5]	-
F13	RO1_DATA[6]	O	1.8/3.3V		Video recording out 1 data[6]	-
A12	RO1_DATA[7]	O	1.8/3.3V		Video recording out 1 data[7]	-
B12	RO1_CLK	O	1.8/3.3V		Video recording out 1 clock	-

2.2.7. SPI Interface

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
A5	SPI0_SS	B	1.8/3.3V	VDDO3 (1.8/3.3V)	SPI 0 slave select (default: master)	GPIO1[26]
B5	SPI2_SS	B	1.8/3.3V		SPI 2 slave select	GPIO1[27]
C5	SPI0_SCK	B	1.8/3.3V		SPI 0 serial clock	GPIO1[28]
A4	SPI0_MOSI	B	1.8/3.3V		SPI 0 data master output, slave input	-
B4	SPI0_MISO	B	1.8/3.3V		SPI 0 data master input, slave output	-
A3	SPI1_SS	B	1.8/3.3V		SPI 1 slave select(default: slave)	GPIO1[29]
B3	SPI1_SCK	B	1.8/3.3V		SPI 1 serial clock	GPIO1[30]
A2	SPI1_MOSI	B	1.8/3.3V		SPI 1 data master output, slave input	GPIO1[31]
A1	SPI1_MISO	B	1.8/3.3V		SPI 1 data master input, slave output	GPIO2[1]
B1	QSPI_SS	B	1.8/3.3V		Quad SPI slave select(default: master)	GPIO2[0]
B2	QSPI_SCK	B	1.8/3.3V		Quad SPI serial clock	-
C1	QSPI_D0	B	1.8/3.3V		Quad SPI data 0	-
C2	QSPI_D0	B	1.8/3.3V		Quad SPI data 1	-
D1	QSPI_D0	B	1.8/3.3V		Quad SPI data 2	-
D2	QSPI_D0	B	1.8/3.3V		Quad SPI data 3	-

2.2.8. I²C Interface

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
T13	I2C0_DAT	B	1.8/3.3V	VDDO1 (1.8/3.3V)	I²C 0 master data	GPIO1[8] MIPI_I2C_DAT
T14	I2C0_CLK	O	1.8/3.3V		I²C 0 master clock	GPIO1[9] MIPI_I2C_CLK
D6	I2C1_DAT	B	1.8/3.3V	VDDO2 (1.8/3.3V)	I²C 1 master data	-
F6	I2C1_CLK	O	1.8/3.3V		I²C 1 master clock	-

2.2.9. MIPI Interface

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
P1	MIPI_DATA_P0	I	1.2V	MIPI	MIPI data lane 0 positive input	-

P2	MIPI_DATA_N0	I	1.2V	(1.2V)	MIPI data lane 0 negative input	-
R1	MIPI_DATA_P1	I	1.2V		MIPI data lane 1 positive input	-
R2	MIPI_DATA_N1	I	1.2V		MIPI data lane 1 negative input	-
U1	MIPI_DATA_P2	I	1.2V		MIPI data lane 2 positive input	-
U2	MIPI_DATA_N2	I	1.2V		MIPI data lane 2 negative input	-
V1	MIPI_DATA_P3	I	1.2V		MIPI data lane 3 positive input	-
V2	MIPI_DATA_N3	I	1.2V		MIPI data lane 3 negative input	-
T1	MIPI_CLKP	I	1.2V		MIPI clock lane positive input	-
T2	MIPI_CLKN	I	1.2V		MIPI clock lane negative input	-

2.2.10. DDR DRAM Interface

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
Y19	DDR_ADDR[0]	O	1.5/1.8V	DDR (1.5/1.8V)	DDR DRAM address [0]	-
W16	DDR_ADDR[1]	O	1.5/1.8V		DDR DRAM address [1]	-
AA19	DDR_ADDR[2]	O	1.5/1.8V		DDR DRAM address [2]	-
W20	DDR_ADDR[3]	O	1.5/1.8V		DDR DRAM address [3]	-
V15	DDR_ADDR[4]	O	1.5/1.8V		DDR DRAM address [4]	-
Y20	DDR_ADDR[5]	O	1.5/1.8V		DDR DRAM address [5]	-
W15	DDR_ADDR[6]	O	1.5/1.8V		DDR DRAM address [6]	-
AA20	DDR_ADDR[7]	O	1.5/1.8V		DDR DRAM address [7]	-
Y15	DDR_ADDR[8]	O	1.5/1.8V		DDR DRAM address [8]	-
Y17	DDR_ADDR[9]	O	1.5/1.8V		DDR DRAM address [9]	-
W17	DDR_ADDR[10]	O	1.5/1.8V		DDR DRAM address [10]	-
Y16	DDR_ADDR[11]	O	1.5/1.8V		DDR DRAM address [11]	-
V16	DDR_ADDR[12]	O	1.5/1.8V		DDR DRAM address [12]	-
AA17	DDR_ADDR[13]	O	1.5/1.8V		DDR DRAM address [13]	-
AA16	DDR_ADDR[14]	O	1.5/1.8V		DDR DRAM address [14]	-
AA21	DDR_BA[0]	O	1.5/1.8V		DDR DRAM bank address [0]	-
U15	DDR_BA[1]	O	1.5/1.8V		DDR DRAM bank address [1]	-
W19	DDR_BA[2]	O	1.5/1.8V		DDR DRAM bank address [2]	-
U21	DDR_CK	O	1.5/1.8V		DDR DRAM positive clock	-
U20	DDR_CKB	O	1.5/1.8V		DDR DRAM negative clock	-
U19	DDR_CKE	O	1.5/1.8V		DDR DRAM clock enable	-

Y21	DDR_CSN[0]	O	1.5/1.8V		DDR DRAM chip select 0	-
W21	DDR_CSN[1]	O	1.5/1.8V		DDR DRAM chip select 1	-
T19	DDR_RASN	O	1.5/1.8V		DDR DRAM row address strobe	-
T20	DDR_CASN	O	1.5/1.8V		DDR DRAM column address strobe	-
T21	DDR_WEN	O	1.5/1.8V		DDR DRAM write enable	-
R18	DDR_ODT[0]	O	1.5/1.8V		DDR DRAM on die termination[0]	-
R17	DDR_ODT[1]	O	1.5/1.8V		DDR DRAM on die termination[1]	-
N18	DDR_RDRVUP	O	1.5/1.8V		DDR DRAM compensating the pull-up driver. It should be tied to GND through a 240Ω resistor with 1% tolerance.	-
N17	DDR_RDRVDN	O	1.5/1.8V		DDR DRAM compensating the pull-down driver. It should be tied to DDR IO PWR through a 240Ω resistor with 1% tolerance.	-
AA15	DDR_RESETN	O	1.5/1.8V		DDR DRAM reset for DDR3/DDR3L	-
N19	DDR_DQ[0]	B	1.5/1.8V		DDR DRAM data[0]	-
M20	DDR_DQ[1]	B	1.5/1.8V		DDR DRAM data[1]	-
R20	DDR_DQ[2]	B	1.5/1.8V		DDR DRAM data[2]	-
M18	DDR_DQ[3]	B	1.5/1.8V		DDR DRAM data[3]	-
R19	DDR_DQ[4]	B	1.5/1.8V		DDR DRAM data[4]	-
M17	DDR_DQ[5]	B	1.5/1.8V		DDR DRAM data[5]	-
R21	DDR_DQ[6]	B	1.5/1.8V		DDR DRAM data[6]	-
M21	DDR_DQ[7]	B	1.5/1.8V		DDR DRAM data[7]	-
K17	DDR_DQ[8]	B	1.5/1.8V		DDR DRAM data[8]	-
J18	DDR_DQ[9]	B	1.5/1.8V		DDR DRAM data[9]	-
K19	DDR_DQ[10]	B	1.5/1.8V		DDR DRAM data[10]	-
H21	DDR_DQ[11]	B	1.5/1.8V		DDR DRAM data[11]	-
K18	DDR_DQ[12]	B	1.5/1.8V		DDR DRAM data[12]	-
H20	DDR_DQ[13]	B	1.5/1.8V		DDR DRAM data[13]	-
L20	DDR_DQ[14]	B	1.5/1.8V		DDR DRAM data[14]	-
J19	DDR_DQ[15]	B	1.5/1.8V		DDR DRAM data[15]	-
G18	DDR_DQ[16]	B	1.5/1.8V		DDR DRAM data[16]	-
F19	DDR_DQ[17]	B	1.5/1.8V		DDR DRAM data[17]	-
G20	DDR_DQ[18]	B	1.5/1.8V		DDR DRAM data[18]	-

E19	DDR_DQ[19]	B	1.5/1.8V		DDR DRAM data[19]	-
G19	DDR_DQ[20]	B	1.5/1.8V		DDR DRAM data[20]	-
D21	DDR_DQ[21]	B	1.5/1.8V		DDR DRAM data[21]	-
G21	DDR_DQ[22]	B	1.5/1.8V		DDR DRAM data[22]	-
G17	DDR_DQ[23]	B	1.5/1.8V		DDR DRAM data[23]	-
B19	DDR_DQ[24]	B	1.5/1.8V		DDR DRAM data[24]	-
A18	DDR_DQ[25]	B	1.5/1.8V		DDR DRAM data[25]	-
C20	DDR_DQ[26]	B	1.5/1.8V		DDR DRAM data[26]	-
A17	DDR_DQ[27]	B	1.5/1.8V		DDR DRAM data[27]	-
C19	DDR_DQ[28]	B	1.5/1.8V		DDR DRAM data[28]	-
B17	DDR_DQ[29]	B	1.5/1.8V		DDR DRAM data[29]	-
C21	DDR_DQ[30]	B	1.5/1.8V		DDR DRAM data[30]	-
A19	DDR_DQ[31]	B	1.5/1.8V		DDR DRAM data[31]	-
N21	DDR_DQS[0]	B	1.5/1.8V		DDR DRAM positive data strobe[0]	-
J21	DDR_DQS[1]	B	1.5/1.8V		DDR DRAM positive data strobe[1]	-
E21	DDR_DQS[2]	B	1.5/1.8V		DDR DRAM positive data strobe[2]	-
A21	DDR_DQS[3]	B	1.5/1.8V		DDR DRAM positive data strobe[3]	-
N20	DDR_DQSB[0]	B	1.5/1.8V		DDR DRAM negative data strobe[0]	-
J20	DDR_DQSB[1]	B	1.5/1.8V		DDR DRAM negative data strobe[1]	-
E20	DDR_DQSB[2]	B	1.5/1.8V		DDR DRAM negative data strobe[2]	-
A20	DDR_DQSB[3]	B	1.5/1.8V		DDR DRAM negative data strobe[3]	-
M19	DDR_DQM[0]	B	1.5/1.8V		DDR DRAM data mask[0]	-
J17	DDR_DQM[1]	B	1.5/1.8V		DDR DRAM data mask[1]	-
F18	DDR_DQM[2]	B	1.5/1.8V		DDR DRAM data mask[2]	-
B18	DDR_DQM[3]	B	1.5/1.8V		DDR DRAM data mask[3]	-
T18	DDR_VREF[0]	I	1.5/1.8V		DDR DRAM reference voltage[0]	-
L21	DDR_VREF[1]	I	1.5/1.8V		DDR DRAM reference voltage[1]	-
H16	DDR_VREF[2]	I	1.5/1.8V		DDR DRAM reference voltage[2]	-
D20	DDR_VREF[3]	I	1.5/1.8V		DDR DRAM reference voltage[3]	-

2.2.11. General ADC Interface

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
M1	ADC_0	A	3.3V	Analog	General ADC input 0	-

M2	ADC_1	A	3.3V	(3.3V)	General ADC input 1	-

2.2.12. Video ADC Interface

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
F1	NC	A	1.2/3.3V	Analog (1.2/3.3V)	Reserved	-
F2	NC	A	1.2/3.3V		Reserved	-
F3	NC	A	1.2/3.3V		Reserved	-
G3	NC	A	1.2/3.3V		Reserved	-
G4	NC	A	1.2/3.3V		Reserved	-
G5	NC	A	1.2/3.3V		Reserved	-
H1	NC	A	1.2/3.3V		Reserved	-
H2	NC	A	1.2/3.3V		Reserved	-
H6	NC	A	1.2/3.3V		Reserved	-
J3	NC	A	1.2/3.3V		Reserved	-
J4	NC	A	1.2/3.3V		Reserved	-
J5	NC	A	1.2/3.3V		Reserved	-

2.2.13. Video DAC Interface

Ball No.	Pin Name	IO	Voltage	Power Group	Main Function	Alternative Function
K1	NC	A	3.3V	Analog (3.3V)	Reserved	-
K2	NC	A	3.3V		Reserved	-
K3	NC	A	3.3V		Reserved	-

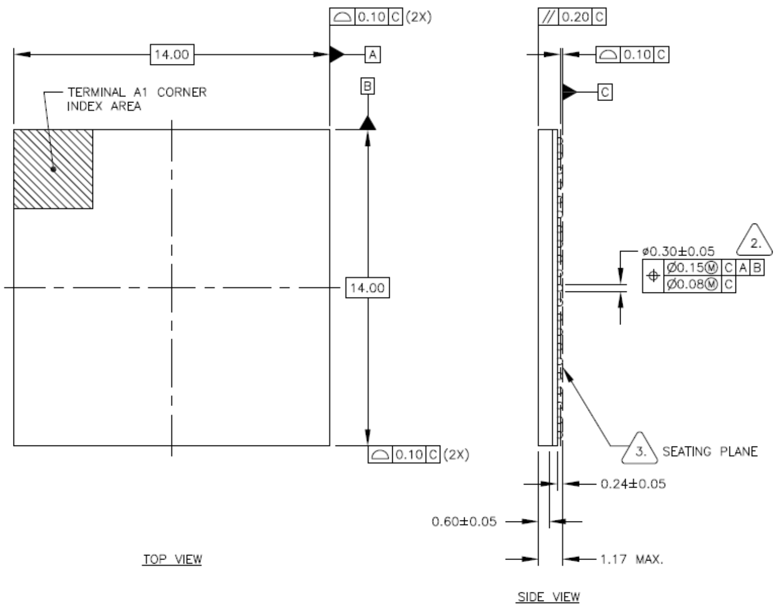
2.2.14. Powers

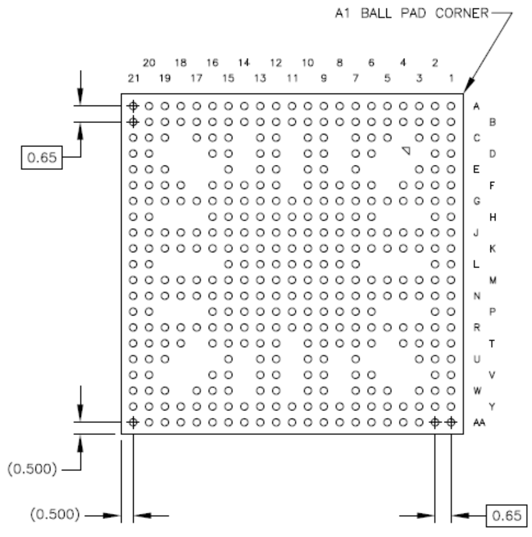
Pin Name	Ball No.	Voltage	Main Function
VDDI	F16, G16, H11, J10, J11, J12, K10, K11, K12, L10, L11, L12, M10, M11, M12, N10, N11, N12, P11	1.2V	Digital core power
VDDO0	P8, P9, R8, R9	3.3V	Digital IO power group 0
VDDO1	P13, P14, R12, R13, R14	1.8/3.3V	Digital IO power group 1

VDDO2	G13, G14, G15, H14, H15	1.8/3.3V	Digital IO power group 2
VDDO3	G8, G9, H8, H9	1.8/3.3V	Digital IO power group 3
VDD1AM	N2, T3, W2	1.2V	Analog MIPI power
VDDI_DDRPHY	J15, J16, K15, K16	1.2V	DDR PHY core and DDR PLL power
VDDO_DDR	L15, M15, M16, N15, N16, R16, T15, T16	1.5/1.8V	DDR IO power
VDD3AG	M4	3.3V	General ADC power
VDD1AR0	F4	1.25V	Analog power for VADC0
VDD3AR0	E2	3.3V	Analog power for VADC0
VDD1AR1	G7	1.25V	Analog power for VADC1
VDD3AR1	G2	3.3V	Analog power for VADC1
VDD1AR2	J7	1.25V	Analog power for VADC2
VDD3AR2	J2	3.3V	Analog power for VADC2
VDD1AR3	K6	1.25V	Analog power for VADC3
VDD3AR3	K5	3.3V	Analog power for VADC3
VDD3AT	L2	3.3V	Analog power for VDAC
VDD1AP0	L7	1.2V	Analog power for PLL0(FPLL)
VDD1AP1	M6	1.2V	Analog power for PLL1(MPLL0)
VDD1AP2	N7	1.2V	Analog power for PLL2(MPLL1)
VSS	A16, B16, B20, B21, C3, C6, C9, C13, C17, E1, E3, F20, F21, G1, G6, G10, G11, G12, H7, H10, H12, H13, J1, J6, J8, J9, J13, J14, K4, K7, K8, K9, K13, K14, K20, K21, L1, L8, L9, L13, L14, M3, M5, M7, M8, M9, M13, M14, N1, N8, N9, N13, N14, P7, P10, P12, P15, P16, P20, P21, R3, R10, R11, R15, U3, V20, V21, W1, W3, W6, W9, W13, Y14, Y18, AA14, AA18	1.2/1.5/1.8/3.3V	Ground

2.3. Package Specification

PI5008KA package type is 369 FBGA. Package mechanical drawing is as below.





BOTTOM VIEW
369 SOLDER BALLS

4. REFERENCE SPECIFICATIONS:
   A. AWW SPEC #001-2234: PACKING OPERATION PROCEDURE
   B. AWW SPEC #001-2062: MARKING

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5 – 2009

NOTES: UNLESS OTHERWISE SPECIFIED

3. Functional Description

3.1. Clock and Reset

3.1.1. Clock

For the clock fed at internal processing blocks and CPU, PI5008 includes one FPLL and two MPLL. FPLL is used to generate clocks needed for CPU, Bus and SVM block. DDR DRAM interface clock is also originated from the FPLL. To generate various operating clocks for video processing block such as VPU, DU and Quad, two MPLL should be set correctly depending on video input and output video resolution frequency. The main clock is fixed to 27MHz, which is used for reference clock of all PLLs and fed at PI5008 by crystal oscillator pad (XTALI, XTALO). The SCU (System Control Unit) in PI5008 provides various clocks selectively to each functional block as figure below. Changing clock frequency, disabling unused clocks for reducing power dissipation also can be controlled by setting the SCU.

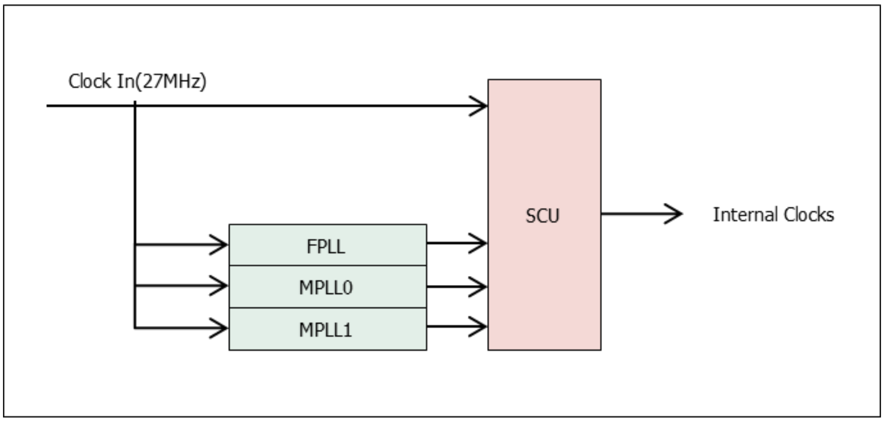


Fig 6. Clock Generation and Control Scheme

Since the FPLL generates CPU and DDR DRAM interface clock, there are some clock dependency between them. When the DDR DRAM interface clock frequency is 500MHz, CPU clock frequency can be set to operate at 250MHz, but the DDR DRAM interface clock frequency is 400MHz, maximum CPU clock is limited to 200MHz.

3.1.2. Reset

For initialization, PI5008 requires reset fed from the external. The reset pin (RSTB) is asynchronous LOW active input. The width of reset pulse should be above 1 cycle of main clock (27MHz). The reset pulse is clocked by main clock within PI5008 and regenerated within PI5008.

3.1.3. Power-Up Sequence

PI5008 utilizes multiple power rails. The digital core and IO powers, analog and DDR powers are needed depending on the application system in which PI5008 chip is used. Basically, 1.8V is strongly recommended to save power for digital IO signals. All power domains for driving PI5008 are shown in the following table.

Table 1. Power Domain Information

Power Domain	Voltage	Ball Number	Comment
VDDI	1.2V	H11/J10/J11/J12/K10/ K11/K12/L10/L11/L12/ M10/M11/M12/N10/N11/ N12/P11/F16/G16	Digital Core 1.2V Power
VDD1AP0~2		L7/M6/N7	Analog PLL 1.2V Power
VDD1AM		N2/T3/W2	MIPI 1.2V Power
VDDI_DDRPHY		J15/J16/K15/K16	DDR PHY 1.2V Power
VDD1AR0~3	1.25V	F4/G7/J7/K6	Analog VADC 1.25V Power
VDDO_DDR	1.8V/1.5V	L15/M15/M16/N15/N16/ R16/T15/T16	DDR PHY IO (1.8 or 1.5V) Power
VDDO0	1.8V/3.3V	P8/P9/R8/R9	IO_0 Group (3.3V Only) Power
VDDO1		P13/P14/R12/R13/R14	IO_1 Group (1.8V or 3.3V) Power
VDDO2		G13/G14/G15/H14/H15	IO_2 Group (1.8V or 3.3V) Power
VDDO3		G8/G9/H8/H9	IO_3 Group (1.8V or 3.3V) Power
VDD3AR0~3		E2/G2/J2/K5	Analog VADC 3.3V Power
VDD3AG		M4	Analog GADC 3.3V Power
VDD3AT		L2	Analog VDAC 3.3V Power

To prevent the leakage current that may occur in the power sequence, and for the reliable operation, power-up should be done in the order of high to low voltage, and down sequencing should be done in the opposite process.

3.2. CPU platform

3.2.1. Overview

PI5008 includes two D10 processors with 2 way 8Kbyte instruction cache and data cache each. It supports DSP function and single-precision FPU (Floating Point Unit) and has an ICE debugger that uses the JTAG interface. Both CPU can be used for user application when the internal ISP does not need to be running, but basically secondary sub-CPU is allocated to ISP operation control. CPU platform and bus architecture is based on high performance AXI bus protocol. Each CPU can access any sub block in the bus according to memory mapped addressing and communicate each other through mail box block. The full CPU platform interconnections are shown in the following figure.

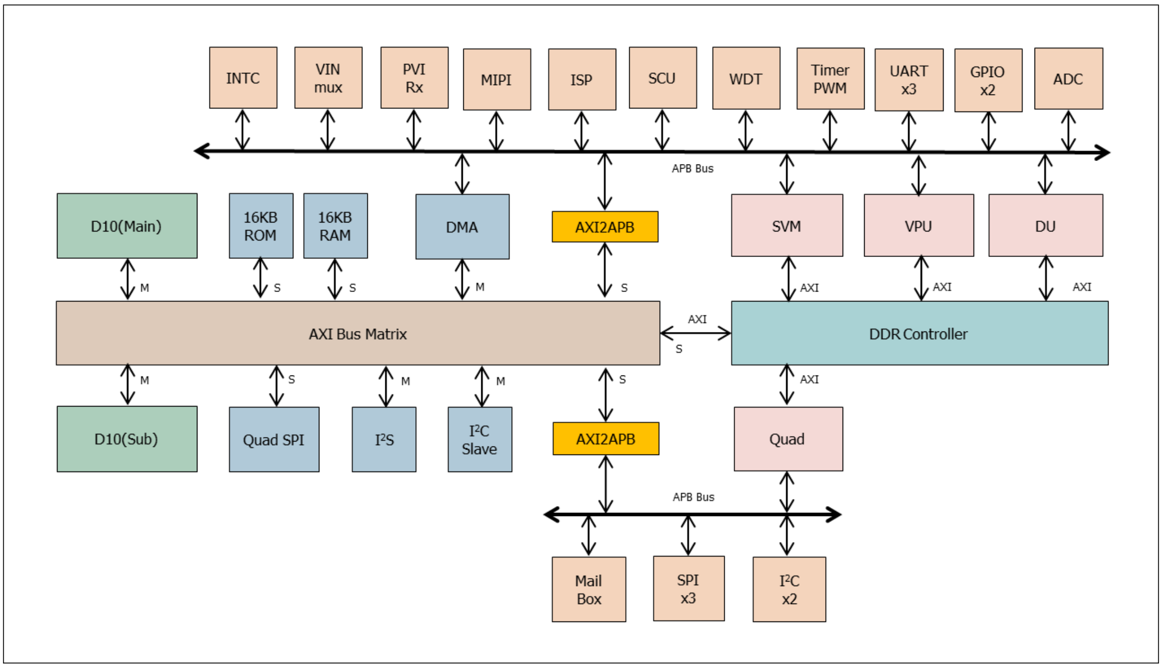


Fig 7. CPU Platform Interconnection

3.2.2. Main Features

- Two 32-bit RISC CPU (Andes D1088-S):
  - ✓ Max. 250MHz, 8K/8K Cache
  - ✓ DSP/FPU (Single Precision) imbedded
- General DMA (8 channel)
- SPI type NAND/NOR flash interface
- DDR2/3, LPDDR2 controller/PHY
- Watch-Dog Timer

- 3 ports General SPI master/slave
- 8 channel timer/PWM
- 3 ports UART
- 1 port I^2S for audio output
- 2 ports I^2C master/slave, 1 port I^2C slave(proprietary)
- 64 ports GPIO (2 channel, 32 ports per channel)
- 2 ports General purpose ADC

3.2.3. Boot Mode

Since the PI5008 operation is based on CPU, boot sequence is necessary for initialization. During the boot sequence, PI5008 loads the program code from external flash, SD card, UART or SPI interface of the other external application CPU. This boot mode is selected by BOOTMODE[2:0] pins as table below.

Table 2. Boot Mode

Boot Mode	BOOTMODE[2:0]	Comments
NOR Flash	3'b000	Boot from external NOR type flash
SD Card	3'b001	Boot from external SD Card , QSPI port is dedicated to this boot mode. *NOTE: single bit serial mode only supported
SPI slave	3'b010	Boot from external Application CPU, SPI1 port is dedicated to this boot mode
NAND Flash	3'b100	Boot from external NAND type flash

In order to support various boot sequence, internal 16Kbytes ROM contains boot code that reads bootloader program from external device (ex. Flash memory) just after reset sequence. The bootloader in 16Kbytes SRAM normally initializes PLLs and DDR DRAM controller first and loads application program to external DDR DRAM memory.

3.2.4. Flash Interface

Flash memory controller in PI5008 accesses the external SPI type flash. For the automotive SVM system, fast booting is necessary and it mostly depends on flash read performance. PI5008 flash read interface supports quad mode and specific DMA dedicated to transfer from the flash to external DDR DRAM directly. Since the erase and write flash speed mainly just depends on the internal flash execution time, configurable single mode SPI interface is used for these operations. Other features of PI5008 flash controller are as below:

- Supports NOR/NAND flash memory
- 24/32-bit address mode
- Max. 256M-byte flash access
- Max. 64MHz interface clock

3.2.5. DDR DRAM Interface

The video processing blocks including SVM and two CPU requires external DDR DRAM to process their own function. As figure below, DDR DRAM interface consists of DDR controller and PHY. Each video processing block and CPU can access the DDR DRAM by requesting permission to DDR controller.

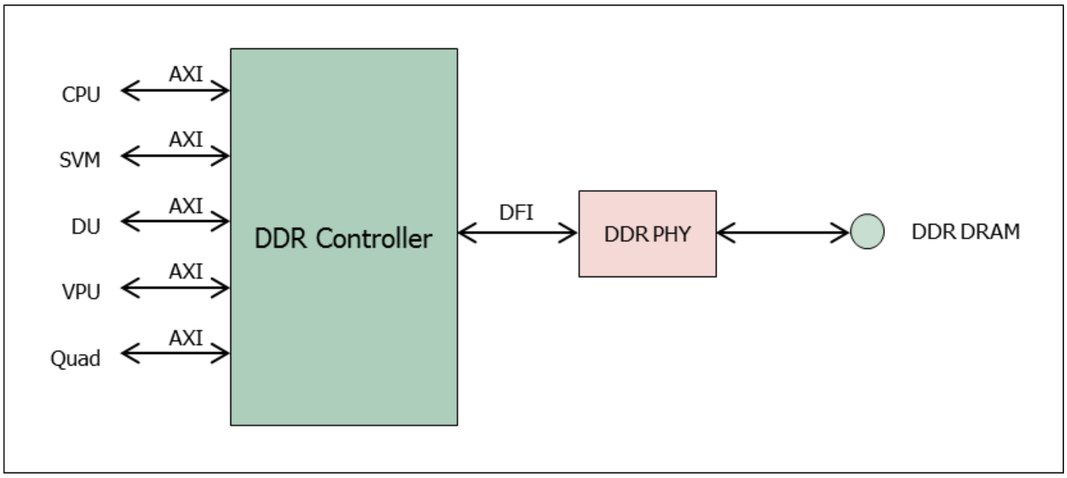


Fig 8. DDR DRAM Interface

The main feature of DDR DRAM interface is as below:

- DDR2(1.8V), DDR3(1.5V), LPDDR2(1.2V)
- Max. interface frequency is 500MHz(DDR1000) for DDR2/DDR3, 400MHz(DDR800) for LPDDR2: *Note: 400MHz interface clock is minimum frequency for all type DDR DRAM
- 16-bit or 32-bit interface
- Max. 2Gbyte addressing

The DDR DRAM clock frequency required for PI5008 to operate depends on the CPU performance, display overlay mode and whether the Quad function is used or not, but it is mainly related to the video resolution and frame rate (25/30/50/60Hz). Recommended DDR DRAM requirement for the major video input, output resolutions are shown in the following table.

Table 3. Recommended DDR DRAM requirement for the major video resolution

Input Resolution	**Output Resolution**	**DDR Interface Bus Width**	**Min. Interface Clock Frequency**
SD 720/960H 60Hz	SD 720/960H 60Hz	16-bit	400MHz
HD 1280x720 30Hz	HD 1280x720 30Hz	16-bit	400MHz
HD 1280x960 30Hz	HD 1280x720 30Hz	16-bit	500MHz
HD 1280x720 60Hz	HD 1280x720 60Hz	32-bit	500MHz
HD 1280x960 30Hz	HD 1280x960 30Hz	32-bit	400MHz
FHD 1920x1080 30Hz	FHD 1920x1080 30Hz	32-bit	500MHz

The DDR DRAM controller can support up to 2Gbyte DDR DRAM, but it depends on the DDR DRAM type and bit width as shown in the table below. It is assumed that DDR2 and DDR3 devices usually support up to 16-bit data bus width per chip, and LPDDR2 supports 16-bit or 32-bit per chip.

Table 4. DDR DRAM configuration

16-bit DDR2 case			
Row x Column x Bank	Total Memory Size	DDR Chip Configuration	Number of DDR Chip
13x10x3	128Mbytes	64Mbits x 16 (1Gbits)	1
14x10x3	256Mbytes	128Mbits x 16 (2Gbits)	1
15x10x3	512Mbytes	512Mbits x 16 (4Gbits)	1
32-bit DDR2 case			
13x10x3	256Mbytes	64Mbits x 16 (1Gbits)	2
14x10x3	512Mbytes	128Mbits x 16 (2Gbits)	2
15x10x3	1Gbytes	256Mbits x 16 (4Gbits)	2
16-bit DDR3 case			
12x10x3	64Mbytes	32Mbits x 16 (512Mbits)	1
13x10x3	128Mbytes	64Mbits x 16 (1Gbits)	1
14x10x3	256Mbytes	128Mbits x 16 (2Gbits)	1
15x10x3	512Mbytes	256Mbits x 16 (4Gbits)	1
32-bit DDR3 case			

12x10x3	128Mbytes	32Mbits x 16 (512Mbits)	2
13x10x3	256Mbytes	64Mbits x 16 (1Gbits)	2
14x10x3	512Mbytes	128Mbits x 16 (2Gbits)	2
15x10x3	1Gbytes	256Mbits x 16 (4Gbits)	2
16/32-bit LPDDR2			
13x9x2	64Mbytes	32Mbits x 16 (256Mbits)	2
		16Mbits x 32 (512Mbits)	1
13x10x2	128Mbytes	32Mbits x 16 (512Mbits)	2
13x9x3		32Mbits x 32 (1Gbits)	1
13x10x3	256Mbytes	64Mbits x 16 (1Gbits)	2
14x9x3		64Mbits x 32 (2Gbits)	1
14x10x3	512Mbytes	128Mbits x 16 (2Gbits)	2
		128Mbits x 32 (4Gbits)	1
15x10x3	1Gbytes	256Mbits x 32 (8Gbits)	1

3.2.6. DMA Controller

DMAC is a direct memory access controller that enhances system performance by transferring large data blocks between memories in background without CPU intervention. The features of the DMAC are as below.

- Up to 8 configurable DMA channels
- Group round-robin arbitration scheme with 2 priority levels
- 8, 16 and 32-bit width data transfer
- Supports chained transfer mode

3.2.7. UART Interface

Three UART interfaces are built in PI5008 and available for debugging and communication with external devices. All UART interface ports are user configurable to use. Main features of the UART are as below:

- Programmable baud rate control: Max. 230400
- HW configurable 16, 32, 64 and 128 bytes Tx/Rx FIFO with DMA
- 5~8 bits per character

- 1, 1.5 and 2 stop bits
- Even, odd and stick parity bits
- Line break, parity error, framing errors and data overrun detection

3.2.8. I²C Interface

PI5008 includes three I²C ports, two of them (General I²C) support both master and slave mode, and the other one (Specific I²C) supports slave mode only for special purpose (communication with ISP tuning tool). The pins of general I²C are dedicated, but specific I²C pin is shared with other pins. All I²C ports do not have pull-up resistance within PI5008. Therefore, it is necessary to attach pull-up resistance on the outside. Main features of the I²C are as below:

- Data format: 7/10-bit address
- Slave mode format: programmable
- Master mode:
  - ✓ 1 byte address + 1 byte data
  - ✓ 1 byte address + 2 byte data
  - ✓ 2 byte address + 1 byte data
  - ✓ 2 byte address + 2 byte data
- Speed: Fast mode(max. 400Kbit/sec), Standard mode(max. 100Kbit.sec)

3.2.9. I²S Interface

The I²S (Integrated Inter-IC Sound) is a serial bus interface standard for connecting digital audio devices. It is originally bi-directional interface standard, but the I²S block of PI5008 operates as a transmitter only. It reads PCM data using DMA and transmits the PCM data to external audio IC. I²S interface pins are shared with other pins. Main features are as below:

- 1 channel transmitter only
- 16/24/32 bit PCM data (Stereo support only)
- 8/16/32K sampling rate
- Master/slave clock mode

Since the I²S master clock is typically 24.576MHz, using master clock mode needs dedicated clock fed from external. On the contrary, slave clock mode does not need extra clock from the outside.

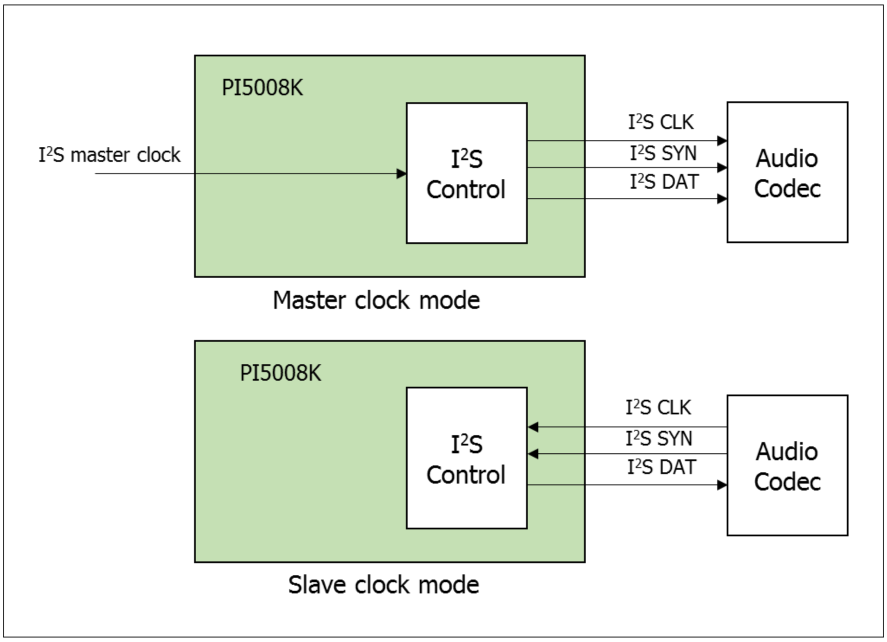


Fig 9. I2S Interface Mode

3.2.10. SPI Interface

Besides The QSPI which is mainly targeted at flash interface, PI5008 supports three general SPI interfaces. Among them, SPI port 0 and 2 shares interface pins except slave select pin (SPI0_SS, SPI2_SS). When the port 0, 2 are needed to be used at the same time, by setting both ports as master, PI5008 can control each slave device. The SPI port 1 is dedicated to boot mode in which the external CPU having its own flash memory can boot PI5008 through SPI port 1. For this purpose, port 1 automatically enters the slave mode just after reset sequence. The maximum general SPI interface clock frequency is 32MHz around and can be configurable.

3.2.11. Timers/PWM

There are eight 32-bit timers in PI5008. All eight timers are available for user application, especially, fourth and fifth timers are connected to PWM (Pulse Width Modulation) function which is used for wide range of purpose. PWM signal can be emitted to outside by alternative pin selection. User can select various timer clocks divided from main clock (27MHz) as range 1/2 to 1/16.

3.2.12. Watch-Dog Timer

The watch-dog timer is used to reset the whole chip when the firmware runs out of order or some systematic error detected. It is consists 32-bit counter and its clock is selected as the timer clock source.

3.2.13. General ADC

PI5008 includes two general purpose ADC having 8-bit precision. It converts 0~3.3V analog input to 8-bit digital output. Sampling rate is quite slow and it is about 128K samples/sec.

3.2.14. General Purpose I/O

PI5008 has all sixty four GPIO (General Purpose I/O) pins. Each pin, which is a bi-directional buffer, may be used in input mode or output mode by program. When each GPIO is used in the input mode, it may be used as an external interrupt source. By signal level or edge fed to GPIO pins, interrupt may be transmitted to PI5008 CPU. The use of level and edge, and the decision of interrupt source of high/low level and rising/falling edge all may be selected by program.

Sixty four GPIO is composed of two 32-bit GPIO groups, GPIO1[31:0] and GPIO2[31:0] internally. Among all GPIOs only eight bit (GPIO1[7:0]) is assigned to dedicate pins (GPIO[7:0]). Other GPIOs are usable by selecting alternative pin configuration.

3.3. Video Input

PI5008 supports parallel port, MIPI Rx and analog HD Rx interface for multi-channel video input. The functional block diagram of video input interface is shown as the following figure.

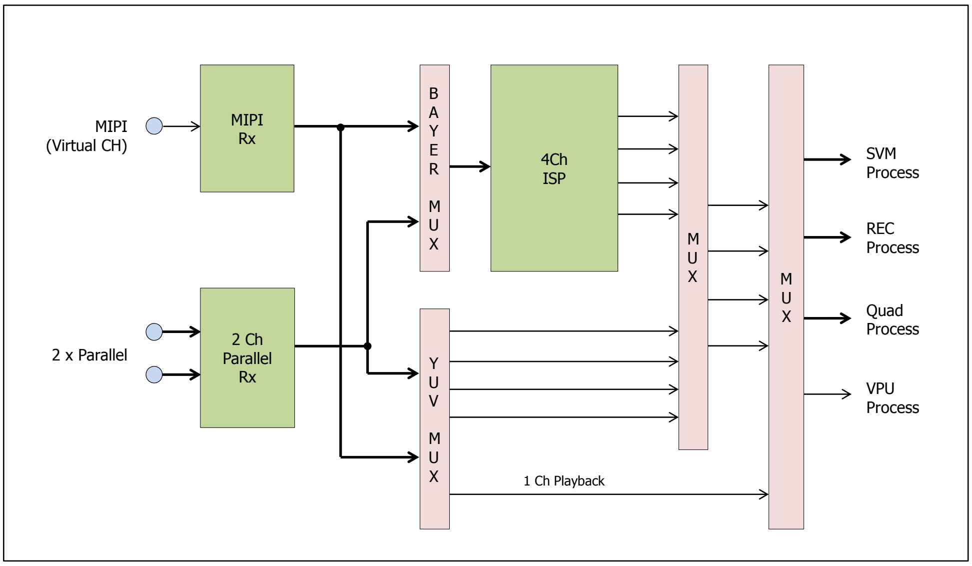


Fig 10. Block Diagram of Video Input Interface

3.3.1. Parallel port Interface

3.3.1.1. Parallel Port Map

PI5008 supports 10/12/16/20 Bit Bayer and 8 Bit YcbCr 4:2:2 video input with various pin configuration as the following table. PI5008 also supports 2 or 4 channel multiplexed mode for 8 Bit YcbCr video input to save port number.

Table 5. SDR/HDR Bayer and 8bit YcbCr Pin Map

Pin Name	8 Bits	Single Bayer Mode		HDR Bayer Mode	
	YcbCr	10 Bit Bayer	12 Bit Bayer	16 Bits	20 Bits
VI0_D[11]	YcbCr[7]	Bayer[9]	Bayer[11]	Bayer[7] / Bayer[15]	Bayer[9] / Bayer[19]
VI0_D[10]	YcbCr[6]	Bayer[8]	Bayer[10]	Bayer[6] / Bayer[14]	Bayer[8] / Bayer[18]
VI0_D[9]	YcbCr[5]	Bayer[7]	Bayer[9]	Bayer[5] / Bayer[13]	Bayer[7] / Bayer[17]
VI0_D[8]	YcbCr[4]	Bayer[6]	Bayer[8]	Bayer[4] / Bayer[12]	Bayer[6] / Bayer[16]
VI0_D[7]	YcbCr[3]	Bayer[5]	Bayer[7]	Bayer[3] / Bayer[11]	Bayer[5] / Bayer[15]
VI0_D[6]	YcbCr[2]	Bayer[4]	Bayer[6]	Bayer[2] / Bayer[10]	Bayer[4] / Bayer[14]
VI0_D[5]	YcbCr[1]	Bayer[3]	Bayer[5]	Bayer[1] / Bayer[9]	Bayer[3] / Bayer[13]
VI0_D[4]	YcbCr[0]	Bayer[2]	Bayer[4]	Bayer[0] / Bayer[8]	Bayer[2] / Bayer[12]
VI0_D[3]		Bayer[1]	Bayer[3]		Bayer[1] / Bayer[11]
VI0_D[2]		Bayer[0]	Bayer[2]		Bayer[0] / Bayer[10]
VI0_D[1]			Bayer[1]		
VI0_D[0]			Bayer[0]		
VI1_D[11]	YcbCr[7]	Bayer[9]	Bayer[11]	Bayer[7] / Bayer[15]	Bayer[9] / Bayer[19]
VI1_D[10]	YcbCr[6]	Bayer[8]	Bayer[10]	Bayer[6] / Bayer[14]	Bayer[8] / Bayer[18]
VI1_D[9]	YcbCr[5]	Bayer[7]	Bayer[9]	Bayer[5] / Bayer[13]	Bayer[7] / Bayer[17]
VI1_D[8]	YcbCr[4]	Bayer[6]	Bayer[8]	Bayer[4] / Bayer[12]	Bayer[6] / Bayer[16]
VI1_D[7]	YcbCr[3]	Bayer[5]	Bayer[7]	Bayer[3] / Bayer[11]	Bayer[5] / Bayer[15]
VI1_D[6]	YcbCr[2]	Bayer[4]	Bayer[6]	Bayer[2] / Bayer[10]	Bayer[4] / Bayer[14]
VI1_D[5]	YcbCr[1]	Bayer[3]	Bayer[5]	Bayer[1] / Bayer[9]	Bayer[3] / Bayer[13]
VI1_D[4]	YcbCr[0]	Bayer[2]	Bayer[4]	Bayer[0] / Bayer[8]	Bayer[2] / Bayer[12]
VI1_D[3]		Bayer[1]	Bayer[3]		Bayer[1] / Bayer[11]
VI1_D[2]		Bayer[0]	Bayer[2]		Bayer[0] / Bayer[10]
VI1_D[1]			Bayer[1]		
VI1_D[0]			Bayer[0]		

PI5008 supports 16 Bits/24 Bits YcbCr and RGB mode with VD0_D and VD1_D pin combination as the following table.

Table 6. 16 Bit YcbCr and 24 Bit YcbCr/RGB Pin Map

Pin Name	16 Bit 4:2:2 YcbCr Mode				24 Bits RGB / YcbCr Mode	
	Mode0	Mode1	Mode2	Mode 3	RGB Mode	YcbCr Mode
VI0_PCLK	PCLK					
VI0_VSYNC	VSYNC					
VI0_HSYNC	HSYNC					
VI0_D[11]	Y[7]			Y[7]	B[7]	Cr[7]
VI0_D[10]	Y[6]			Y[6]	B[6]	Cr[6]
VI0_D[9]	Y[5]			Y[5]	B[5]	Cr[5]
VI0_D[8]	Y[4]			Y[4]	B[4]	Cr[4]
VI0_D[7]	Y[3]	Y[7]		Y[3]	B[3]	Cr[3]
VI0_D[6]	Y[2]	Y[6]		Y[2]	B[2]	Cr[2]
VI0_D[5]	Y[1]	Y[5]		Y[1]	B[1]	Cr[1]
VI0_D[4]	Y[0]	Y[4]		Y[0]	B[0]	Cr[0]
VI0_D[3]		Y[3]	Y[7]	C[7]	G[7]	Cb[7]
VI0_D[2]		Y[2]	Y[6]	C[6]	G[6]	Cb[6]
VI0_D[1]		Y[1]	Y[5]	C[5]	G[5]	Cb[5]
VI0_D[0]		Y[0]	Y[4]	C[4]	G[4]	Cb[4]
VI1_D[11]	C[7]		Y[3]	C[3]	G[3]	Cb[3]
VI1_D[10]	C[6]		Y[2]	C[2]	G[2]	Cb[2]
VI1_D[9]	C[5]		Y[1]	C[0]	G[1]	Cb[1]
VI1_D[8]	C[4]		Y[0]	C[1]	G[0]	Cb[0]
VI1_D[7]	C[3]	C[7]	C[7]		R[7]	Y[7]
VI1_D[6]	C[2]	C[6]	C[6]		R[6]	Y[6]
VI1_D[5]	C[0]	C[5]	C[5]		R[5]	Y[5]
VI1_D[4]	C[1]	C[4]	C[4]		R[4]	Y[4]
VI1_D[3]		C[3]	C[3]		R[3]	Y[3]
VI1_D[2]		C[2]	C[2]		R[2]	Y[2]
VI1_D[1]		C[0]	C[0]		R[1]	Y[1]
VI1_D[0]		C[1]	C[1]		R[0]	Y[0]

3.3.1.2. Parallel Input Format

PI5008 supports either external sync or embedded sync mode with ITU-R BT.656/1302/1120 standard format. The following figures show the timing diagram of one channel standard ITU-R BT.656/1302/ 1120 format.

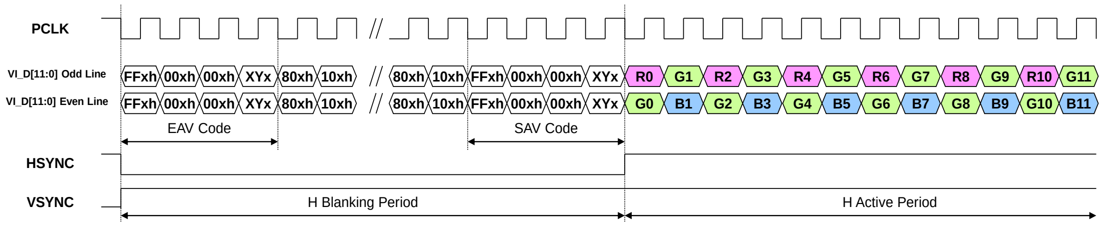


Fig 11. Timing Diagram of One Channel Standard ITU-R BT.656/1302 Format

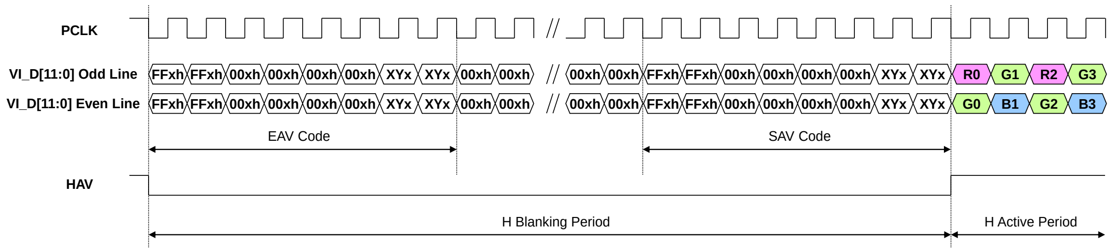


Fig 12. Timing Diagram of One Channel Standard ITU-R BT.1120 Format

In embedded sync mode, PI5008 supports multiplexed input with two or four video channels at 2 or 4 times of pixel clock, and each channel is compatible with ITU-R BT.656/1302/1120 format as following figure.

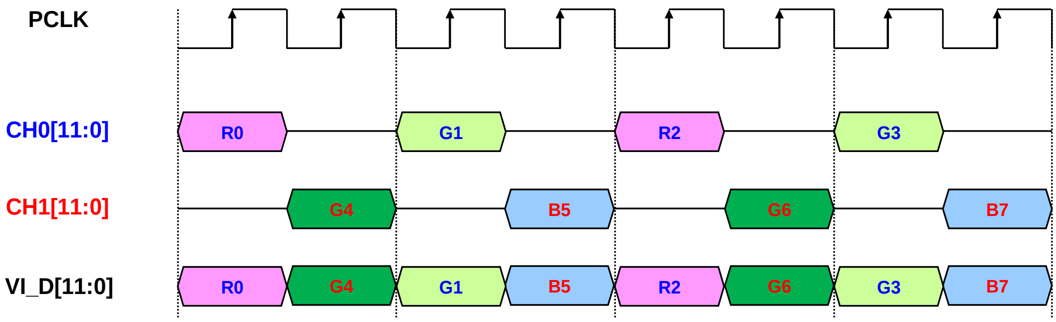


Fig 13. Timing Diagram of Two Channel Multiplexed Format

In the multi-channel multiplexed mode, the channel ID should be included in SAV/EAV LSB code in ITU-R BT.656/1120 format as shown in the following table.

Table 7. Channel ID Insertion in SAV/EAV Code for 2 Channels in ITU-R BT.656 Format

Condition			FVH Value			SAV/EAV Code Sequence for Four CH Format				
Field	V time	H time	F	V	H	1st	2nd	3rd	4th CH1	4th CH2
Even	Blank	EAV	1	1	1	FFh	00h	00h	F0h	F1h
		SAV			0				E0h	E1h
	Active	EAV		0	1				D0h	D1h
		SAV			0				C0h	C1h
Odd	Blank	EAV	0	1	1				B0h	B1h
		SAV			0				A0h	A1h
	Active	EAV		0	1				90h	91h
		SAV			0				80h	81h

Table 8. Channel ID Insertion in SAV/EAV Code for 2 Channels in ITU-R BT.1120 Format

Condition		VH Value		SAV/EAV Code Sequence for Four CH Format				
V time	H time	V	H	1st 2nd	3rd 4th	5th 6th	7th/8th CH1	7th/8th CH2
Blank	EAV	1	1	FFh	00h	00h	B0h	B1h
	SAV		0				A0h	A1h
Active	EAV	0	1				90h	91h
	SAV		0				80h	81h

3.3.2. MIPI Rx Interface

PI5008 supports MIPI Rx interface compliant with MIPI CSI2 V1.3 standard and DPHY V1.2 standard through 1 clock lane and 4 data lanes. The max data rate of MIPI data lane is up to 1296Mbps in HS transmission.

The MIPI data lane transmission order for 4 lane and 2 lane mode is described in the following figure.

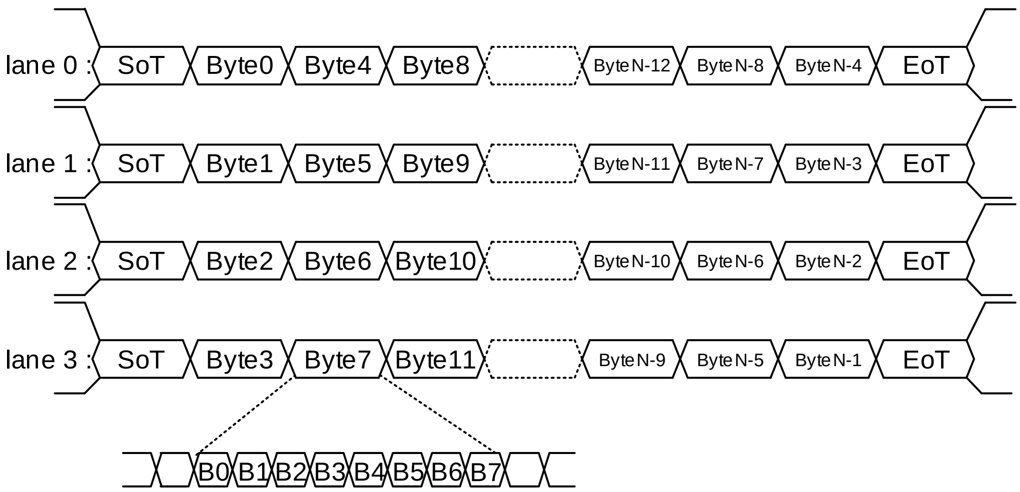


Fig 14. MIPI Data Lane Transmission Order for 4 Lane Mode

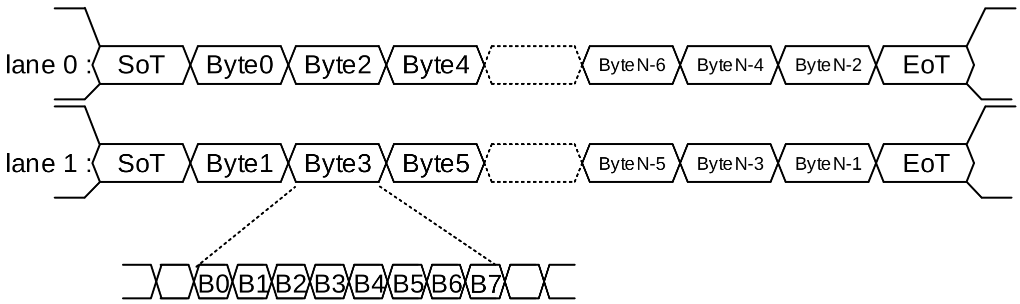


Fig 15. MIPI Data Lane Transmission Order for 2 Lane Mode

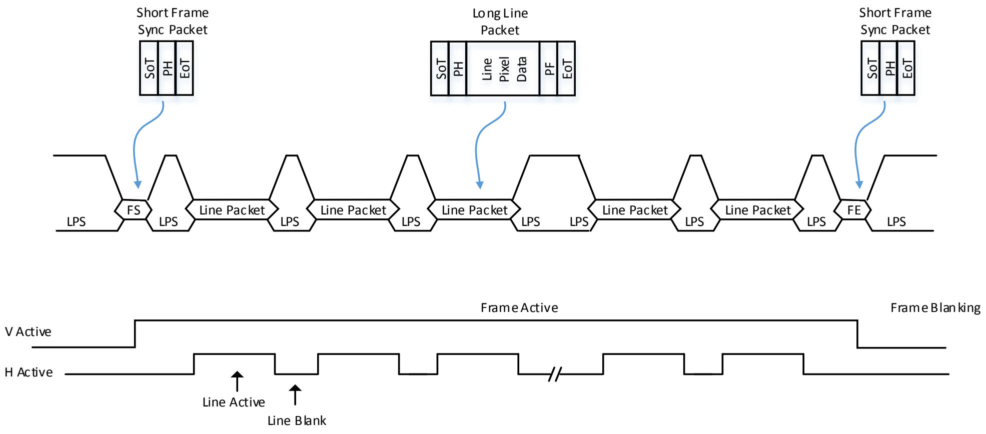


Fig 16. MIPI Low Power Protocol

PI5008 supports multi-channel MIPI Rx interface up to 4 Channels through line concatenated, line interleaved and virtual channel ID mode.

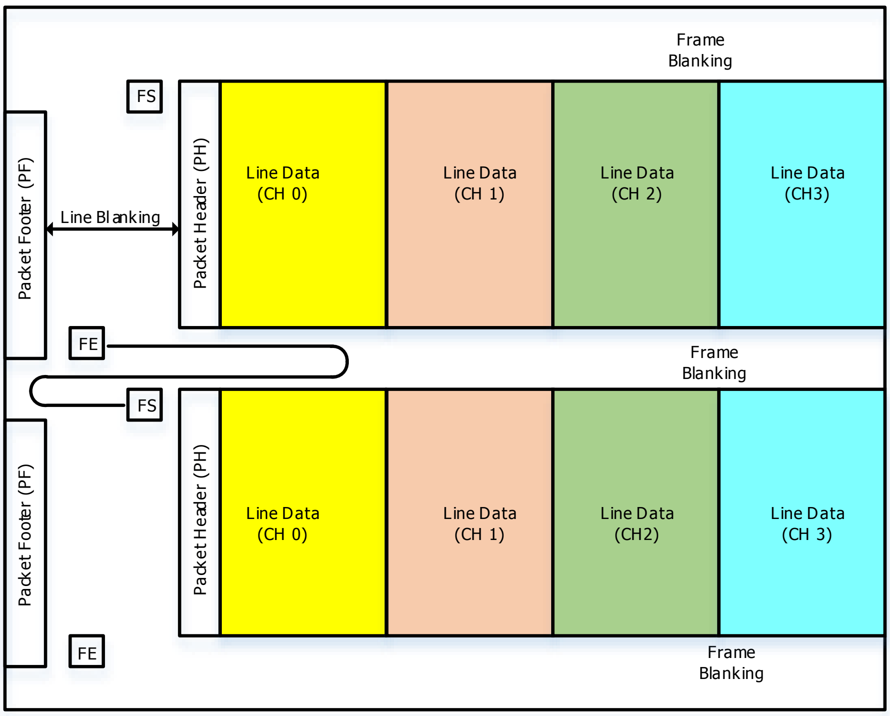


Fig 17. Line Concatenated Mode for 4 Channel MIPI Rx Interface

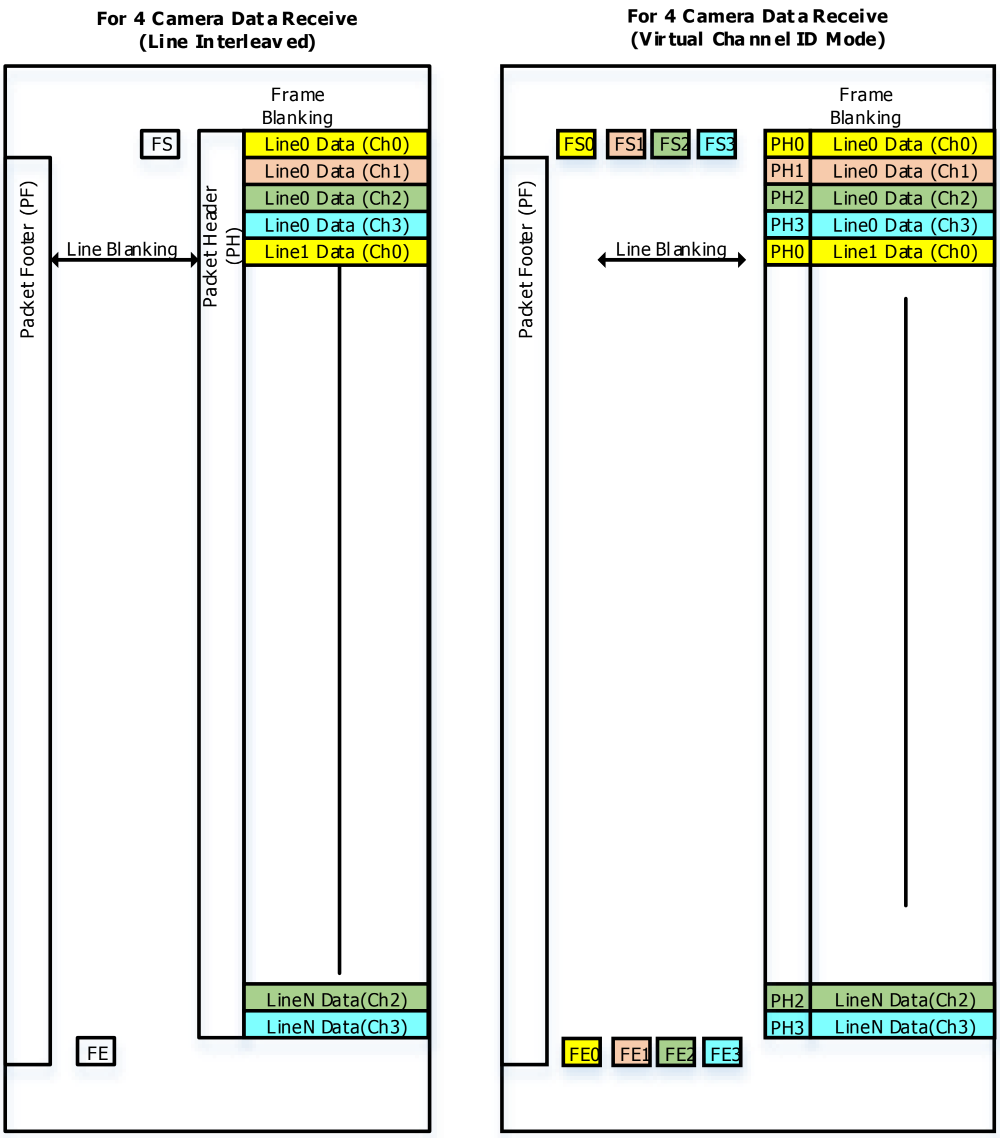


Fig 18. Line Interleaved and Virtual Channel ID Mode for 4 Channel MIPI Rx Interface

3.3.3. Diagnose Interface

PI5008 supports diagnose detection function such as video input loss detection, video input format detection, video input freeze detection and video output freeze detection for svm/quad split output.

3.4. ISP (Image Signal Processor)

The ISP processes bayer image data from external image sensor, and improves the overall image quality. It consists of several functional blocks, and each block corrects and enhances the image data in terms of dynamic range, resolution, color and sharpness. PI5008 includes four ISP to handle four image sensor inputs simultaneously and each ISP can process a combined and compressed raw data from HDR (High Dynamic Range) sensor which is generally used for automotive application. Functional block diagram for ISP is as the following figure.

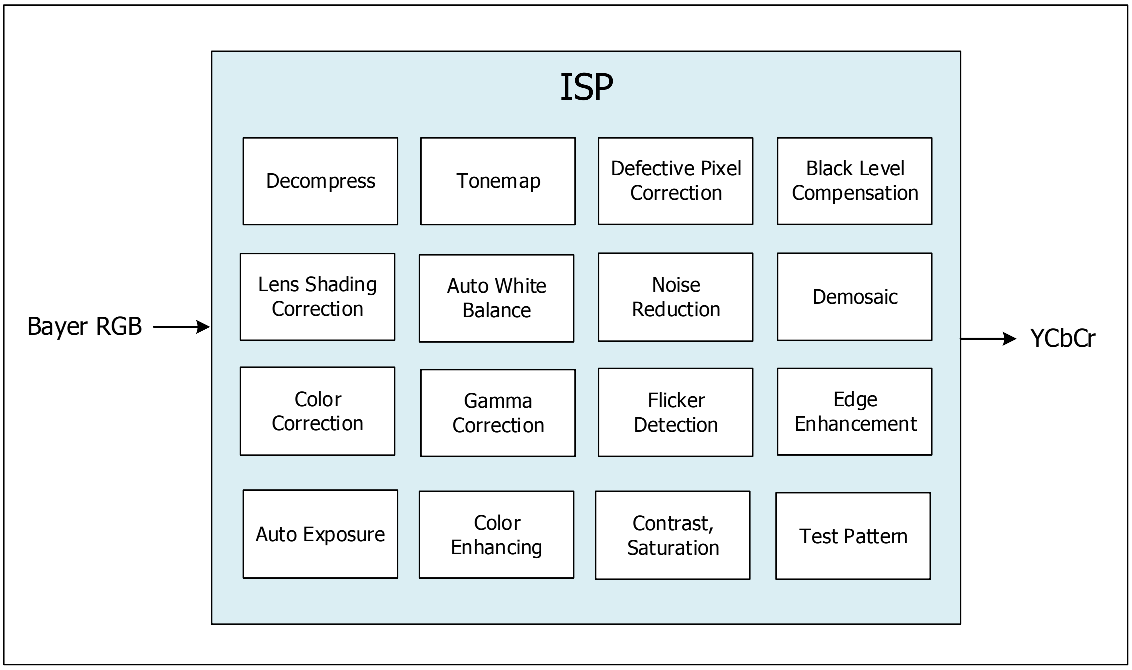


Fig 19. Image Signal Processing Block

The ISP block receives bayer format data through MIPI or parallel interface port. Normally, SDR (Standard Dynamic Range) sensors outputs 10-bit (60db) bayer format data to ISP and HDR sensors outputs 16-bit (96db), 20-bit (120db) combined, uncompressed format or 12-bit combined, compressed format. Since the parallel port supports only up to 12-bit interface, in case of HDR combined, uncompressed format, MIPI interface should be utilized. PI5008 does not support combine function of HDR sensor which combines several different exposures images of the same scene. The combining of multiple exposure images must be performed on the external sensor chip.

Input bayer data is converted into the RGB data by color interpolation (demosaic) process. Before RGB conversion, correcting the defective pixel and lens shading, balancing the color, optimizing the exposure and removing the noise functions are performed as a preprocessing. In case of HDR sensor, tonemap process is performed on this stage to get the high dynamic range image. PI5008 supports local tonemap algorithm which helps bring out details by increasing contrast in local areas. RGB data is converted to YUV data after correcting the color and gamma. The ISP more improves the sharpness and color in YUV domain. After globally adjusting contrast, saturation and brightness again, ISP processed image is created in the YUV format.

Most part of the ISP function is implemented in dedicated hardware cores, but some of them such as tonemap, auto exposure and white balance demands additional software processing. Since four ISP processing requires quite a lot of software resources, PI5008 has two built-in CPU cores, and secondary CPU is recommended to use for ISP processing.

The ISP output image quality is mostly dependent on tuning, and since the preferred images are different for each user, tuning process is important during the full SVM system development.
To facilitate tuning of parameters, specific ISP tuning tool is generally used. PI5008 proprietary tuning tool uses I^{2}C slave port to control the registers in ISP.

Main features of ISP are as below:

- ✓ 8/10/12-bit bayer raw input
  - 8/10-bit non-HDR raw (MIPI/parallel)
  - 12-bit compressed combined raw (MIPI/parallel)
  - Up to 20-bit uncompressed combined raw (MIPI only)
- ✓ Max. FHD 1920x1080 30fps, HD 1280x720 60fps
- ✓ Supports global and local tone map algorithm
- ✓ Auto exposure and white balance
- ✓ High performance spatial Denoising filter (2DNR)
- ✓ Color interpolation (Demosaicking)
- ✓ Defect pixel correction
- ✓ Lens shading correction
- ✓ Color correction
- ✓ Gamma correction
- ✓ Color correction
- ✓ Edge and sharpness enhancement
- ✓ Color Enhancing with hue, saturation control

3.5. SVM (Surround View Monitoring)

3.5.1. Overview

The SVM (Surround View Monitoring) unit receives up to four camera inputs, performs warping process, and generates the seamlessly stitched image (surround view) through blending. Simplified SVM block diagram is as figure below.

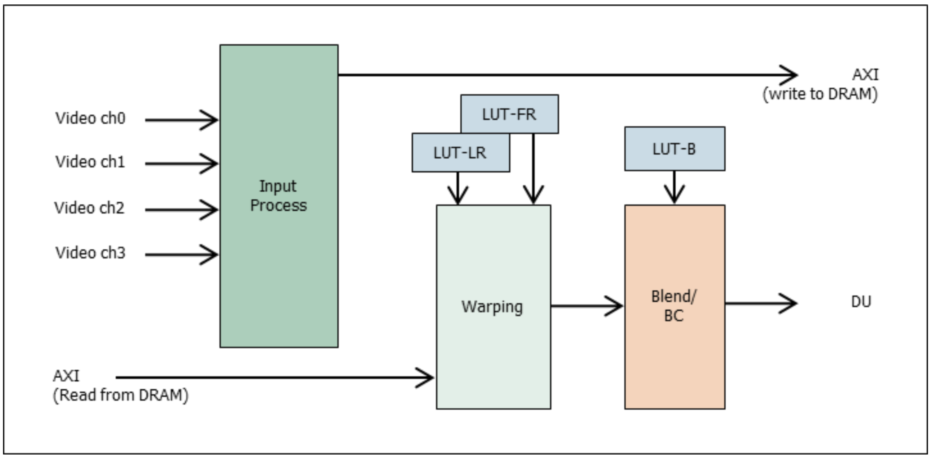


Fig 20. SVM block diagram

Four video sources are selectable from MIPI, ISP, parallel or analog HD, and stored to external DDR DRAM first before being used to create surround view. Actually, current incoming video data is used for a surround view of frame after next, which incurs maximum 3 frames of latency from video input to display out. The main SVM operation consists of two steps in sequence. During the first step, the warping process is performed using the two LUTs. LUT-FR for front and rear images and LUT-LR for left and right images are required for this process. Two warping views (front/rear, left/right) are blended together in second step. The brightness control to reduce the brightness/color disparity between images is also performed using LUT (LUT-B) at this stage. The blended surround view image is optionally overlaid with car image, and goes out to the DU block for final display. Main features of SVM are as below.

- ✓ Real-time performance
  - Full HD (1920x1080) 30fps,
  - HD960p (1280x960) 30fps
  - HD720p (1280x720) 30/60fps
  - SD (720x480, 720x576, 960x480, 860x576) 60fps
- ✓ Interlace and progressive conversion
- ✓ Antialiasing filter for input image
- ✓ Brightness control

- ✓ Dynamic blending
- ✓ LUT morphing
- ✓ Supports overlay function(YUV422 format only)

In PI5008, the clock frequency of SVM block should be set to 148.5MHz only and the clock of DDR controller should be set into 250MHz for proper operation.

3.5.2. Processing Flow

As shown in figure below, generally four cameras are installed around the vehicle for surround view monitoring. The front and rear images are processed by LUT-FR and the left and right images are processed by the other LUT-LR. Single LUT for two camera processing reduces the total number of LUTs required. The following figure shows the process of warping four wide angle cameras using two LUT.

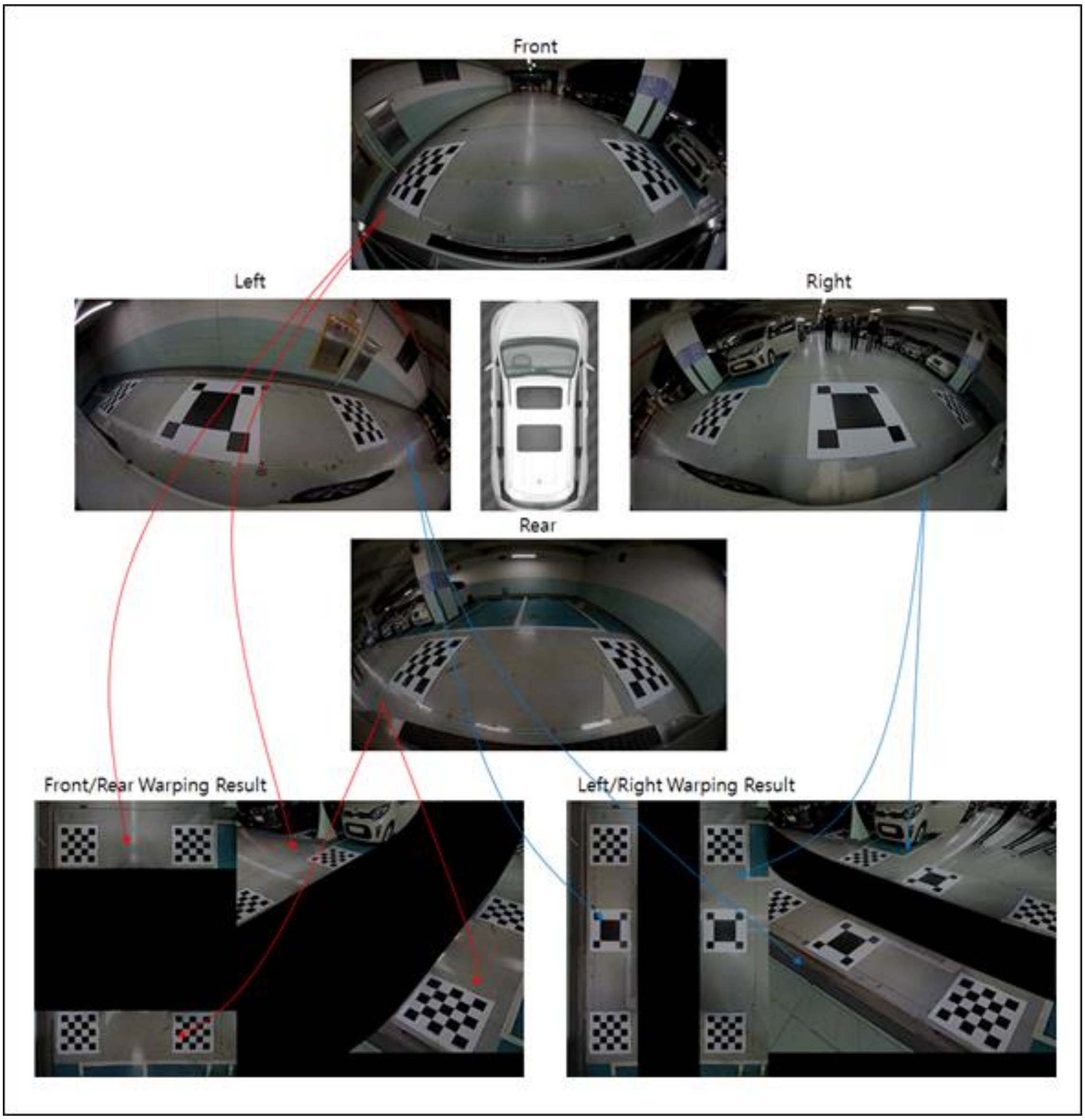


Fig 21. Warping examples

The two warping images (warping result of front/rear and left/right) generated in the above process are blended together through the alpha LUT (LUT-B), and corrected by the information of brightness and color disparity. The 2D/3D car image can be optionally overlaid thereon to generate the final output image, as shown below.

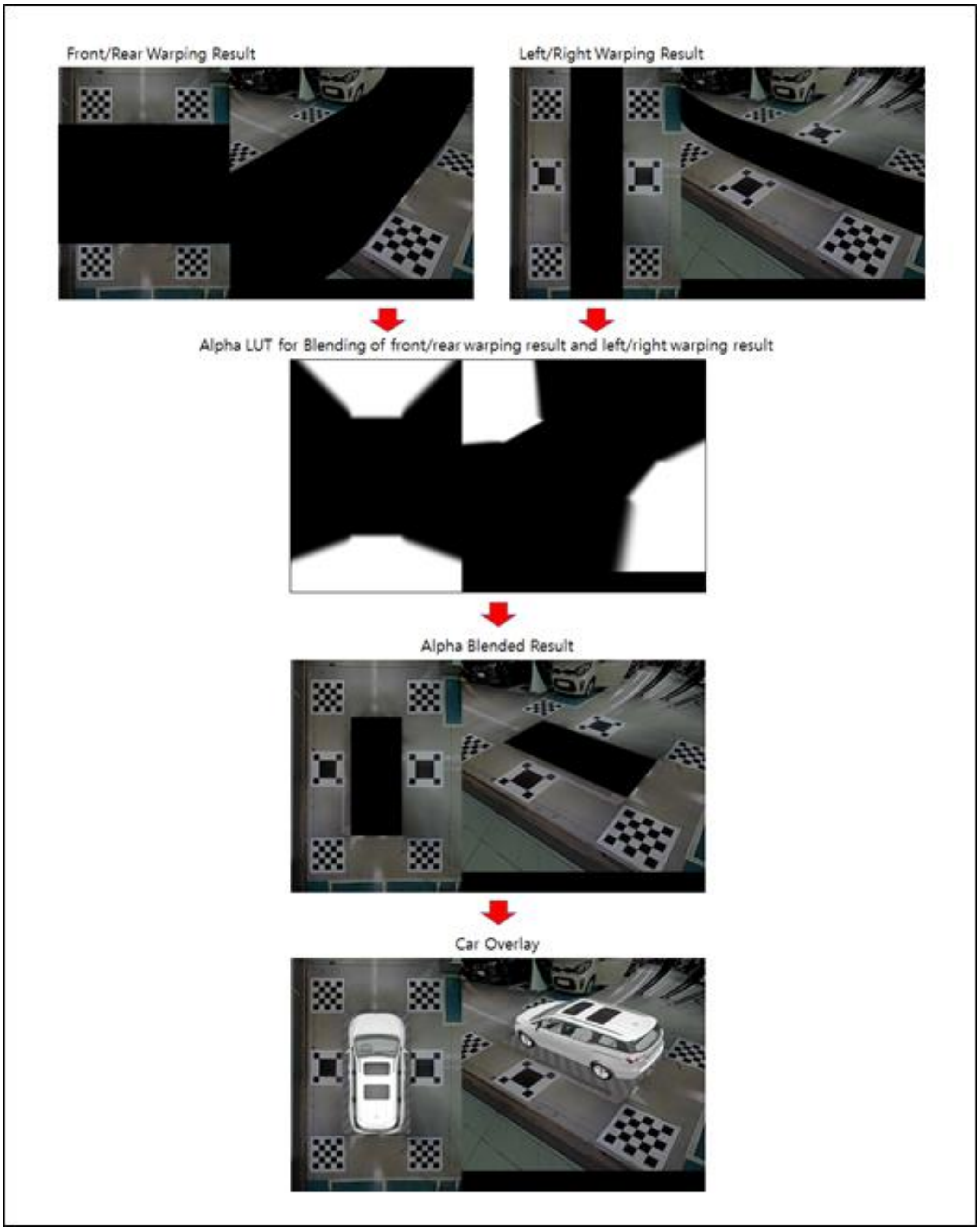


Fig 22. Blending and Car Overlay

3.5.3. Brightness Control

The cameras for the surround view monitoring are installed in different position each other, so there may be some differences in brightness and color. With this problem, a noticeable difference may appear at the stitching boundary, resulting in an unnatural view. As a solution to this problem, SVM provides adjusting function for brightness and color based on color information extracted from the previous frame as shown in the following figure. This makes it possible to generate more natural images by matching the difference in brightness and color.

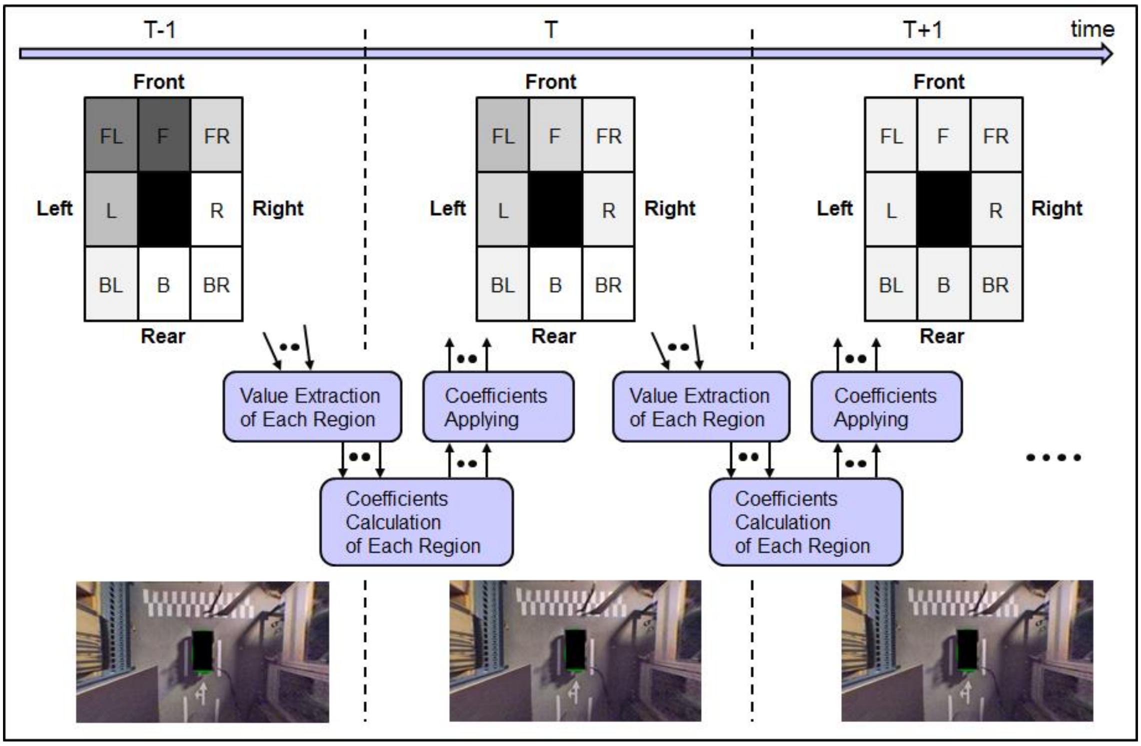


Fig 23. Brightness Control Flow

3.5.4. Dynamic Blending

Since the SVM unit generates the stitching view from multiple cameras, there may be some blind spot between them. When a fast-moving object approaches the vehicle, the SVM generated view may have a momentary blind spot, or a moving object may appear distorted as like ghost. To overcome this problem, SVM can change blending scheme dynamically according to the moving object as figure below. In order to use dynamic blending function, SVM have to get some object moving information from the CPU. Object detection function can be implemented with software, and optical flow accelerator included in VPU may be helped. Object moving information between frames changes the area blended in SVM unit at detecting approaching objects.

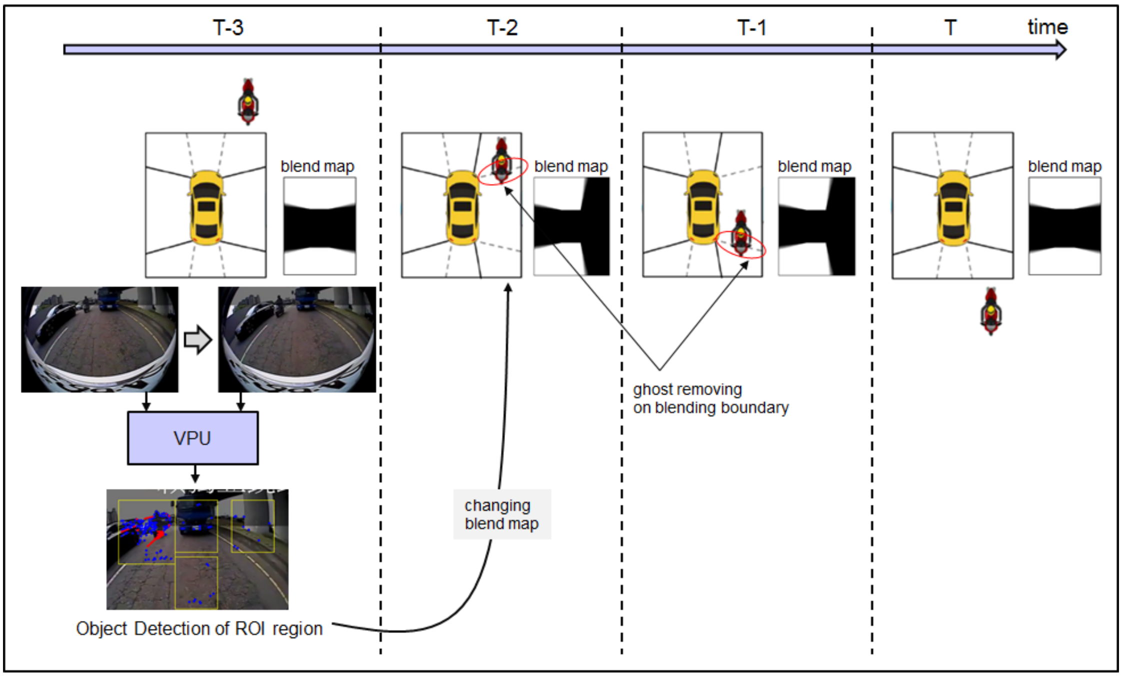


Fig 24. Dynamic Blending Process

3.5.5. Morphing

The SVM unit uses the LUT for warping and blending. According to user application, the SVM system may have several view modes and it needs several LUTs (LUT-FR, LUT-LR and LUT-B per a view mode). As shown in the figure below, a lot of LUTs may be required for supporting view transformation with angle changes, and it may incur storage capacity problem when the Flash or DDR DRAM size is not so sufficient. To solve this problem, SVM supports morphing function which interpolates between view LUTs. As an example, in the figure below, LUT0 is a 0 degree view LUT and LUT1 is a 4 degree view LUT. 1, 2, and 3 degrees view LUTs can be generated by morphing function. In this case, only the 1/4 LUT storing capacity is needed for supporting the whole rotation function.

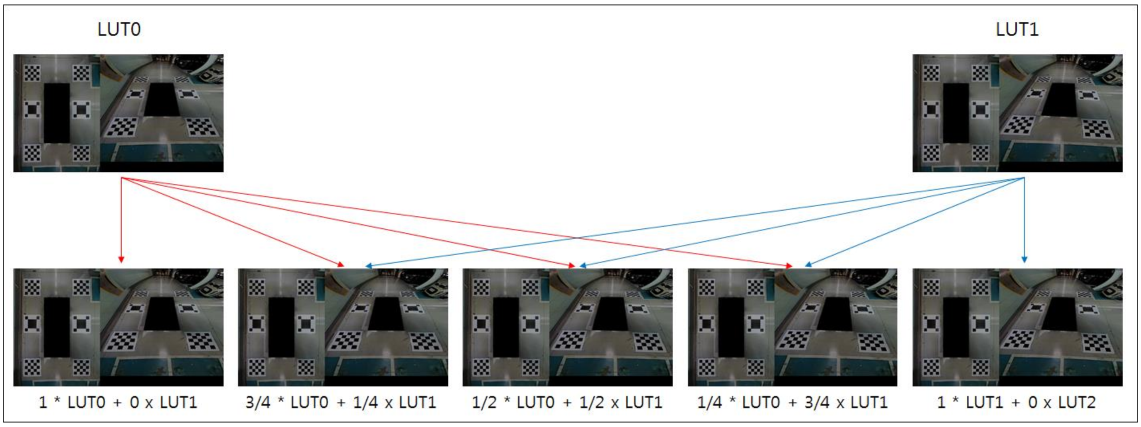


Fig 25. LUT Morphing Results

3.6. VPU (Video Processing Unit)

3.6.1. Overview

The VPU is a hardware accelerator for optical flow and canny edge detector which are basic preprocessing routine used for various automotive video processing algorithms. High quality SVM view needs some ancillary functions such as on-line calibration and object detection for dynamic blending. Optical flow can be applied for those algorithms as preprocessor and it may take very long time if only software approach is applied. Canny edge detector extracts boundary and edge lines of object and it may be used to detect traffic lanes. VPU input source can be direct input from external cameras (through MIPI, ISP, Parallel or Analog HD), Quad output which merges multiple input to a quad view, DDR DRAM to which user can load target source images, or SVM output. Besides optical flow and canny edge detection, VPU includes fast 2D DMA and RLE encoder with DMA for user application convenience. Main feature of VPU is as below:

- ✓ Optical flow
  - FAST/BRIEF algorithm
  - Hamming distance comparing acceleration
- ✓ Canny edge detector
- ✓ High performance 2D DMA
- ✓ RLE encoder for overlay data generation

3.6.2. Optical flow

The optical flow function finds the feature points of incoming video on-the-fly way. Based on the feature point information from 2 frames, feature movements are calculated as optical flow. The main optical flow implemented in VPU is based on FAST/BRIEF that is the one of the sparse optical flow algorithms. The VPU hardware accelerator also covers hamming distance calculation between feature descriptors. Main feature of hardware implemented optical flow engine is as below:

- ✓ 16 zone based feature point extraction
- ✓ Down scaler included before FAST/BRIEF
- ✓ ROI (Region Of Interest) configurable
- ✓ FAST(Features from Accelerated Segment Test) corner detection
- ✓ BRIEF(Binary Robust Independent Elementary Features) descriptor generation
- ✓ Input video image pre-filtering before FAST/BRIEF
- ✓ Max 1080p
- ✓ 8-bit Luma processing only

3.6.2.1. Pre-processing for FAST/BRIEF

The input source for optical flow is selectable from one of direct camera video channel 0~3, SVM output, Quad output and loaded data in external DDR DRAM. After multiplexing of all sources, user can downsize input by scaler. To exclude unneeded feature point, several regions of interest (ROIs) can be set by program up to 16 regions. The size and start position of each ROI is basically arbitrary and can be overlapped in an image as figure below. ROI zone 0 has the highest priority when the region is overlapped and higher zone number, lower priority. The minimum size of each ROI is eight by eight and its maximum is image size itself. ROI size can be set to multiple of eight units(x: pixel, y: line) in the horizontal and vertical direction.

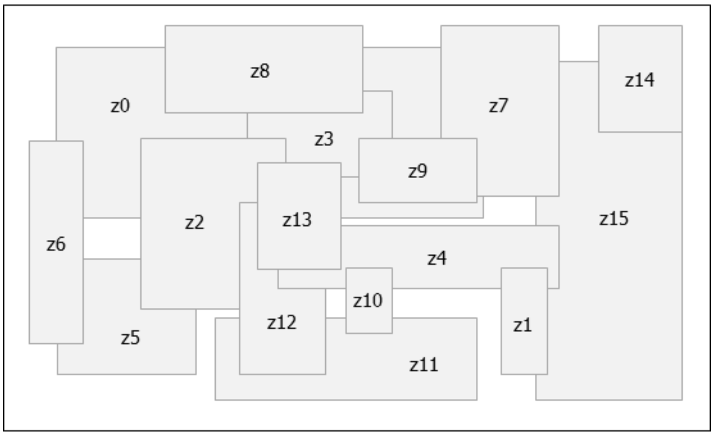


Fig 26. Example for 16 ROI allocations

After ROI zone processing, simple blur filter can be applied to reduce noise that may lead to increase in erroneous feature point. This blur filter has 5x3 size (in x, y order) kernel and its coefficients can be configurable independently for FAST and BRIEF each by program. Full processing flow for FAST/BRIEF is as figure below.

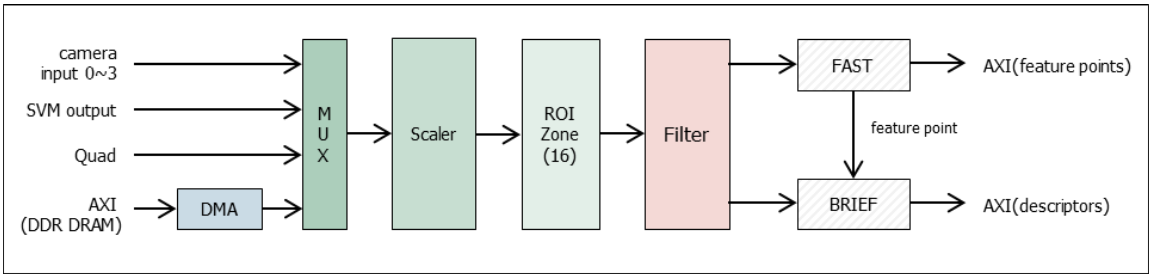


Fig 27. Optical Flow Processing Flow

3.6.2.2. FAST

The FAST algorithm is based on 7x7 window, which corresponds to 16-point continuous circular positions. When N (default is 9 and generally called as FAST-9) continuous pixels are brighter or darker than the center pixel, that center position is selected as a feature point candidate. One problem with FAST feature point is that if center point is detected as a feature point, then the neighboring points adjacent to center point are very likely detected as feature points again. To solve this problem, FAST algorithm applies an additional post processing step called non-maximal suppression. As the non-maximal suppression processing, feature point candidates are compared among 3x3 score window. When the score of center pixel is bigger than the surrounding 8 scores within 3x3 window, then the center position is selected as a real feature point. The selected feature point position is stored to DDR DRAM automatically. The total number of feature point may vary greatly frame by frame, but the maximum number of feature point to be stored can be limited by program.

3.6.2.3. BRIEF

FAST detects feature point, and BRIEF creates a descriptor for that feature point. Based on the predefined LUT containing information about the 128 positions in the 24x12 pixel window centered on feature point, BRIEF generates 128-bit descriptor per feature point with the total 128 position information (1-bit descriptor per a position). 128-bit descriptors for feature points identified by FAST block are automatically stored to external DDR DRAM. BRIEF has four user selectable predefined LUT.

3.6.2.4. Hamming Distance Comparison

To calculate the optical flow, it is needed to find out whether the feature point is moved and how much the moving distance is. It is determined by hamming distance of two descriptors between feature points. Comparing all descriptors by using software only requires a lot of time. VPU supports hamming distance acceleration with DMA base, which automatically loads descriptors and feature positions from DDR DRAM, and compares them using hamming distances calculation.

3.6.3. Canny Edge Detector

The canny edge detector extracts edge information on the fly from input video and stores the edge data to DDR DRAM. The canny edge detector can accept various input source as like optical flow does. The edge result is stored to DDR DRAM through DMA and it has 1-bit per pixel data. The figure below shows the input image and the result of canny edge detector.

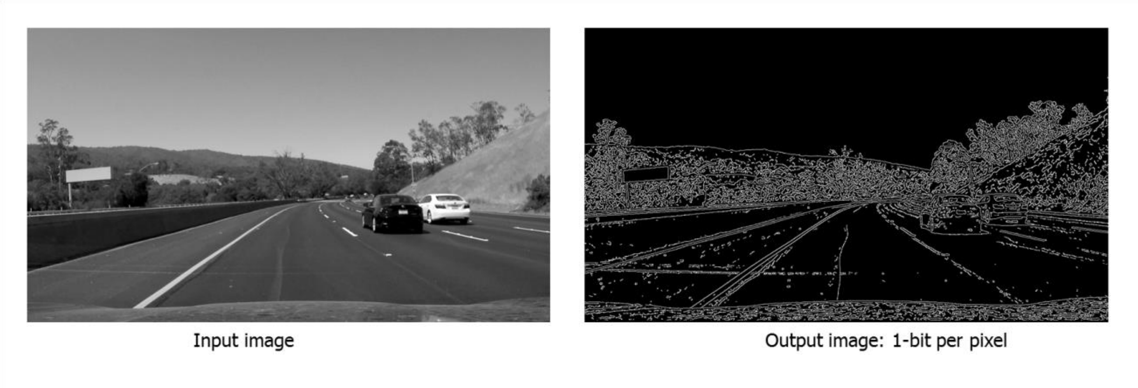


Fig 28. Input and Output of Canny Edge Detector

3.6.3.1. ROI and scaling

In some application, if only partial part of images are interested rather than the entire image, extracting edge data within the ROI can be more efficient for saving memory space and improving application performance. The canny edge detector supports ROI setting and stores only the edge results of the ROI. The ROI area can be controlled in line units.

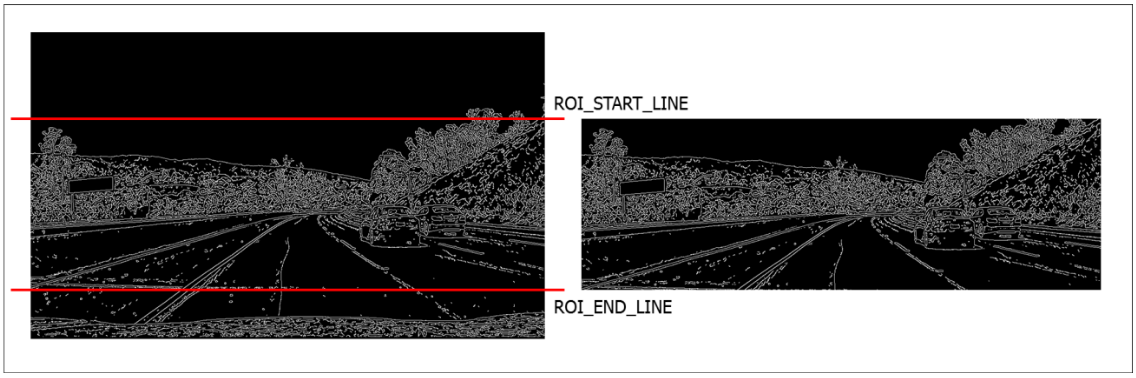


Fig 29. ROI area

The canny edge detector also supports down-scaling in both the horizontal and vertical directions. The down-scale ratio is fixed to 3 types which are 1/2 horizontal, 1/2 vertical and 1/2 both direction down-scaling.

3.6.3.2. Thresholding

The canny edge detector supports two modes for hysteresis thresholding. The one is a method using gradient magnitude after the Sobel filtering, in which two threshold values for strong and weak edge are defined by control registers. The other way is specifying the ratio for two threshold values from magnitude histogram. In the second case, the threshold value obtained from the previous frame is applied to the current frame.

3.7. DU (Display Unit)

3.7.1. Overview

The DU controls a main display output of the chip. It may selectively generate a SVM output, four video input directly or quad output with overlay data. The video data which comes into the DU is blended with the five overlay layers and each layer supports the RLE (Run Length Encoder) or BMP (Bitmap) mode respectively. These RLE and BMP format data for the overlay are stored into the external DDR DRAM during the boot sequence. The DU output is transferred to the outside in analog and digital format. In case of analog, conventional SD and HD formats are supported. Digital output can be formatted in various ways such as YUV, RGB or bayer. The functional block diagram for DU is as figure below.

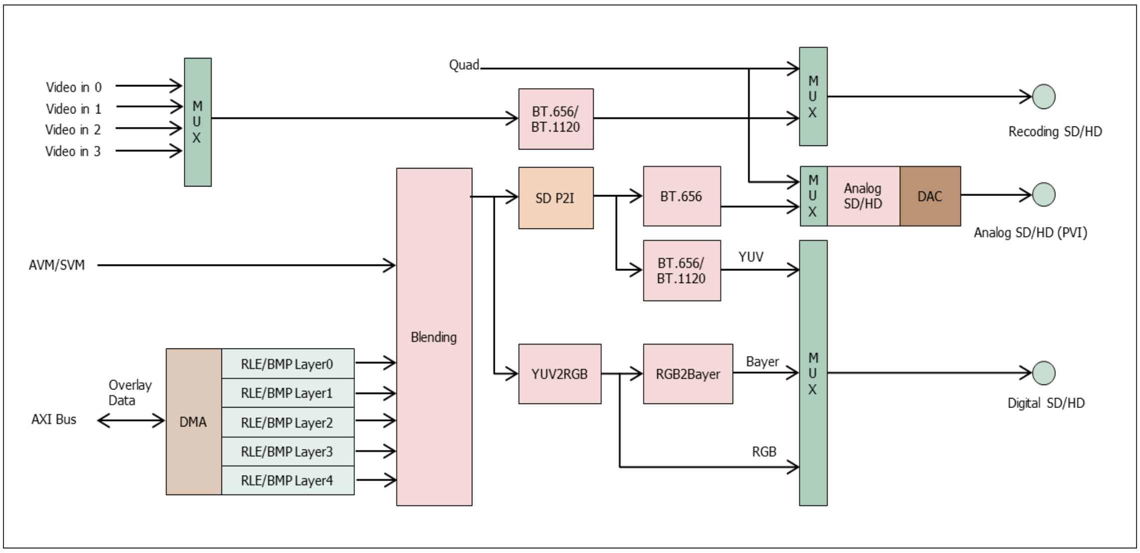


Fig 30. DU Block Diagram

The main features of DU are as below:

- ✓ OSD (On Screen Display)
  - 5 overlay layers,
  - 8/16/24/32-bit per overlay data format
  - RLE or BMP mode
- ✓ Video output
  - Analog: Multi-Standard analog HD, SD(NTSC/PAL)
    - > DAC: 10-bit @148.5MHz imbedded
  - Digital: YUV/RGB/Bayer
    - > BT.1120 8/16-bit, BT.656, 709 YUV conversion

> RGB 565/666/888

- Recoding output: Digital YUV only
  > Digital YUV only: BT. 8-bit 2 Channels, BT1120 16-bit 1 Channel

3.7.2. Overlay

The DU performs overlay function with five layers (layer0~layer4), in which layer0 is the lowest and layer4 is the highest layer. Each layer puts the overlay data on an incoming video in RGB format, and allows up to four regions defined as 'area' to overlay independently. Four 'area' per a layer can't be overlapped, but the 'area' between layers can be overlapped as figure below.

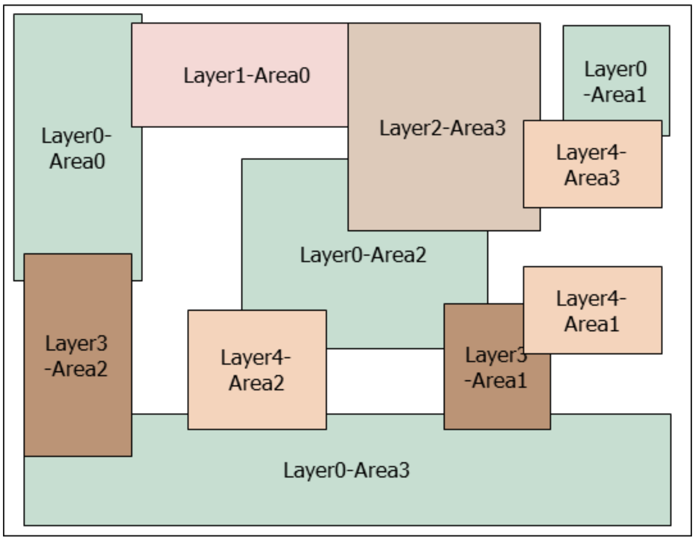


Fig 31. Layer/Area Allocation Example

Each layer supports RLE or BMP overlay mode, and 8, 16, 24, 32-bit overlay data per a pixel. Among the all layers, layer0, layer1 and layer2 supports only 8-bit LUT mode for RLE and BMP pixel, and 8, 16, 24 and 32-bit bitmap mode per a pixel format are applicable to layer3, layer4 only.

Table 9. Overlay Data Format

Overlay Data format	Description
8-bit(LUT Mode)	256 LUT, Each LUT is 32-bit and consisted as below. [31:24]: Alpha, [23:16]: R, [15:8]: G, [7:0]: B
16-bit	Supports 4:4:4:4 and 5:6:5 mode. 4:4:4:4 Mode:

	R, G, B and Alpha are 4-bit each as below. [15:12]: R, [11:8]: G, [7:4]: B, [3:0]: Alpha 5:6:5 Mode: R, G and B are 5, 6, 5-bit each as below. One Alpha value which is set by specific 8-bit register is applied to all pixels. [15:11]: R, [10:5]: G, [4:0]: B
24-bit	R, G and B are 8-bit each. One Alpha value which is set by specific 8-bit register is applied to all pixels.
32-bit	R, G, B and Alpha are all 8-bit each as below. [31:24]: Alpha, [23:16]: R, [15:8]: G, [7:0]: B In this bit mode, one 'area' maximum horizontal size is limited to 1/2 line. As an example, in case of HD display, maximum horizontal size of 'area' is limited to 640-pixel(1280/2).

3.7.2.1. RLE Mode

RLE overlay data is the 8-bit bitmap data compressed by RLE algorithm. It is used to save the memory size needed to store the overlay data. RLE compressed data is decompressed in RLE layer and restored to original bitmap data with which RLE layer performs overlay using the RGB and Alpha value stored in LUT.

3.7.2.2. BMP Mode

BMP Layer performs overlay using uncompressed bitmap data. It can selectively use 8, 16, 24 and 32-bit LUT overlay data format. The overlay data in RGB format is converted to YUV data to blend with incoming video into DU. All conversion coefficients for YUV are fully programmable.

3.7.3. Video Output

PI5008 contains the main display and record path for video output. The main display path output is composed of digital video and analog video output mode. The record path output is comprised of video input bypass mode and quad split mode.

3.7.3.1. Main Display Path

In case of analog video output mode, PI5008 supports multi-standard analog HD/SD formats which are widely used in the industry and a 10-bit, 148.5MHz DAC is imbedded for up to full HD analog output. If the analog output resolution is the same with digital output, analog video can go out simultaneously with the digital video output for display path. In case of digital video output mode, YUV, RGB and bayer format is available. Since PI5008 includes programmable timing generator in display path, arbitrary output resolution (e.g. 800x480, 1024x600) is configurable if it is smaller than 2047 in the horizontal (pixel) and vertical (line) both direction. However, standard formats listed in the following table are strongly recommended to use.

Table 10. Video Output Format for Main Display Path

Video Format	Resolution	Pixel Clock(MHz)	Comment
SD720H50	720x288@50Hz	27	BT.601
SD720H60	720x240@60Hz	27	BT.601
SD960H50	960x288@50Hz	36	BT.1302
SD960H60	960x240@60Hz	36	BT.1302
720P25	1280x720@25Hz	37.125/74.25	BT.709
720P30	1280x720@30Hz	37.125/74.25	BT.709
720P50	1280x720@50Hz	74.25	BT.709
720P60	1280x720@60Hz	74.25	BT.709
960P25	1280x960@25Hz	74.25	Non Standard
960P30	1280x960@30Hz	74.25	Non Standard
1080P25	1920x1080@25Hz	74.25	BT.709
1080P30	1920x1080@30Hz	74.25	BT.709

3.7.3.1.1. Digital Video Output Mode

The ITU-BT.601, BT.1120 8/16-bit interfaces including separate or embedded sync mode are configurable for YUV format digital output as shown in the following figure. When the RGB mode is used, 8-bit for each RGB channels are all assigned to dedicated pins so that various RGB output formats such as RGB565, RGB666 and RGB888 are supported.

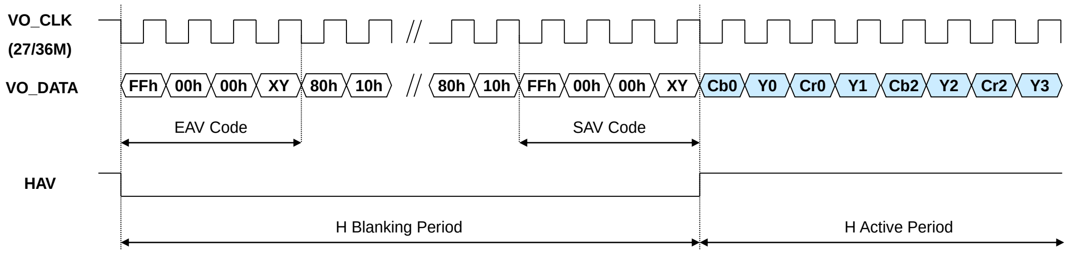


Fig 32. Timing Diagram of 8bit ITU-R BT.656/1302 Format

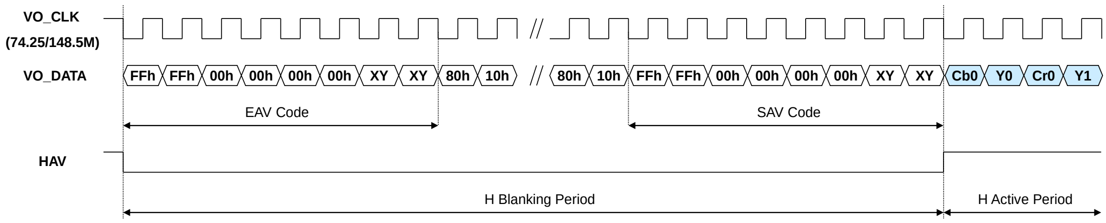


Fig 33. Timing Diagram of 8bit ITU-R BT.1120 Format

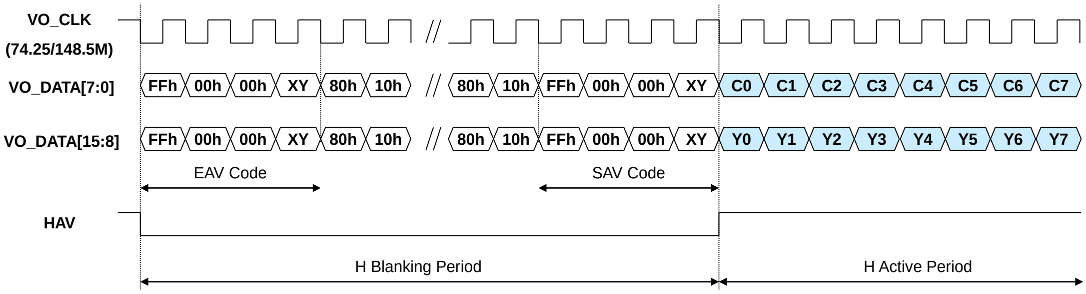


Fig 34. Timing Diagram of 16bit ITU-R BT.1120 Format

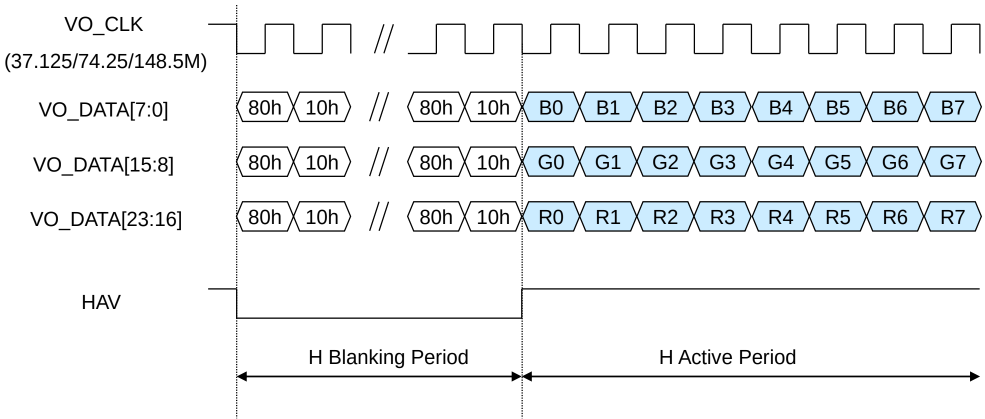


Fig 35. Timing Diagram of 24bit RGB with External Sync Format

The Bayer type output is usable in case that output video needed to be interfaced with UVC chips outside of PI5008. There are four types of bayer format: RGGB, BGGR, GRBG and GBRG. These four output formats are selectable by register control. The pin assignments for each digital output mode are shown in the following table.

Table 11. Pin Configuration for Display Output

Pin Name	8/10 bit Mode	16 bit Mode	24 bit Mode
VO_DATA[0]	YC_MUX[0] / Bayer[0]	C Data[0]	B Data[0]
VO_DATA[1]	YC_MUX[1] / Bayer[1]	C Data[1]	B Data[1]
VO_DATA[2]	YC_MUX[2] / Bayer[2]	C Data[2]	B Data[2]
VO_DATA[3]	YC_MUX[3] / Bayer[3]	C Data[3]	B Data[3]
VO_DATA[4]	YC_MUX[4] / Bayer[4]	C Data[4]	B Data[4]
VO_DATA[5]	YC_MUX[5] / Bayer[5]	C Data[5]	B Data[5]
VO_DATA[6]	YC_MUX[6] / Bayer[6]	C Data[6]	B Data[6]
VO_DATA[7]	YC_MUX[7] / Bayer[7]	C Data[7]	B Data[7]
VO_DATA[8]	Bayer[8]	Y Data[0]	G Data[0]
VO_DATA[9]	Bayer[9]	Y Data[1]	G Data[1]
VO_DATA[10]		Y Data[2]	G Data[2]
VO_DATA[11]		Y Data[3]	G Data[3]
VO_DATA[12]		Y Data[4]	G Data[4]
VO_DATA[13]		Y Data[5]	G Data[5]
VO_DATA[14]		Y Data[6]	G Data[6]
VO_DATA[15]		Y Data[7]	G Data[7]
VO_DATA[16]			R Data[0]
VO_DATA[17]			R Data[1]
VO_DATA[18]			R Data[2]
VO_DATA[19]			R Data[3]
VO_DATA[20]			R Data[4]
VO_DATA[21]			R Data[5]
VO_DATA[22]			R Data[6]
VO_DATA[23]			R Data[7]
VO_HSYNC			HSYNC
VO_VSYNC			VSYNC
VO_EN			FSYNC / OUT_EN

3.7.3.2. Recoding Path

The record path output is composed of video input bypass mode and quad split mode. In case of video input bypass mode, the video output resolution should be same as video input. But in quad split mode, the video output resolution can be defined regardless of video input resolution. The pin configuration for recording output can be controlled as shown in the following table.

Table 12. Pin Configuration for Record Output

Pin	8-bit Mode (2 Port)	16-bit Mode (1 Port)
R0_CLK	Recoding Port 0 Clock	Recoding Clock
R0_DATA[7:0]	Recoding Port 0 Data	Recoding Data[7:0]
R1_CLK	Recoding Port 1 Clock	Reserved
R1_DATA[7:0]	Recoding Port 1 Data	Recoding Data[15:8]

3.7.3.2.1. Video Input Bypass Mode

The video input bypass mode includes one channel output, two channel and four channel multiplexed output mode with SDR (Single Data Rate) or DDR (Dual Data Rate) format as shown in the following figure. For SDR format, the video output data is triggered at clock rising or falling edge, but it is triggered at both clock rising and falling edge for DDR format. The video data from each channel are all synchronous with output clock so that two or four channels can be multiplexed and only one clock can be used for it.

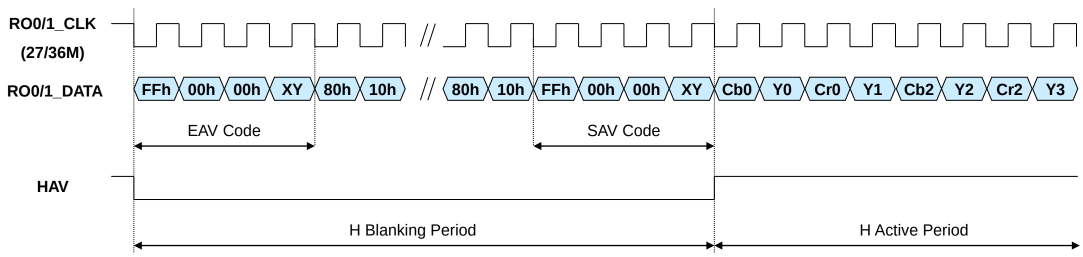


Fig 36. Timing Diagram of One Channel Standard ITU-R BT.656/1302 Format

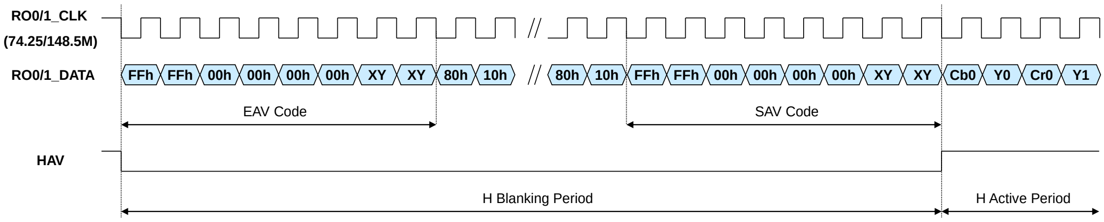


Fig 37. Timing Diagram of One Channel Standard ITU-R BT.1120 Format

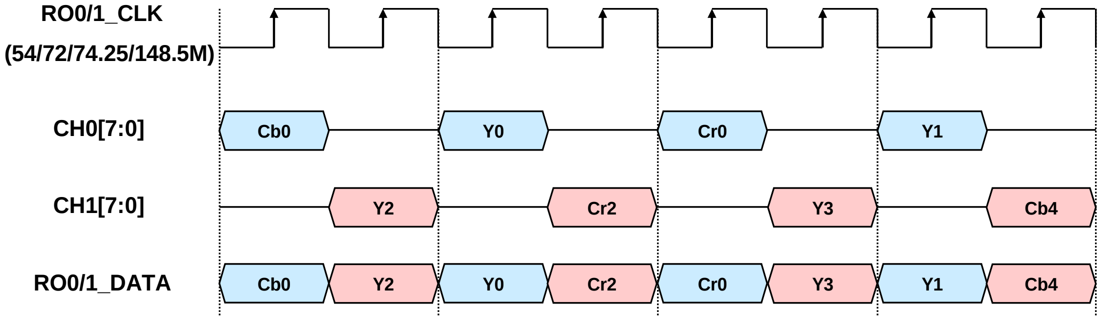


Fig 38. Timing Diagram of Two Channel Multiplexed Format for SDR Mode

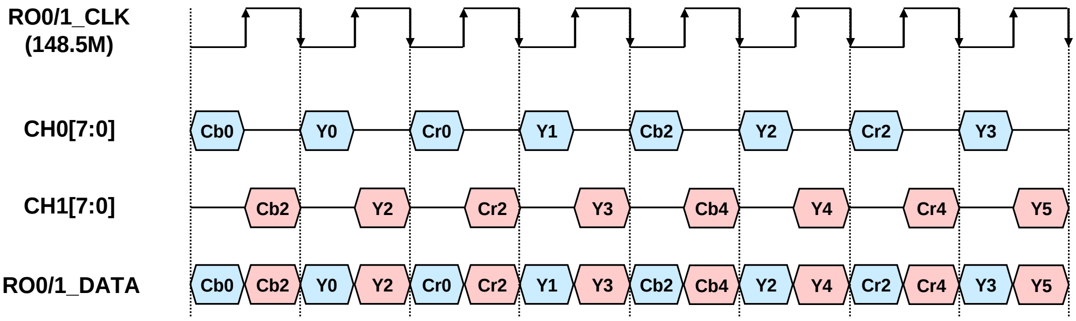


Fig 39. Timing Diagram of Two Channel Multiplexed Format for DDR Mode

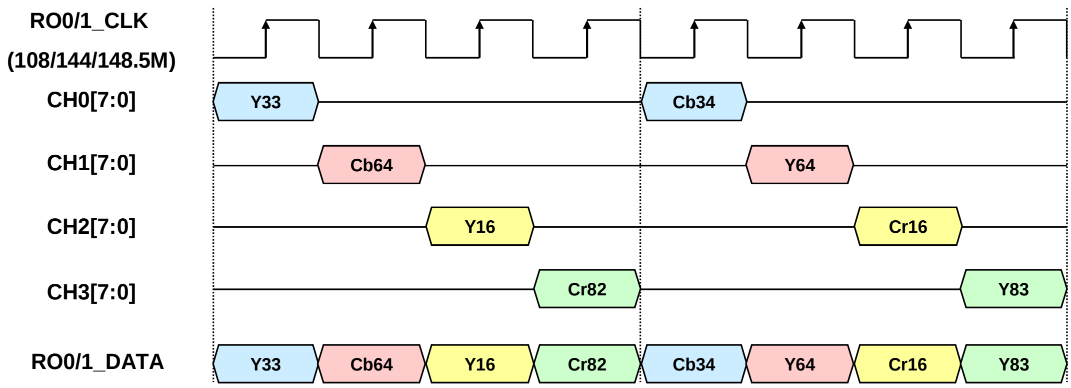


Fig 40. Timing Diagram of Four Channel Multiplexed Format for SDR Mode

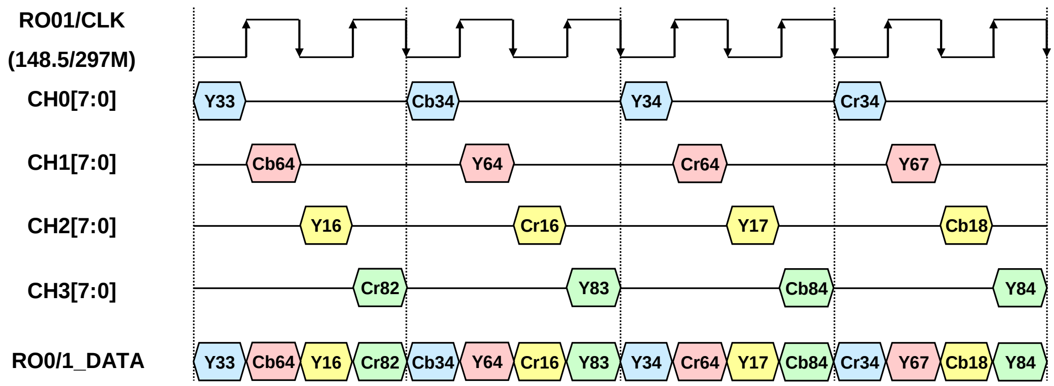


Fig 41. Timing Diagram of Four Channel Multiplexed Format for DDR Mode

In the multi-channel multiplexed mode, the channel ID can be inserted in SAV/EAV LSB code in ITU-R BT.656/1120 format as shown in the following table.

Table 13. Channel ID Format in SAV/EAV Code for Four Channels in ITU-R BT.656 Format

Condition			FVH Value			SAV/EAV Code Sequence for Four CH Format						
Field	V time	H time	F	V	H	1st	2nd	3rd	4th			
									CH1	CH2	CH3	CH4
Even	Blank	EAV	1	1	1	FFh	00h	00h	F0h	F1h	F2h	F3h
		SAV			0				E0h	E1h	E2h	E3h
	Active	EAV		0	1				D0h	D1h	D2h	D3h
		SAV			0				C0h	C1h	C2h	C3h
Odd	Blank	EAV	0	1	1				B0h	B1h	B2h	B3h
		SAV			0				A0h	A1h	A2h	A3h
	Active	EAV		0	1				90h	91h	92h	93h
		SAV			0				80h	81h	82h	83h

Table 14. Channel ID Format in SAV/EAV Code for Four Channels in ITU-R BT.1120 Format

Condition		VH Value		SAV/EAV Code Sequence for Four CH Format						
V time	H time	V	H	1st 2nd	3rd 4th	5th 6th	7th/8th			
							CH1	CH2	CH3	CH4
Blank	EAV	1	1	FFh	00h	00h	B0h	B1h	B2h	B3h
	SAV		0				A0h	A1h	A2h	A3h
Active	EAV	0	1				90h	91h	92h	93h
	SAV		0				80h	81h	82h	83h

3.7.3.2.2. Quad Split Mode

PI5008 supports quad split mode up to Full HD resolution independently of video input resolution as shown in the following figure. The quad output processing supports either quad display or single full display with arbitrary down scaler. The quad video data can be output through digital RO0/RO1_DATA[7:0] pins and analog HD Tx interface. The digital output format of quad display can be 8bit ITU-R BT.656 or 8bit/16bit ITU-R BT1120.

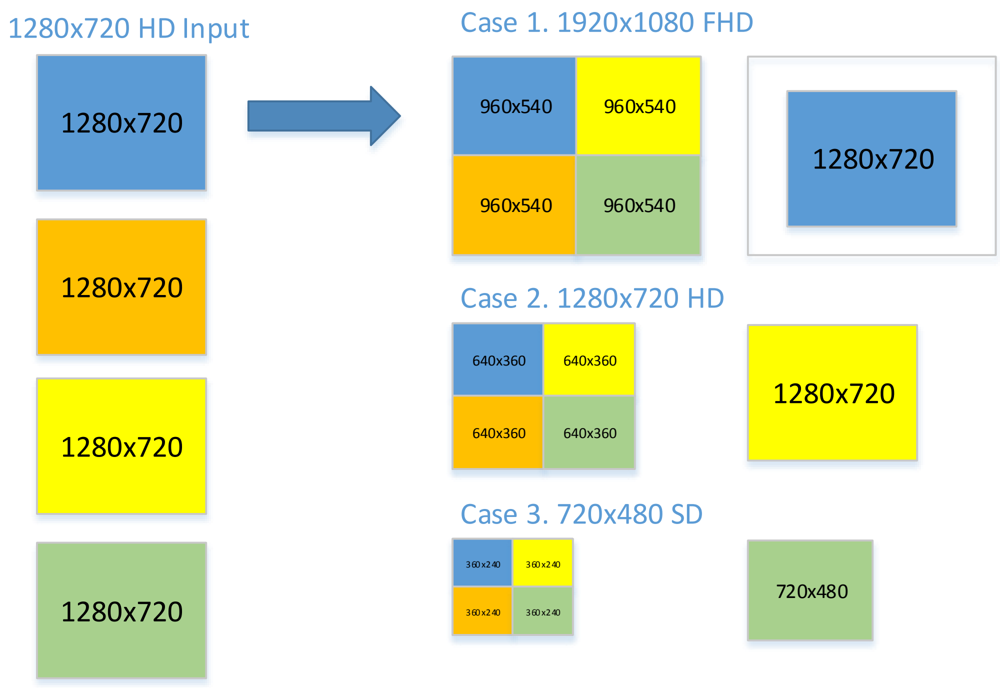


Fig 42. Illustration of Quad Split Output Mode

4. Electrical Characteristics DC Electrical Characteristics

Table 15. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDDO, VDD3AG, VDD3AR, VDD3AT	-0.5		4.6	V	
Voltage for VDDO_DDR	-0.5		2.5	V	
Voltage for VDDI, VDD1AM, VDD1AR, VDD1AP, VDDI_DDRPHY	-0.5		1.68	V	
Voltage for Digital Input Pin	-0.5		3.8	V	
Storage Temperature	-40		125	°C	
Junction Temperature	-40		125	°C	
Peak Temperature on Reflow Soldering			260	°C	15 Sec

NOTE: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition

Table 16. Recommended Operating Conditions for Power and Temperature

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3AG, VDD3AR, VDD3AT	3.0	3.3	3.6	V	
Voltage for VDDO	3.0/1.62	3.3/1.8	3.6/1.98	V	
Voltage for VDDO_DDR	1.71/1.42	1.8/1.5	1.89/1.57	V	
Voltage for VDDI, VDD1AR, VDD1AM, VDD1AP, VDDI_DDRPHY	1.14	1.2	1.26	V	
Ambient Operation Temperature	-40		105	°C	

Note : Power On/Off sequence should keep the following rule

- Apply the power to VDD3AG, VDD3AR, VDD3AT, VDDO, VDDO_DDR and VDDI, VDD1AM, VDD1AR, VDD1AP, VDDI_DDRPHY at the same time
- If it is difficult to apply the power to these pins at the same time, apply the power to VDD3AG, VDD3AR, VDD3AT, VDDO, VDDO_DDR first and to VDDI, VDD1AM, VDD1AR, VDD1AP, VDDI_DDRPHY later
- Cut the power to VDD3AG, VDD3AR, VDD3AT, VDDO, VDDO_DDR and VDDI, VDD1AM, VDD1AR, VDD1AP, VDDI_DDRPHY at the same time
- If it is difficult to cut the power to these pins at the same time, apply the power of VDDI, VDD1AM, VDD1AR, VDD1AP, VDDI_DDRPHY first and to VDD3AG, VDD3AR, VDD3AT,

VDDO, VDDO_DDR later

Table 17. Recommended Operating Conditions for Digital I/O

Parameter	Min	Typ	Max	Unit	Condition
Digital Inputs					
Input High Voltage	2.0		3.6	V	
Input Low Voltage	-0.3		0.8	V	
Input Capacitance		6		pF	
Input Leakage Current			±10	uA	
Digital Output					
Output High Voltage	2.4			V	
Output Low Voltage			0.4	V	
High Level Output Current	9.2	19.6	30.8	mA	Voh = 2.4V
Low Level Output Current	8.0	12.4	15.6	mA	Vol = 0.4V
Tri-state Output Current			±10	uA	
Output Capacitance		6		pF	

Table 18. Supply Current and Power Dissipation for ISP Mode of HD720p

Parameter	ISP Mode (HD720p)			Unit
	Min	Typ	Max	
Supply Current at VDD3AG (3.3V)	2	2	2	mA
Supply Current at VDD3AR (3.3V)	8	10	11	mA
Supply Current at VDD3AT (3.3V)	1	2	2	mA
Supply Current at VDDO (3.3V)	36	38	40	mA
Supply Current at VDDO_DDR 16bit (1.5V)	110	112	120	mA
Supply Current at VDD1AM (1.2V)	9	10	11	mA
Supply Current at VDD1AR (1.2V)	24	27	30	mA
Supply Current at VDD1AP (1.2V)	3	3	3	mA
Supply Current at VDDI_DDRPHY (1.2V)	24	27	30	mA
Supply Current at VDDI (1.2V)	350	400	556	mA
Power Dissipation	812	900	1117	mW

ISP mode is the case using MIPI and ISP.

Table 19. Supply Current and Power Dissipation for ISP Mode of HD960p

Parameter	ISP Mode (HD960p)			Unit
	Min	Typ	Max	
Supply Current at VDD3AG (3.3V)	2	2	2	mA
Supply Current at VDD3AR (3.3V)	8	10	11	mA
Supply Current at VDD3AT (3.3V)	1	2	2	mA
Supply Current at VDDO (3.3V)	73	77	81	mA
Supply Current at VDDO_DDR 16bit (1.5V)	117	120	128	mA
Supply Current at VDD1AM (1.2V)	9	10	11	mA
Supply Current at VDD1AR (1.2V)	24	27	30	mA
Supply Current at VDD1AP (1.2V)	3	3	3	mA
Supply Current at VDDI_DDRPHY (1.2V)	24	27	30	mA
Supply Current at VDDI (1.2V)	495	567	788	mA
Power Dissipation	1118	1241	1543	mW

ISP mode is the case using MIPI and ISP.

4.2. AC Electrical Characteristics

Table 20. Analog Input and Output Parameter

Parameter	Symbol	Min	Typ	Max	Unit
Video ADCs					
Differential Non-Linearity	DLE		± 0.5	± 1	
Integral Non-Linearity	ILE		± 1	± 3	
Signal-to-Noise Ratio	SNR	50	55		dB
Analog Clock PLL					
RMS Jitter	rms_{pll}		8		ps
Duty Cycle	dt_{pll}	45		55	%
Lock Time	t_{lock}		50		us
Crystal Input					
Nominal Frequency	$f_{x\text{-}tal}$		27		MHz
Frequency Deviation	$\Delta f_{x\text{-}tal}$	-50		50	ppm
Duty Cycle	$dt_{x\text{-}tal}$			55	%

Table 21. Serial Host Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Bus free time between STOP and START	t1	1.3			us
Data Hold time	t2	0		0.9	us
Data Setup time	t3	0.1			us
Setup time for a(repeated) START condition	t4	0.6			us
Setup time for a STOP condition	t5	0.6			us
Hold time (repeated) START	t6	0.6			us
Rise time SDA and SCL signal	t7			250	ns
Fall time SDA and SCL signal	t8			250	ns
Capacitive load for each bus line	C_b			400	pF
I^2C Clock frequency	f_{I2C}			400	KHz

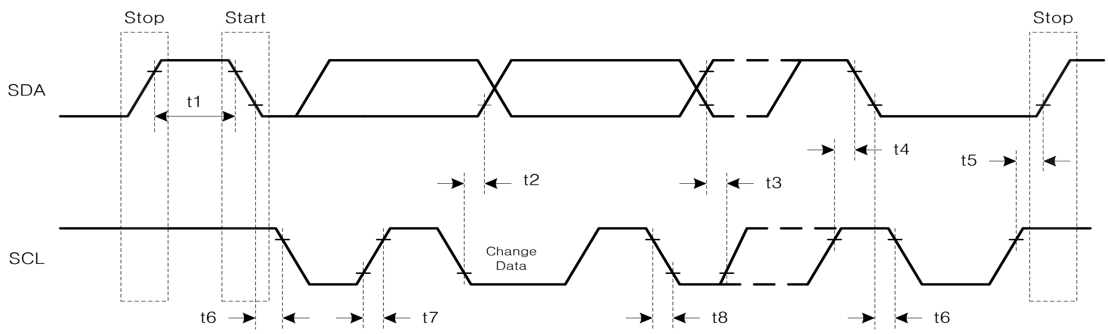


Fig 43. Serial Host Interface Timing Diagram

Table 22. MIPI LP Transmitter Timing

Parameter	Symbol	Min	Typ	Max	Unit
15% ~ 85% rise/fall time	t_{RLP}/t_{FLP}			25	ns
30% ~ 85% rise time in EOT state	t_{REOT}			35	ns
Slew rate	dV/dt_{SR}			120	mV/ns
Load capacitance	C_{LOAD}	0		70	pF
Thevenin output low level	V_{OL}	-50		50	mV
Thevenin output High level	V_{OH}	1.1	1.2	1.3	V
Output Impedance	Z_{OLP}	110			Ohm

Table 23. MIPI HS Transmitter Timing

Parameter	Symbol	Min	Typ	Max	Unit
20% ~ 80% rise/fall time	t_R/t_F	150		0.3UI	ps
HS transmit differential voltage	V_{OD}	140	200	270	mV
HS transmit static common mode voltage	V_{CMTX}	150	200	250	mV
V_{OD} mismatch when output is Differntial-1 or Differntial-0	ΔV_{OD}			10	mV
V_{CMTX} mismatch when output is Differntial-1 or Differntial-0	ΔV_{CMTX}			5	mV
HS output high voltage	V_{OHHS}			360	mV
Single ended output impedance	Z_{OS}	40	50	62.5	Ohm
Single ended output impedance mismatch	ΔZ_{OS}			10	%
Common-level variation for 50~450MHz	ΔV_{CMTX}			25	mV

5. Revision History

Version	Date	Description
V0.1	2018.05.30	Preliminary datasheet is released
V0.2	2018.09.12	Power Consumption is Updated (P.73 ~ 74)
V0.3	2018.11.26	1. DDR_RDRVUP/DN Pin Description is Updated (P.21) 2. Video Input Port Map is Updated (P.38)
V0.31	2018.12.04	Change the Device Name from PI5008K to PI5008KA
V0.32	2019.01.10	Video Input Port Map is updated (P.38, P.39)