Crystal Image through
Imaging Innovation

PIXELPLUS

FHD HDR ISP for Automotive Camera

With HD Analog Transmitter

PI6008K

Rev 0.34

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1. General Description

1.1. Product Overview

The PI6008K is a high performance and low power HDR ISP for automotive application. It supports up to 2.0M SDR or HDR CMOS Image Sensor with parallel or MIPI interface. It enhances HDR images with local tone map and provides excellent low light image with advanced noise reduction filter. It supports output interface with parallel or MIPI interface and HD analog video with embedded video DAC.

1.2. Features

- **CIS Input**
  - ✓ MIPI or Parallel Input
    - *Up to 1920x1080p@60Hz*
    - *MIPI CSI-2 RAW 10/12/14/16/20 Bits*
    - *MIPI CSI-2 1/2/4 Lane @ 600Mbps*
    - *Parallel 10/12 Bits with H/V Sync*
- Video Output
  - ✓ High Quality Free Down Scaling Engine
    - 1080p/960p to 960p/720p
    - 1080p/960p/720p to SD (NTSC/PAL)
  - ✓ MIPI or Parallel Output
    - *Selectable between scaler in and scaler out*
    - *Up to 1920x1080p@60Hz*
    - *MIPI CSI-2 RAW 10/12 Bits, YUV 16 Bits*
    - *MIPI CSI-2 1/2/4 Lane @ 450Mbps*
    - *Parallel 10/12/16 Bits with H/V/F Sync*
  - ✓ Analog HD Output
    - *Selectable between scaler in and scaler out*
    - Up to 1920x1080p @30fps
    - Video DAC with 10 Bits
    - Bi-directional UTC
- **Image Signal Processing**
  - ✓ HDR Tone-map
  - ✓ BLC, LSC, DPC

- ✓ 2D Noise Reduction
- ✓ De-mosaic
- ✓ Color / Gamma Correction
- ✓ De-color, Edge Enhancement
- ✓ Contrast & Brightness Control
- ✓ Hue & Saturation Control
- ✓ BW Mode
- ✓ Auto Flicker detection
- ✓ AE/AWB Static Engine

◆ Graphic Overlay

- ✓ 1-BMP (RLE) Layer
  - 4 Area (none-overlap)
  - Parking Guide Line
- ✓ 1 Font Layer
  - Font Width 16, 24 supported
- ✓ Private Zone Mask
  - Programmable 8-zones
  - Minimum 8x8 pixels

◆ **External Interface**

- ✓ UART 1 Ch
- ✓ Timer 4 Ch
- ✓ WDT 1 Ch
- ✓ Single / Dual SPI
- ✓ I2C Serial Interface
- ✓ Interrupt Controller
- ✓ GPIOs
- ✓ DMA

◆ **Low Power Consumption**

- ✓ TBD mW (Parallel In/Output), TBD mW (MIPI In/Output)

◆ **Operating Temperature/Package**

- ✓ -40~85 °C
- ✓ 68 QFN Package

1.3. Ordering Information

Table 1. Device Option

Product	Package Type	Target Application
PI6008K	68 QFN	Consumer

1.4. Block Diagram

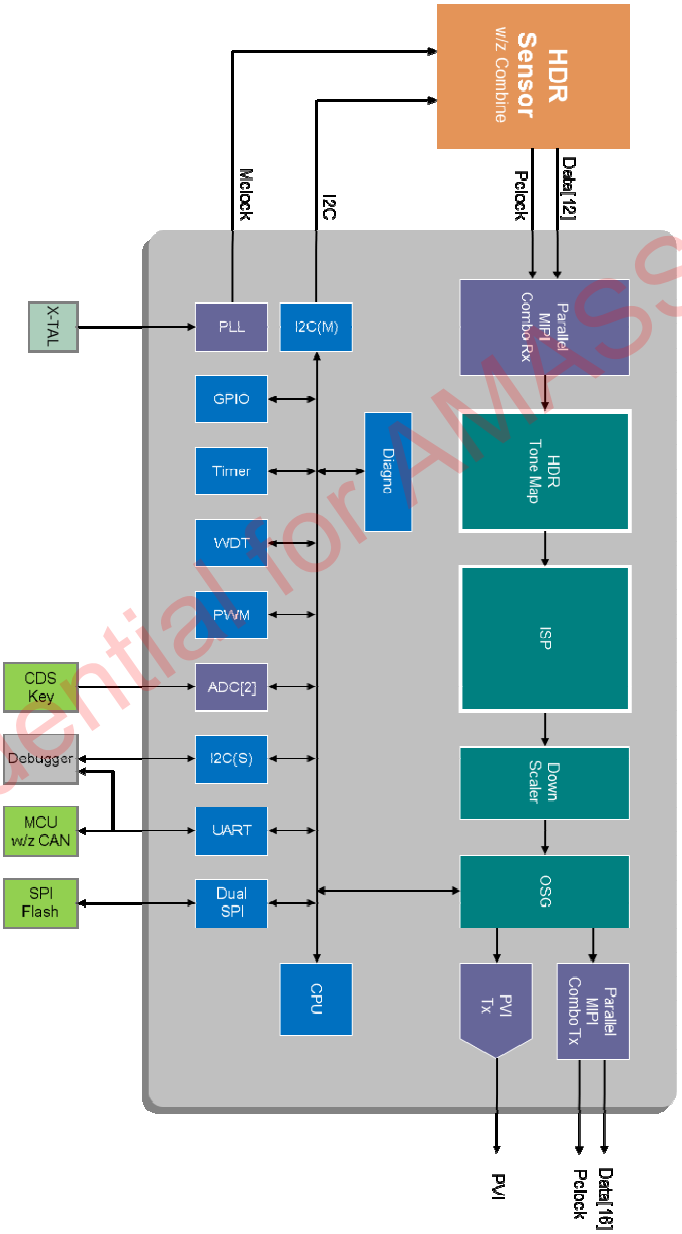


Fig 1. Functional Block Diagram

2. Pin Information

2.1. Pin Diagram

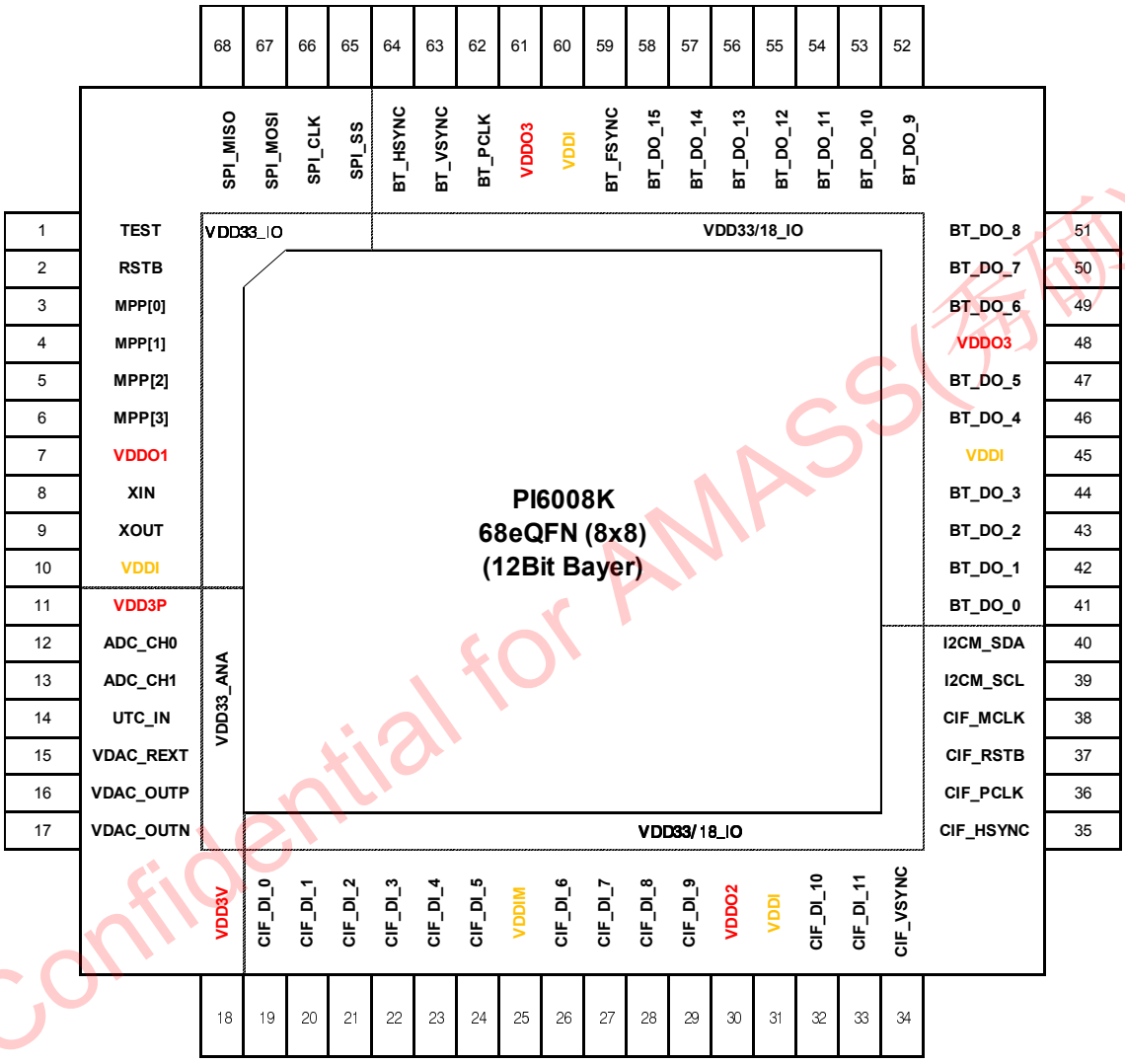


Fig 2. Pin Diagram

2.2. Pin Description

Table 2. Pin Description

Pin Name	Pin Number (68 QFN)	I/O	Pin Description
Sensor Digital Input or MIPI Rx CSI-2 Interface (10 Pin)			
CIF_DI_0 / MIPI_RX_DP0	19	I	CIF Digital Video Data Bit[0] or Data Lane 0 Positive Input for MIPI CSI-2
CIF_DI_1/ MIPI_RX_DN0	20	I	CIF Digital Video Data Bit[1] or Data Lane 0 Negative Input for MIPI CSI-2
CIF_DI_2/ MIPI_RX_DP1	21	I	CIF Digital Video Data Bit[2] or Data Lane 1 Positive Input for MIPI CSI-2
CIF_DI_3/ MIPI_RX_DN1	22	I	CIF Digital Video Data Bit[3] or Data Lane 1 Negative Input for MIPI CSI-2
CIF_DI_4/ MIPI_RX_CKP	23	I	CIF Digital Video Data Bit[4] or Clock Lane Positive Input for MIPI CSI-2
CIF_DI_5/ MIPI_RX_CKN	24	I	CIF Digital Video Data Bit[5] or Clock Lane Negative Input for MIPI CSI-2
CIF_DI_6/ MIPI_RX_DP2	26	I	CIF Digital Video Data Bit[6] or Data Lane 2 Positive Input for MIPI CSI-2
CIF_DI_7/ MIPI_RX_DN2	27	I	CIF Digital Video Data Bit[7] or Data Lane 2 Negative Input for MIPI CSI-2
CIF_DI_8/ MIPI_RX_DP3	28	I	CIF Digital Video Data Bit[8] or Data Lane 3 Positive Input for MIPI CSI-2
CIF_DI_9/ MIPI_RX_DN3	29	I	CIF Digital Video Data Bit[9] or Data Lane 3 Negative Input for MIPI CSI-2
Sensor Digital Input & Control (9 Pin)			
CIF_DI_10	32	I	CIF Digital Video Data Bit[10] or GPIO
CIF_DI_11	33	I	CIF Digital Video Data Bit[11] or GPIO
CIF_VSYNC	34	I	CIF Digital V Sync or GPIO
CIF_HSYNC	35	I	CIF Digital H Sync or GPIO
CIF_PCLK	36	I	CIF Digital Pixel Clock
CIF_RSTN	37	O	CIF Reset Output
CIF_MCLK	38	O	CIF reference Clock Output (27MHz)
I2CM_SCL	39	O	CIF I2C Serial Clock

I2CM_SDA	40	I/O	CIF I2C Serial Data
Digital Video Output or MIPI Tx CSI-2 Interface (20 Pin)			
BT_DO_0 / MIPI_TX_DP3	41	O	BT Digital Video Data Bit[0] or Data Lane 3 Positive Input for MIPI CSI-2
BT_DO_1/ MIPI_TX_DN3	42	O	BT Digital Video Data Bit[1] or Data Lane 3 Negative Input for MIPI CSI-2
BT_DO_2/ MIPI_TX_DP2	43	O	BT Digital Video Data Bit[2] or Data Lane 2 Positive Input for MIPI CSI-2
BT_DO_3/ MIPI_TX_DN2	44	O	BT Digital Video Data Bit[3] or Data Lane 2 Negative Input for MIPI CSI-2
BT_DO_4/ MIPI_TX_DP1	46	O	BT Digital Video Data Bit[4] or Clock Lane Positive Input for MIPI CSI-2
BT_DO_5/ MIPI_TX_CN1	47	O	BT Digital Video Data Bit[5] or Clock Lane Negative Input for MIPI CSI-2
BT_DO_6/ MIPI_TX_DP0	49	O	BT Digital Video Data Bit[6] or Data Lane 2 Positive Input for MIPI CSI-2
BT_DO_7/ MIPI_TX_DN0	50	O	BT Digital Video Data Bit[7] or Data Lane 2 Negative Input for MIPI CSI-2
BT_DO_8/ MIPI_TX_CKP	51	O	BT Digital Video Data Bit[4] or Clock Lane Positive Input for MIPI CSI-2
BT_DO_9/ MIPI_TX_CKN	52	O	BT Digital Video Data Bit[5] or Clock Lane Negative Input for MIPI CSI-2
BT_DO_10	53	O	BT Digital Video Data Bit[10] or JTAG_SRSTn
BT_DO_11	54	O	BT Digital Video Data Bit[11] or JTAG_TRSTn
BT_DO_12	55	O	BT Digital Video Data Bit[12] or JTAG_TDO
BT_DO_13	56	O	BT Digital Video Data Bit[13] or JTAG_TMS
BT_DO_14	57	O	BT Digital Video Data Bit[14] or JTAG_TDI
BT_DO_15	58	O	BT Digital Video Data Bit[15] or JTAG_TCK
BT_FSYNC	59	O	BT Digital F Sync or GPIO
BT_PCLK	62	O	BT Digital Pixel Clock
BT_VSYNC	63	O	BT Digital V Sync or GPIO
BT_HSYNC	64	O	BT Digital H Sync or GPIO
Analog I/O Interface (6 Pin)			
ADC_CH0	12	I	ADC CH 0 Input
ADC_CH1	13	I	ADC CH 1 Input

UTC_IN	14	I	Analog Input for UTC Interface
VDAC_REXT	15	I/O	External Reference for Analog Video
VDAC_OUTP	16	O	Analog Video Positive Output
VDAC_OUTN	17	O	Analog Video Negative Output
MPP Interface (4 Pin)			
MPP[0]	3	I/O	Multi-Purpose Pin 0
MPP[1]	4	I/O	Multi-Purpose Pin 1
MPP[2]	5	I/O	Multi-Purpose Pin 2
MPP[3]	6	I/O	Multi-Purpose Pin 3
SPI Interface (4 Pin)			
SPI_SS	65	O	SPI Slave Select
SPI_SCK	66	O	SPI Serial Clock
SPI_MOSI	67	I/O	SPI Master Output Slave Input
SPI_MISO	68	I/O	SPI Master Input Slave Output
System Control Interface (4 Pin)			
TEST	1	I	Reserved Pin for TEST (Should be connected to VSS)
RESETN	2	I	System Reset
XIN	8	I	Crystal (27MHz) Input
XOUT	9	O	Crystal (27MHz) Output
Power and Ground (12 Pin)			
VDD3P	11	P	3.3V Power for PLL
VDD3V	18	P	3.3V Power for VDAC
VDDIM	25	P	1.2V Core Power for MIPI Rx
VDDI	10/31/45/60	P	1.2V Core Power
VDDO1	7	P	3.3V Power for SPI / XTAL / MPP
VDDO2	30	P	1.8/3.3V I/O Power for CIF
VDDO3	48/61	P	1.8/3.3V Power for BT Output 3.3V Only Power for MIPI Tx Output
VSS	E-pad	G	Thermal PAD & Ground

Table 3. MPP[3:0] Pin Function Matrix

Pin Name	FUNC_MODE*			I/O	Function
MPP[0]	0	1	0	I	UART RX Data
	0	1	1	I	I2C Slave Serial Clock (Reserved)
	1	0	0	O	PWM4 Output
	1	1	1	I/O	GPIO
MPP[1]	0	1	0	O	UART TX Data
	0	1	1	I/O	I2C Slave Serial Data (Reserved)
	1	0	0	O	PWM5 Output
	1	1	1	I/O	GPIO
MPP[2]	0	1	0	I	UART RX Data (Reserved)
	0	1	1	I	I2C Slave Serial Clock
	1	0	0	O	PWM6 Output
	1	1	1	I/O	GPIO
MPP[3]	0	1	0	O	UART TX Data (Reserved)
	0	1	1	I/O	I2C Slave Serial Data
	1	0	0	O	PWM7 Output
	1	1	1	I/O	GPIO

* Note : FUNC_MODE of each pin is defined independently.

3. Functional Description

3.1. CPU platform

PI6008K includes Andes N7 processors. It has an ICE debugger that uses the JTAG interface. The CPU can be used for user application when the internal ISP does not need to be running. CPU platform and bus architecture is based on high performance AXI bus protocol. The CPU can access any sub block in the bus according to memory mapped addressing. The full CPU platform interconnections are as below.

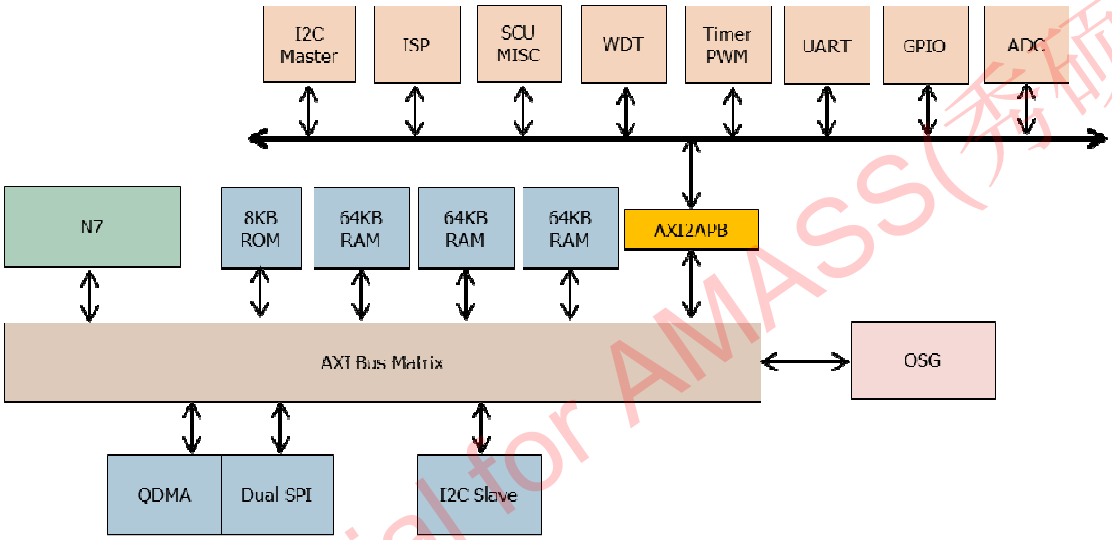


Fig 3. CPU Platform interconnections

3.1.1. Main feature

- 32-bit RISC CPU (Andes N705):
  - ✓ Max. 99MHz
- SPI type NOR flash interface
- Watch-Dog Timer
- General SPI master/slave for Flash Memory
- 8 channel timer/PWM
- 1 ports UART
- 1 ports I^2C slave, 1 port I^2C master
- 11 ports GPIO
  - ✓ 2 ports General purpose ADC

3.1.2. Boot Sequence

Since the PI6008K operation is based on CPU, boot sequence is necessary for initialization. During the boot sequence, PI6008K loads the program code from external SPI flash.

3.1.3. Flash Interface

Flash memory controller in PI6008K accesses the external SPI type flash. For the automotive system, fast booting is necessary and it mostly depends on flash read performance. Since the erase and write flash speed mainly just depends on the internal flash execution time, configurable single mode SPI interface is used for these operations. Other features of PI6008K flash controller are as below:

- Supports NOR flash memory
- 24 bit address mode
- Max. 256M-byte flash access
- Max. 64MHz interface clock

PI6008K include general SPI interface that share pin with Flash memory controller. It used for Program, Block Erase and Read Statues of Flash Memory.

3.1.4. UART Interface

One UART interfaces are built in PI6008K and available for debugging and communication with external devices. Main features of the UART are as below:

- Programmable baud rate control: Max. 230400
- HW configurable 16, 32, 64 and 128 bytes Tx/Rx FIFO with DMA
- 5~8 bits per character
- 1, 1.5 and 2 stop bits
- Even, odd and stick parity bits
- Line break, parity error, framing errors and data overrun detection

3.1.5. I2C Interface

PI6008K includes two I^2C ports, one of them support both master and slave mode, and the other one (Specific I^2C) supports slave mode only for special purpose (communication with ISP

tuning tool). The pins of general I^2C are dedicated, but specific I^2C pin is shared with other pins. All I^2C ports do not have pull-up resistance within PI6008K. Therefore, it is necessary to attach pull-up resistance on the outside. Main features of the I^2C are as below:

- Data format: 7/10-bit address
- Slave mode format: programmable
- Master mode:
  - ✓ 1 byte address + 1 byte data
  - ✓ 1 byte address + 2 byte data
  - ✓ 2 byte address + 1 byte data
  - ✓ 2 byte address + 2 byte data
- Speed
  - ✓ Fast mode(max. 400Kbit/sec)
  - ✓ Standard mode(max. 100Kbit/sec)

3.1.6. Timers/PWM

There are eight 32-bit timers in PI6008K. All eight timers are available for user application, especially fifth ~ eighth timers are connected to PWM (Pulse Width Modulation) function which is used for wide range of purpose. PWM signal can be emitted to outside by alternative pin selection. User can select various timer clocks divided from main clock (27MHz) as range 1/2 to 1/16.

3.1.7. Watch-Dog Timer

The watch-dog timer is used to reset the whole chip when the firmware runs out of order or some systematic error detected. It is consists 32-bit counter and its clock is selected as the timer clock source.

3.1.8. General ADC

PI6008K includes two general purpose ADC having 8-bit precision. It converts 0~3.3V analog input to 8-bit digital output. Sampling rate is quite slow and it is about 128K samples/sec.

3.1.9. General Purpose I/O

PI6008K has 11 GPIO (General Purpose I/O) pins. Each pin, which is a bi-directional buffer,

may be used in input mode or output mode by program. When each GPIO is used in the input mode, it may be used as an external interrupt source. By signal level or edge fed to GPIO pins, interrupt may be transmitted to PI6008K CPU. The use of level and edge, and the decision of interrupt source of high/low level and rising/falling edge all may be selected by program.

3.1.10. Clock & PLL Interface

A crystal can be connected across terminals XIN and XOUT, or an external oscillator clock input can be connected to XIN Pin. PI6008K has dual PLL with clock source, one is used to generate system and video processing clock, and the other is used to generate a clock for MIPI Tx output interface.

3.2. Camera Input Format

PI6008K supports parallel or MIPI Rx interface for Camera Input Format.

3.2.1. Parallel Input

PI6008K supports 10/12/16/20 Bits Bayer video input with various pin map configuration as following table.

Table 4. SDR/HDR Bayer Pin Map

Pin Name	Single Bayer Mode		HDR Bayer Mode	
	10 Bit Bayer	12 Bit Bayer	16 Bits	20 Bits
CIF_DI[0]		Bayer[0]		
CIF_DI[1]		Bayer[1]		
CIF_DI[2]	Bayer[0]	Bayer[2]		Bayer[0] / Bayer[10]
CIF_DI[3]	Bayer[1]	Bayer[3]		Bayer[1] / Bayer[11]
CIF_DI[4]	Bayer[2]	Bayer[4]	Bayer[0] / Bayer[8]	Bayer[2] / Bayer[12]
CIF_DI[5]	Bayer[3]	Bayer[5]	Bayer[1] / Bayer[9]	Bayer[3] / Bayer[13]
CIF_DI[6]	Bayer[4]	Bayer[6]	Bayer[2] / Bayer[10]	Bayer[4] / Bayer[14]
CIF_DI[7]	Bayer[5]	Bayer[7]	Bayer[3] / Bayer[11]	Bayer[5] / Bayer[15]
CIF_DI[8]	Bayer[6]	Bayer[8]	Bayer[4] / Bayer[12]	Bayer[6] / Bayer[16]
CIF_DI[9]	Bayer[7]	Bayer[9]	Bayer[5] / Bayer[13]	Bayer[7] / Bayer[17]
CIF_DI[10]	Bayer[8]	Bayer[10]	Bayer[6] / Bayer[14]	Bayer[8] / Bayer[18]
CIF_DI[11]	Bayer[9]	Bayer[11]	Bayer[7] / Bayer[15]	Bayer[9] / Bayer[19]

3.2.2. MIPI CSI-2 Rx Input

PI6008K supports MIPI Rx interface compliant with MIPI CSI2 V1.3 standard and DPHY V1.2 standard through 1 clock lane and 4 data lanes. MIPI Rx supports functions below

- Data rate constraints (per lane)
  - ✓ Min. : 200 Mbps
  - ✓ Max. : 520 Mbps
- Numbers of lanes used : 1-lane, 2-lane, 4-lane (Support Data Lane Swap Function)
- Transmission : Packets are transmitted in HSDT only
- Packets (image format)
  - ✓ Short packets : frame start, frame end
  - ✓ Long packets : RAW 8-bit, RAW 10-bit, RAW 12-bit, RAW 14-bit
- ECC(Error Correction Code), CRC(Cycle Redundancy Check)

The MIPI data lane transmission order for 4 lane and 2 lane mode is described following figure.

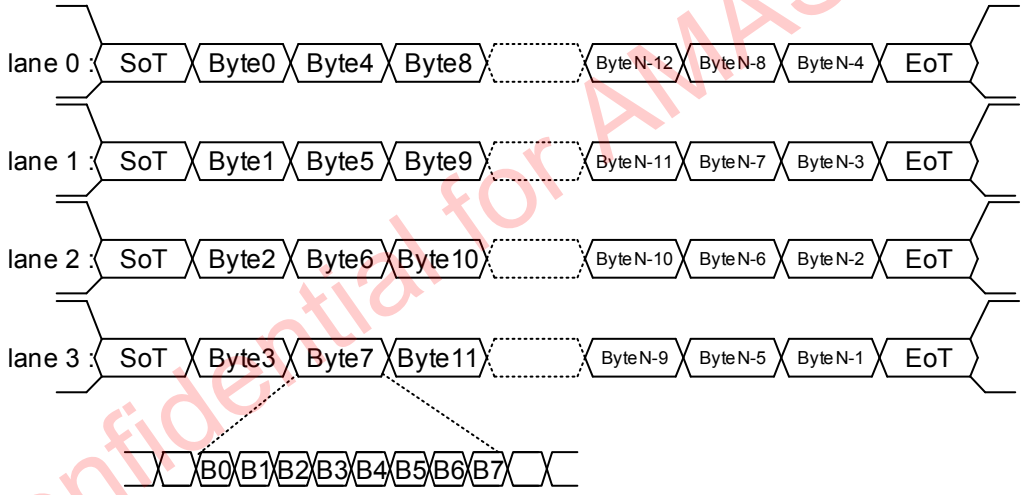


Fig 4. MIPI Data Lane Transmission Order for 4 Lane Mode

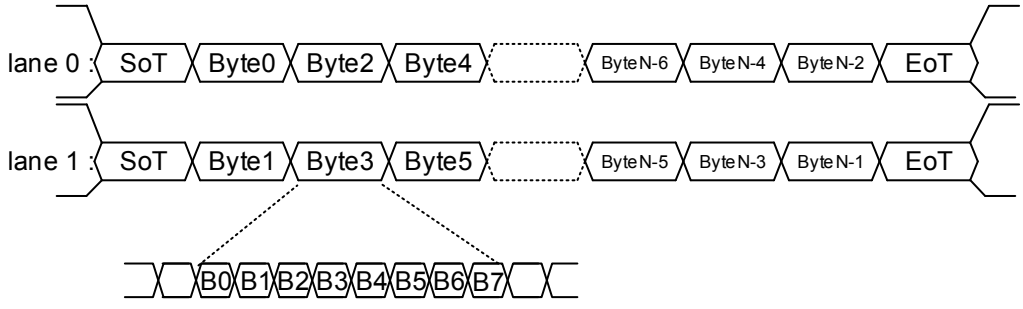


Fig 5. MIPI Data Lane Transmission Order for 2 Lane Mode

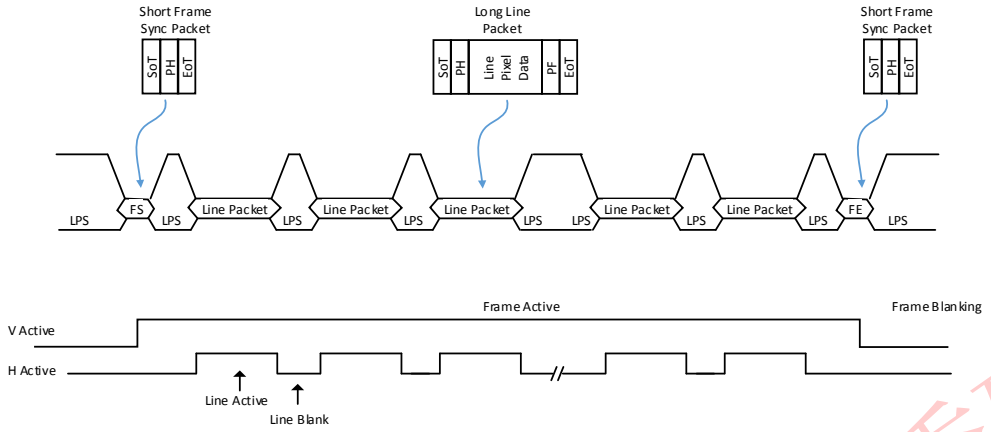


Fig 6. MIPI Low Power Protocol

PI6008K MIPI Rx receive RAW 8/10/12/14-bit packet and generate vsync, hsync bayer pixel data. Frame start, frame end packet corresponds to vsync active period. A line packet is a 1-line image. The PH value of the line packet is analyzed to obtain the bit-width and the word count (active width period). Vertical blanking period maintains LPS state or receives blanking packet.

3.3. ISP Processing

The ISP processes bayer image data from external image sensor, and improves the overall image quality. It consists of several functional blocks, and each block corrects and enhances the image data in terms of dynamic range, resolution, color and sharpness. PI6008K includes an ISP to handle image sensor input and each ISP can process a combined and compressed raw data from HDR (High Dynamic Range) sensor which is generally used for automotive application. Functional block diagram for ISP is as figure below.

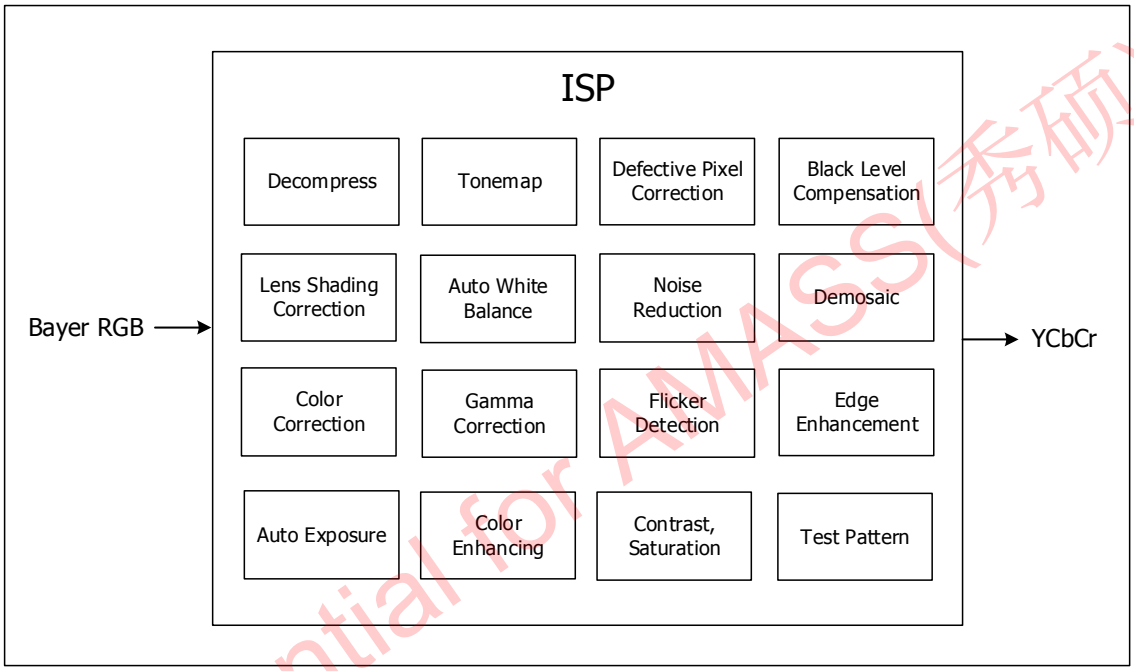


Fig 7. Image Signal Processing block

The ISP block receives bayer format data through MIPI or parallel interface port. Normally, SDR (Standard Dynamic Range) sensors outputs 10-bit (60db) bayer format data to ISP and HDR sensors outputs 16-bit (96db), 20-bit (120db) combined, uncompressed format or 12-bit combined, compressed format. Since the parallel port supports only up to 12-bit interface, in case of HDR combined, uncompressed format, MIPI interface should be utilized. PI6008K does not support combine function of HDR sensor which combines several different exposures images of the same scene. The combining of multiple exposure images must be performed on the external sensor chip.

Input bayer data is converted into the RGB data by color interpolation (demosaic) process. Before RGB conversion, correcting the defective pixel and lens shading, balancing the color,

optimizing the exposure and removing the noise functions are performed as a preprocessing. In case of HDR sensor, tonemap process is performed on this stage to get the high dynamic range image. PI6008K supports local tonemap algorithm which helps bring out details by increasing contrast in local areas. RGB data is converted to YUV data after correcting the color and gamma. The ISP more improves the sharpness and color in YUV domain. After globally adjusting contrast, saturation and brightness again, ISP processed image is created in the YUV format.

Most part of the ISP function is implemented in dedicated hardware cores, but some of them such as tonemap, auto exposure and white balance demands additional software processing. PI6008K has a built-in CPU core that can be used for ISP processing.

The ISP output image quality is mostly dependent on tuning, and since the preferred images are different for each user, tuning process is important during the full system development. To facilitate tuning of parameters, specific ISP tuning tool is generally used. PI6008K proprietary tuning tool uses I^2C slave port to control the registers in ISP.

Main features of ISP are as below:

- 8/10/12-bit bayer raw input
  - ✓ 8/10-bit non-HDR raw
  - ✓ 12-bit compressed combined raw
  - ✓ Up to 20-bit uncompressed combined raw
- Max. FHD 1920x1080 60fps, HD 1280x720 60fps
- Supports global and local tone map algorithm
- Auto exposure and white balance
- High performance spatial Denoising filter (2DNR)
- Color interpolation (Demosaicking)
- Defect pixel correction
- Lens shading correction
- Color correction
- Gamma correction
- Color correction
- Edge and sharpness enhancement
- Color Enhancing with hue, saturation control

3.4. Down Scaler Processing

The PI6008K provides the high quality free down scaling engine for video format conversion such as FHD (1080p) to HD (720p) and FHD/HD to SD (NTSC/PAL) conversion. It also converts operating clock through embedded FIFO so that it can produce the standard video output and clock regardless of video input format.

3.5. OSG Overlay

OSG is a block that control display overlay video output. Main feature is follows.

- 4 Overlay Layers : 1-area each
  - ✓ RLE (Run-Length Encoding)
- 1 Font Layer
  - ✓ Font width : 8,16,24
  - ✓ Font height : 8, 16, 24, 32, …, 120, 128
- Private Zone
  - ✓ Programmable 8 zones

For supporting upper function OSG has below Block Diagram.

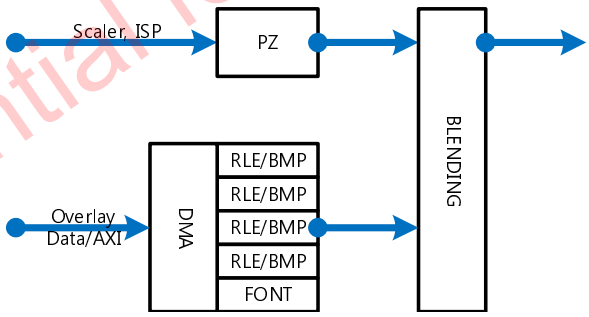


Fig 8. OSG Block Diagram

OSG is block of processing last display image. Input image has blended with five overlay layers. 4 overlay layer support RLE mode, one font layer is overlaid with designated font. Each layer puts the overlay data on an incoming video in RGB format. Each layer process one overlay image. Each layer can control blending rate.

Data for overlay should be saved internal SRAM before OSG block is operated.

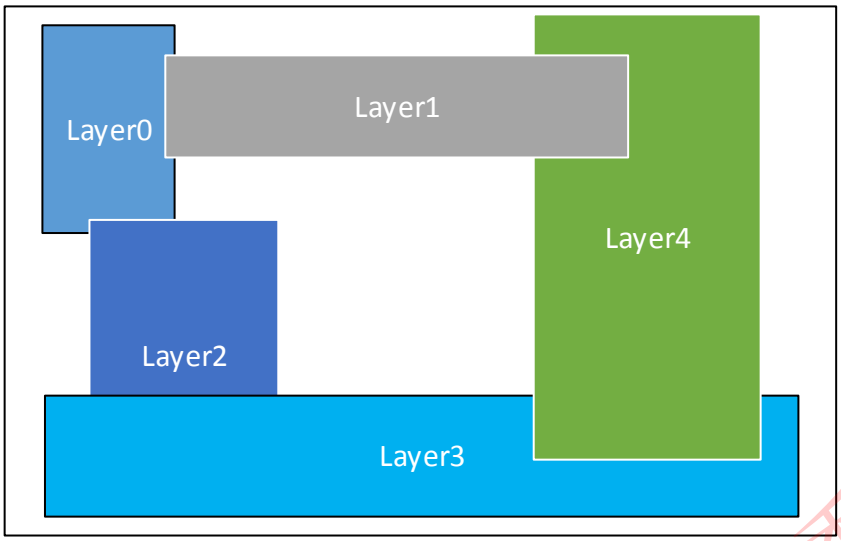


Fig 9. Layer Allocation Example

3.5.1. RLE Mode

RLE mode compress to 8 bit BMP overlay data with RLE algorithm. Compressed data is decoded to uncompressed original BMP 8-bit Overlay data and it overlaid with RGB and alpha blending value in stored 256 LUT by overlay data value.

Table 5. . RLE Data Format

Overlay Data format	Description
8-bit(LUT Mode)	256 LUT, Each LUT is 32-bit and consisted as below. [31:24]: Alpha, [23:16]: R, [15:8]: G, [7:0]: B

3.5.2. FONT Mode

It overlaid Font selected by designated character code.

Overlay Data of RGB format is converted to blend with OSG input. It can program Coefficient that is used for converting from RGB to YUV.

3.5.3. Private Mask Overlay

Private Mask Overlay has 8 Overlays with controllable Mask color and size and position.

3.6. Video Output

PI6008K supports parallel or MIPI interface for digital video output interface, and supports PVI HD/SD analog interface for video analog output interface.

3.6.1. Parallel Output

Table 6. . YCbCr and Bayer Pin Map

Pin Name	YCbCr Mode		Bayer Mode	
	8 Bits	16 Bits	10 Bits	12 Bits
BT_DO[0]	YCbCr[0]	CbCR[0] /Y[0]		
BT_DO[1]	YCbCr[1]	CbCr[1] /Y[1]		
BT_DO[2]	YCbCr[2]	CbCr[2] /Y[2]		
BT_DO[3]	YCbCr[3]	CbCr[3] /Y[3]		
BT_DO[4]	YCbCr[4]	CbCr[4] /Y[4]		Bayer[0]
BT_DO[5]	YCbCr[5]	CbCr[5] /Y[5]		Bayer[1]
BT_DO[6]	YCbCr[6]	CbCr[6] /Y[6]	Bayer[0]	Bayer[2]
BT_DO[7]	YCbCr[7]	CbCr[7] /Y[7]	Bayer[1]	Bayer[3]
BT_DO[8]	YCbCr[0]	Y[0] / CbCR[0]	Bayer[2]	Bayer[4]
BT_DO[9]	YCbCr[1]	Y[1] / CbCR[1]	Bayer[3]	Bayer[5]
BT_DO[10]	YCbCr[2]	Y[2] / CbCR[2]	Bayer[4]	Bayer[6]
BT_DO[11]	YCbCr[3]	Y[3] / CbCR[3]	Bayer[5]	Bayer[7]
BT_DO[12]	YCbCr[4]	Y[4] / CbCR[4]	Bayer[6]	Bayer[8]
BT_DO[13]	YCbCr[5]	Y[5] / CbCR[5]	Bayer[7]	Bayer[9]
BT_DO[14]	YCbCr[6]	Y[6] / CbCR[6]	Bayer[8]	Bayer[10]
BT_DO[15]	YCbCr[7]	Y[7] / CbCR[7]	Bayer[9]	Bayer[11]

The video output data is ITU-R BT.656/1302/1120 standard format with 27/36/74.25/148.5MHz. The Fig 10 and Fig 11 show the timing diagram of standard ITU-R BT.656/1302/ 1120 format.

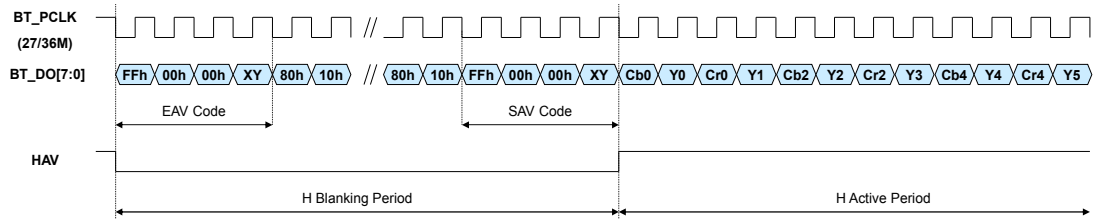


Fig 10. The Timing Diagram of Standard ITU-R BT.656/1302 Format

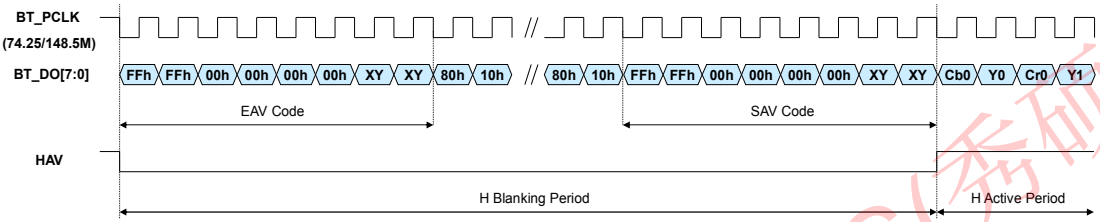


Fig 11. The Timing Diagram of Standard ITU-R BT.1120 Format

3.6.2. MIPI Tx Output

The PI6008K supports a MIPI interface compliant with MIPI CSI2 V1.00 standard and DPHY V1.00.00 standard with 1 clock lane and 4 data lane. The max data rate of MIPI data lane is up to 450Mbps in HS transmission with RAW 10/12 bits and YUV 422-8bit format.

- Data rate constraints (per lane)
  - ✓ Min. : 200 Mbps
  - ✓ Max. : 450 Mbps
- Numbers of lanes used : 1-lane, 2-lane, 4-lane (Support Data Lane Swap Function)
- Transmission : Packets are transmitted in HSDT only
- Packets (image format)
  - ✓ Short packets : frame start, frame end
  - ✓ Long packets : RAW 10-bit, RAW 12-bit, YUV 8-bit
- ECC(Error Correction Code), CRC(Cycle Redundancy Check)

During MIPI Tx operation, there are two lane states such as Low Power (LP) state and High Speed (HS) state. The HS Tx always drives the lane differentially so that it results in two possible HS lane states such as differential-0 and differential-1. The LP Tx drives two lines of a lane independently with single-ended termination so that it results in four possible LP lane states that are used for Control Mode and Escape Mode. The HS data transmission is used to

transfer data in burst mode. It starts from and ends with a stop state (LP-11) of LP Control Mode. The special Escape Mode can only be entered via a request within Control Mode. The data lane shall always exit Escape Mode and return to Control Mode with stop state. If not in HS state or Escape Mode, the data lane shall stay in control mode.

Table 7. Lane State Description of MIPI Transmission

State Code	Line Voltage Levels		High-Speed	Low-Power	
	DP-Line	DN-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

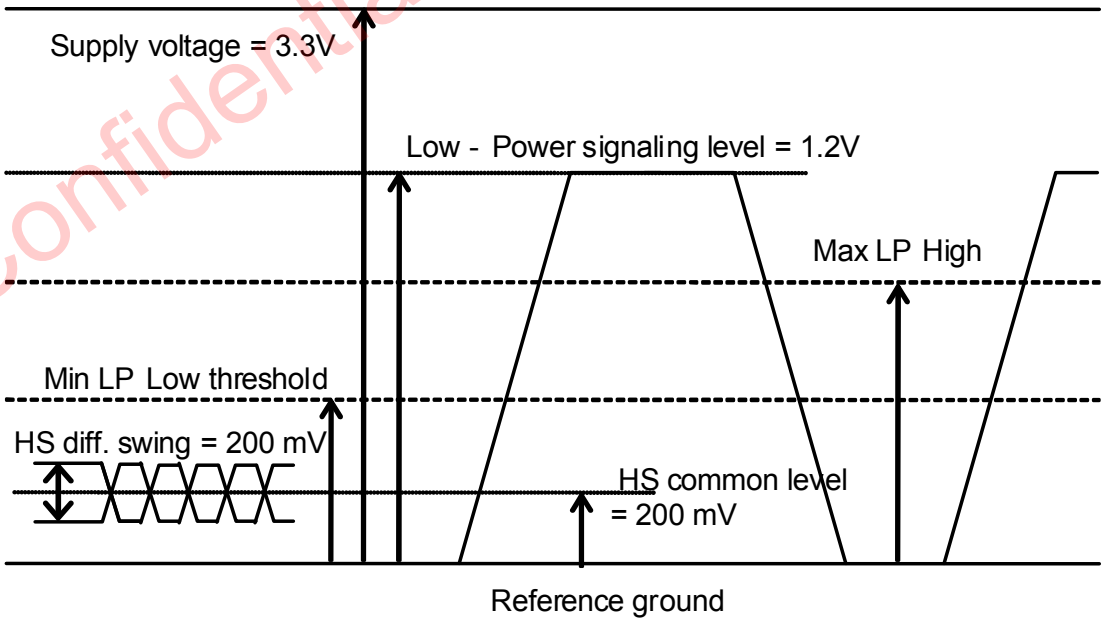


Fig 12. MIPI Signal Levels for HS and LP State

The Low Level Protocol (LLP) is a byte oriented, packet based protocol that supports the transport of image data using short and long packet formats. After exiting from the low power state, the Start of Transmission (ST) sequence indicates the start of the packet and the End of Transmission (ET) sequence indicates the end of the packet.

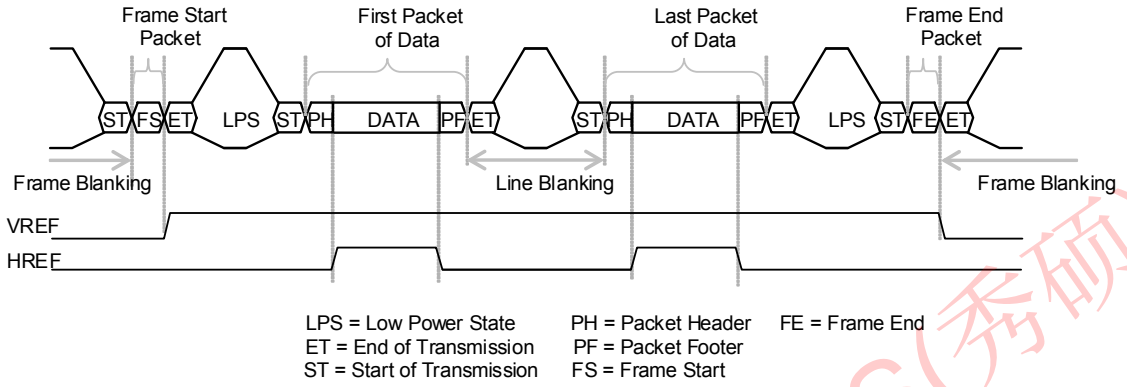


Fig 13. MIPI Low Power Protocol

The PI6008K supports two kinds of Short packet format for frame synchronization such as Frame Start (FS) packet and Frame End (FE) packet. Each image frame shall begin with a FS packet containing the Frame Start Code. The FS Packet shall be followed by one or more long packets containing image data. Each image frame shall end with the FE packet containing the Frame End Code.

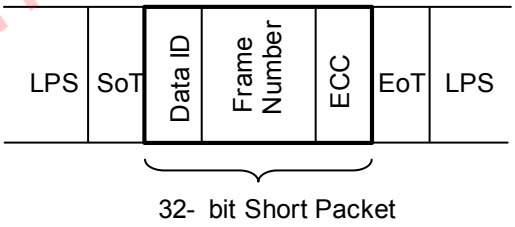


Fig 14. MIPI Short Packet Structure

A Long packet shall consist of 3 elements such as a 32-bit Packet Header (PH), an application Data Payload with a variable number of 8-bit words and a 16-bit Packet Footer (PF).

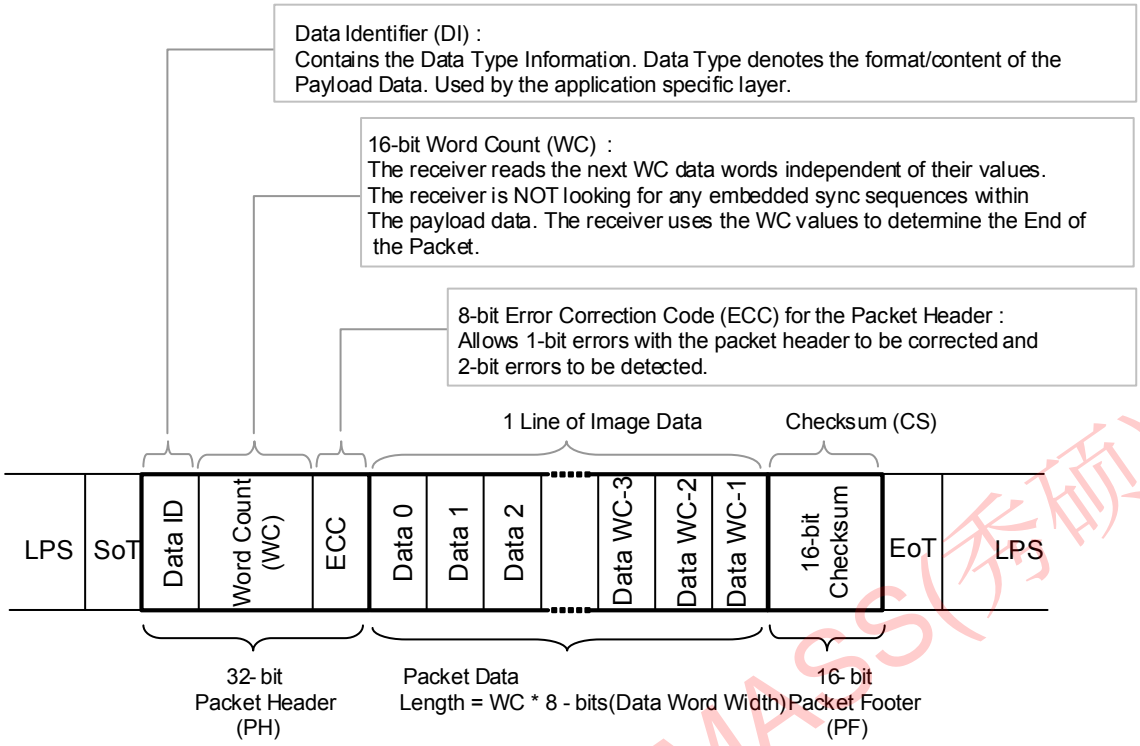


Fig 15. MIPI Long Packet Structure

3.6.3. PVI SD/HD Analog Output

The analog HD Tx in PI6008K supports all existing HD/SD analog video standard and all video format (1080p@25/30, 720p@25/30/50/60, 480i@60 and 576i@50) by programming registers. The band selected filter adjusts the luminance and chrominance signal processing according to video standard and format. The analog HD Tx also supports contrast, brightness, saturation and hue control for the picture adjustment and supplies a various color space conversion. If the video output resolution of analog HD Tx and digital video output is same, the analog HD/SD and digital video output can be supported simultaneously.

The PI6008K also supports any bidirectional Coaxial/UTP PTZ protocol that transmits the data between a controller and the analog HD/SD receiver.

4. Electrical Characteristics

4.1. DC Electrical Characteristics

Table 8. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3V, VDD3P	-0.5		4.6	V	
Voltage for VDDO1, VDDO2, VDDO3	-0.5		4.6	V	
Voltage for VDDIM, VDDI Pin	-0.5		1.8	V	
Voltage for Digital Input Pin	-0.5		3.8	V	
Storage Temperature	-40		125	°C	
Peak Temperature on Reflow Soldering			260	°C	15 Sec

NOTE: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition

Table 9. Recommended Operating Conditions for Power and Temperature

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3V, VDD3P, VDDO1 Pin	2.97	3.3	3.63	V	
Voltage for VDDO2, VDDO3 Pin (Parallel)	2.97	3.3	3.63	V	For 3.3V
	2.25	2.5	2.75	V	For 2.5V
	1.62	1.8	1.98	V	For 1.8V
Voltage for VDDO2 Pin (MIPI Rx)	2.97	3.3	3.63	V	For 3.3V
	1.62	1.8	1.98	V	For 1.8V
Voltage for VDDO3 Pin (MIPI Tx)	2.97	3.3	3.63	V	3.3V Only
Voltage for VDDIM, VDDI Pin	1.14	1.2	1.26	V	
Ambient Operation Temperature	-30		85	°C	

Note : Power On/Off sequence should keep the following rule

- Apply power to VDD3V, VDD3P, VDDO1, VDDO2, VDDO3 and VDDIM, VDDI at the same time
- If it is difficult to apply the power to these pins at the same time, apply the power to VDD3V, VDD3P, VDDO1, VDDO2, VDDO3 first and to VDDIM, VDDI later
- Cut the power of VDD3V, VDD3P, VDDO1, VDDO2, VDDO3 and VDDIM, VDDI at the

same time

- If it is difficult to cut the power of these pins at the same time, cut the power of VDDIM, VDDI first and of VDDO2, VDDO3, VDDO1, VDD3V, VDD3P later

Table 10. Recommended Operating Conditions for Digital I/O (For 1.8V)

Parameter	Min	Typ	Max	Unit	Condition
Digital Inputs					
Input High Voltage	1.2			V	
Input Low Voltage			0.6	V	
Input Capacitance		6		pF	
Input Leakage Current	-10		+ 10	uA	
Digital Output					
Output High Voltage	VDDIO-0.4			V	
Output Low Voltage			0.4	V	
Output Current	2.4 / 4.8 / 7.2 / 9.6			mA	Depends on Register
Tri-state Output Current	-10		+ 10	uA	
Output Capacitance		6		pF	

Table 11. Recommended Operating Conditions for Digital I/O (For 2.5V)

Parameter	Min	Typ	Max	Unit	Condition
Digital Inputs					
Input High Voltage	1.7			V	
Input Low Voltage			0.7	V	
Input Capacitance		6		pF	
Input Leakage Current	-10		+ 10	uA	
Digital Output					
Output High Voltage	VDDIO-0.4			V	
Output Low Voltage			0.4	V	
Output Current	3.8 / 7.6 / 11.4 / 15.2			mA	Depends on Register
Tri-state Output Current	-10		+ 10	uA	
Output Capacitance		6		pF	

Table 12. Recommended Operating Conditions for Digital I/O (For 3.3V)

Parameter	Min	Typ	Max	Unit	Condition
Digital Inputs					
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	
Input Capacitance		6		pF	
Input Leakage Current	-10		+ 10	uA	
Digital Output					
Output High Voltage	VDDIO-0.4			V	
Output Low Voltage			0.4	V	
Output Current	5 / 10 / 15 / 20			mA	Depends on Register
Tri-state Output Current	-10		+ 10	uA	
Output Capacitance		6		pF	

Table 13. Supply Current and Power Dissipation (Parallel I/O)

Parameter	3.3V Parallel I/O			1.8V Parallel I/O			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply Current at VDDIM/VDDI (1.2V)	109	120	134	109	120	134	mA
Supply Current at VDDO2	1	1	1	1	1	1	mA
Supply Current at VDDO3	6	7	8	6	7	8	mA
Supply Current at VDDO1/VDD3V/VDD3P	40	41	43	40	41	43	mA
Total Power Dissipation	285.9	305.7	332.4	275.4	293.7	318.9	mW

Note : Power Checked at normal operation condition under 1280x960HD@30Hz.

Table 14. Supply Current and Power Dissipation (MIPI I/O)

Parameter	3.3V MIPI I/O			1.8V MIPI IN / 3.3V MIPI OUT			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply Current at VDDIM/VDDI (1.2V)	110	122	136	110	122	136	mA
Supply Current at VDDO2	3	3	4	1	1	1	mA
Supply Current at VDDO3 (3.3V Only)	6	7	8	6	7	8	mA
Supply Current at VDDO1/VDD3V/VDD3P	39	41	42	39	41	42	mA
Total Power Dissipation	290.4	314.7	341.4	282.3	306.6	330	mW

Note : **VDDO3 for MIPI Output should be only 3.3V**.

Note : Power Checked at normal operation condition under 1280x960HD@30Hz.

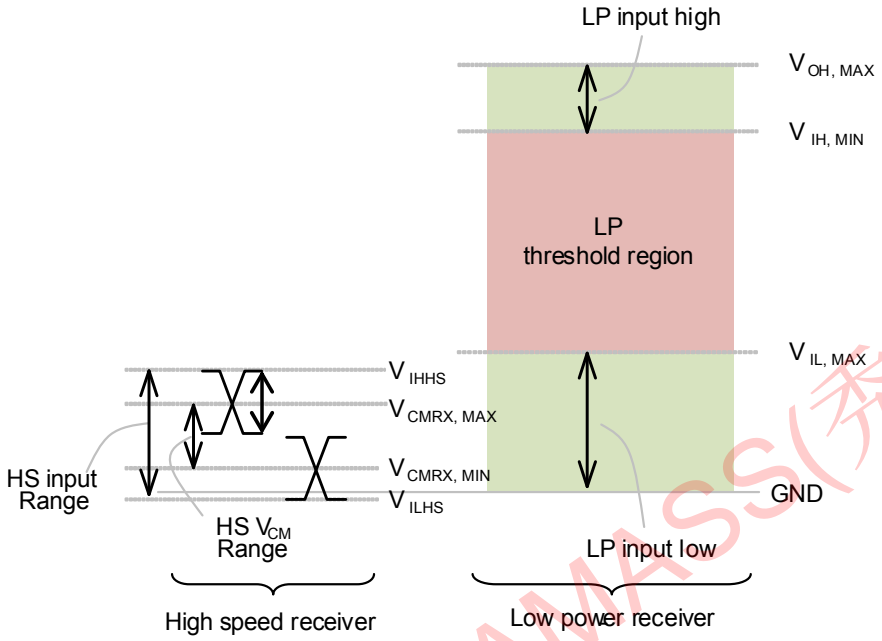


Fig3.8 MIPI D-PHY signaling levels

Table 15. MIPI Rx DC Specification

Parameter	Min	Typ	Max	Unit	Condition
Pin Signal voltage Range	-50		1350	mV	
LP Receiver					
Input High Voltage	880			mV	
Input Low Voltage			550	mV	
Input hysteresis	330			mV	
HS Receiver					
Common-mode voltage	70	200	330	mV	
Differential input High Threshold			70	mV	
Differential input low Threshold	-70			mV	
Single-ended input high voltage		300	460	mV	
Single-ended input low voltage	-40	100			

Table 16. MIPI Tx DC Specification

Parameter	Symbol	Min	Typ	Max	Unit
LP Transmitter					
Thevenin output low level	V_{OL}	-50		50	mV
Thevenin output High level	V_{OH}	1.1	1.2	1.3	V
Output Impedance	Z_{OLP}	110			Ohm
HS Transmitter					
HS transmit differential voltage	V_{OD}	140	200	270	mV
HS transmit static common mode voltage	V_{CMTX}	150	200	250	mV
V_{OD} mismatch when output is Differntial-1 or Differntial-0	ΔV_{OD}			10	mV
V_{CMTX} mismatch when output is Differntial-1 or Differntial-0	ΔV_{CMTX}			5	mV
HS output high voltage	V_{OHHS}			360	mV
Single ended output impedance	Z_{OS}	40	50	62.5	Ohm
Single ended output impedance mismatch	ΔZ_{OS}			10	%
Common-level variation for 100~450MHz	ΔV_{CMTX}			25	mV

4.2. AC Electrical Characteristics

Table 17. Analog Input and Output Parameter

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Input					
Nominal Frequency	$f_{x\text{-}tal}$		27		MHz
Frequency Deviation	$\Delta f_{x\text{-}tal}$	-50		50	ppm
Duty Cycle	$dt_{x\text{-}tal}$			55	%
Analog Clock PLL					
RMS Jitter	rms_{pll}				ps
Duty Cycle	dt_{pll}				%
Lock Time	t_{lock}				us
Generic ADCs					
Differential Non-Linearity	DLE				
Integral Non-Linearity	ILE				
Signal-to-Noise Ratio	SNR				dB

Table 18. Parallel Input AC Specification

Parameter	Symbol	Min	Typ	Max	Unit
Setup time of data		2			ns
Hold time of data		1			ns
clock Period		6			ns

Table 19. MIPI Rx AC Specification

Parameter	Symbol	Min	Typ	Max	Unit
LP Receiver					
Input pulse rejection				300	ps
Minimum pulse width response		20			ns
Length of any Low Power state period		50			ns
HS Receiver					

Data Rate per Lane		200		520	Mbit/s
HS Clock Frequency for Clock Lane		100		260	MHz
Common-mode interference				100	mv
Data to Clock skew		-0.15		0.15	UI
Data to Clock setup time		0.15			UI
Clock to Data hold time		0.15			UI
Period of dual data rate clock		2	2	2	UI

Table 20. MIPI Tx AC Specification

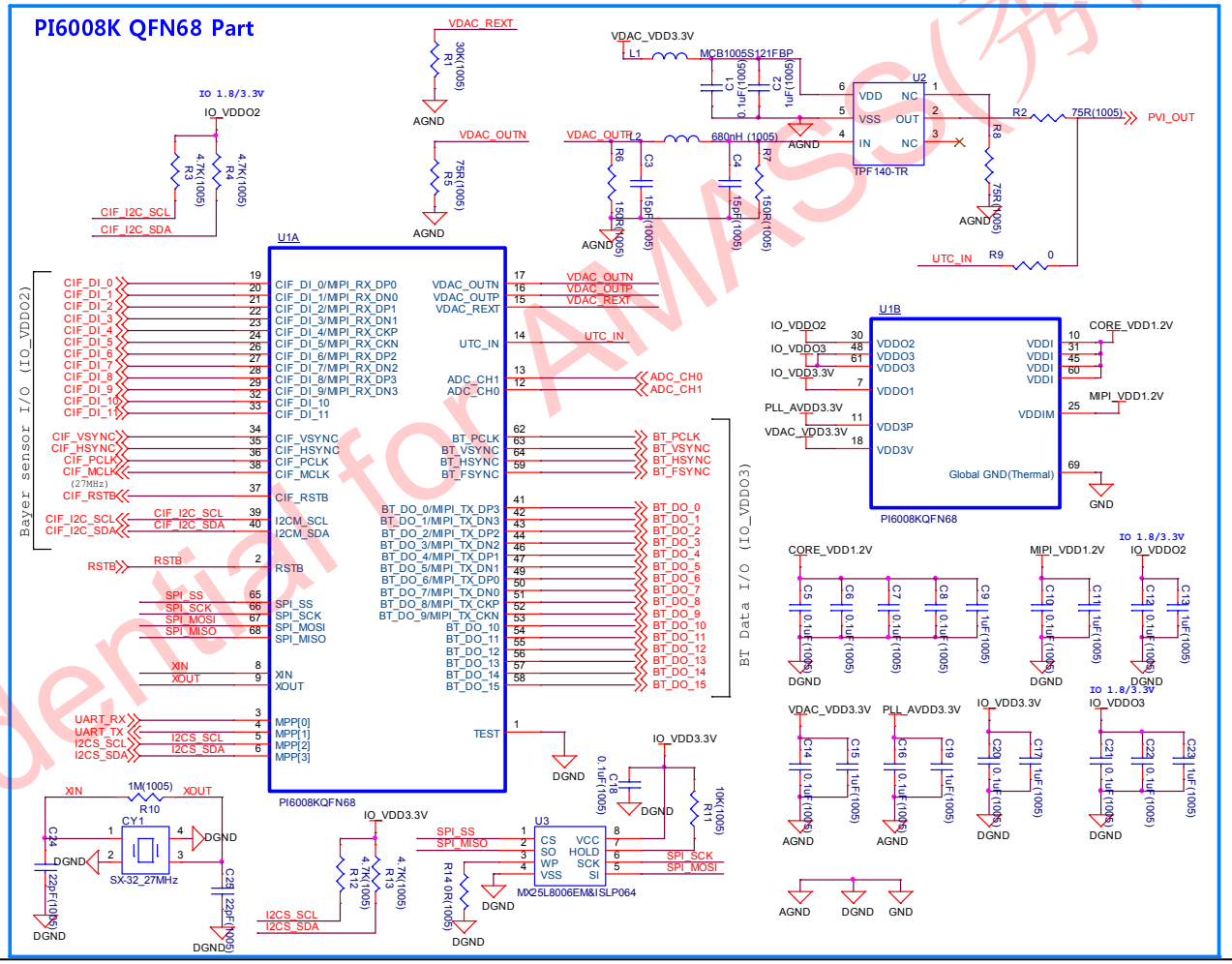
Parameter	Symbol	Min	Typ	Max	Unit
LP Transmitter					
15% ~ 85% rise/fall time	t_{RLP}/t_{FLP}			25	ns
30% ~ 85% rise time in EOT state	t_{REOT}			35	ns
Slew rate	dV/dt_{SR}			120	mV/ns
Load capacitance	C_{LOAD}	0		70	pF
HS Transmitter					
HS transmit Data Rate		200		450	Mbps
HS Clock Frequency		100		225	MHz
20% ~ 80% rise/fall time	t_R/t_F	150		0.3UI	ps

Table 21. Parallel Output AC Specification

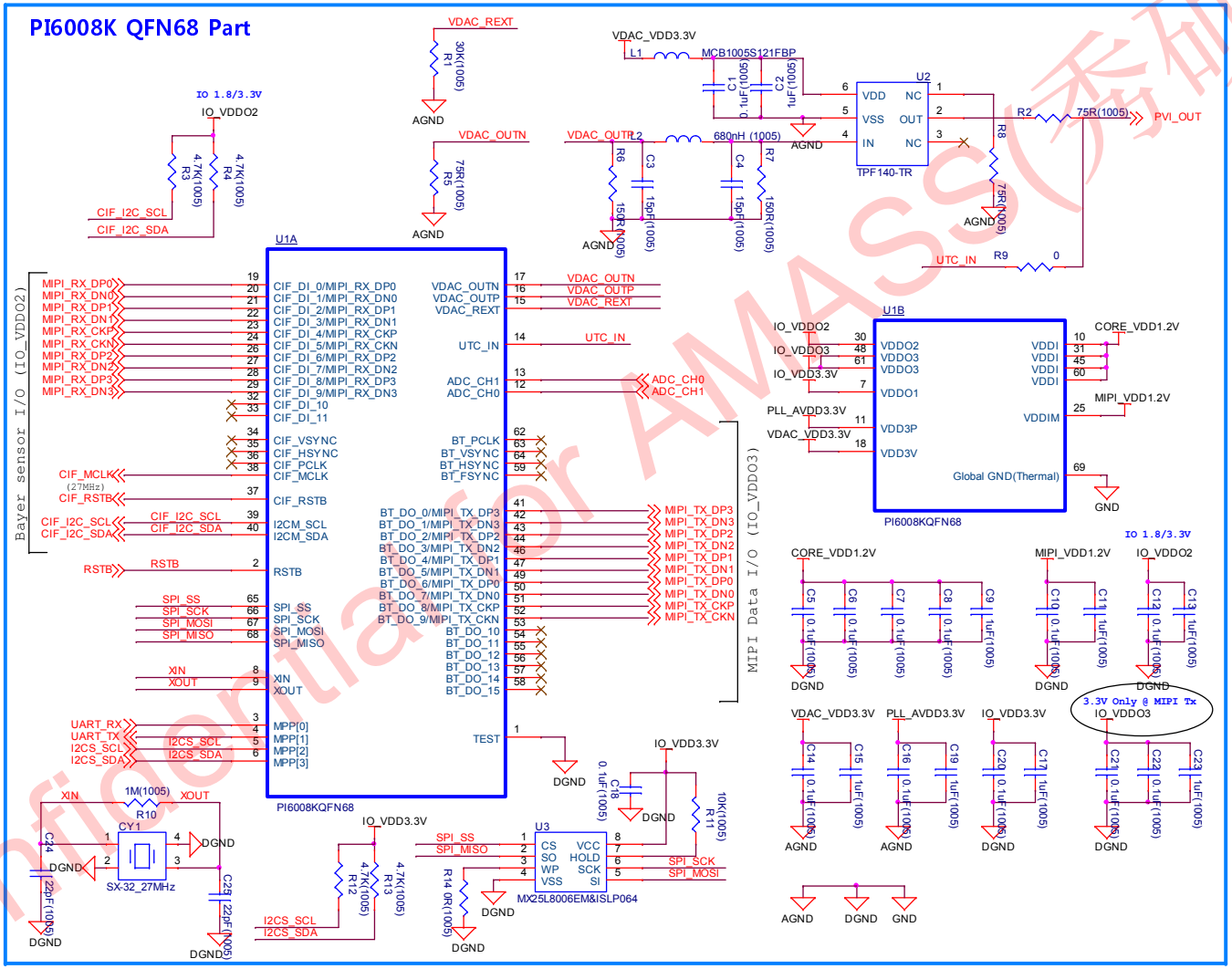
Parameter	Symbol	Min	Typ	Max	Unit
Clock to Data Propagation Time					
Data Skew			1		ns

5. Application Schematic

5.1. Parallel In/Out



5.2. MIPI Rx/Tx

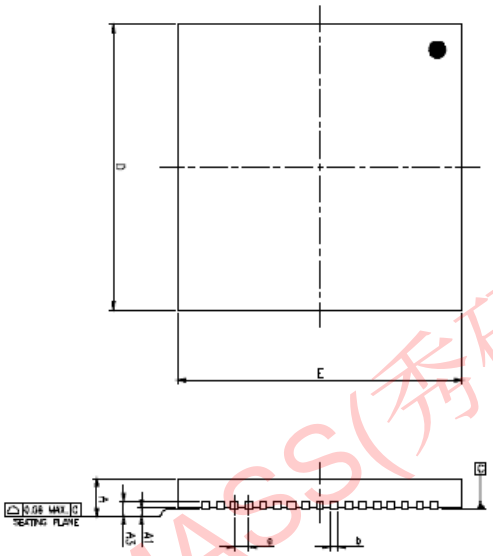


6. Package Specification

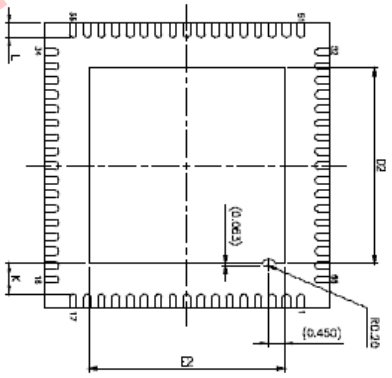
JEDEC OUTLINE	PACKAGE TYPE	
	MO-220	MO-220
PKG CODE	WQFN(XB68)	VQFN(YB68)
SYMBOLS	MIN. NOM. MAX.	MIN. NOM. MAX.
A	0.70 0.75 0.80	0.80 0.85 0.90
A1	0.00 0.02 0.05	0.00 0.02 0.05
A3	0.203 REF.	0.203 REF.
b	0.15 0.20 0.25	0.15 0.20 0.25
D	8.00 BSC	8.00 BSC
E	8.00 BSC	8.00 BSC
e	0.40 BSC	0.40 BSC
L	0.35 0.40 0.45	0.35 0.40 0.45
K	0.20 — —	0.20 — —

PAD SIZE	D2			E2			LEAD FINISH	
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin PPF	JEDEC CODE
185X18* MIL	4.25	4.30	4.35	4.25	4.30	4.35	V X	N/A
236X23* MIL	5.45	5.50	5.55	5.45	5.50	5.55	V X	N/A
252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V X	YLLE-1

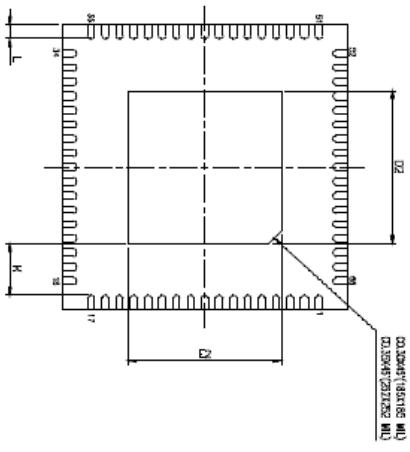
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.



PAD SIZE : 236X23* MIL



PAD SIZE : 185X18* MIL / 252X25* MIL



NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

7. Revision History

Version	Date	Description
0.0	2018/08/13	Initial Release
0.1	2018/08/21	Package Information Updated
0.2	2018/09/19	Application Schematic Updated for VDAC resistance
0.21	2018/10/18	Update Power Dissipation
0.23	2019/03/07	Storage/Operating Temperature Update for Consumer
0.24	2019/04/19	VDDO3 for MIPI Tx Output should be used 3.3V Only. 1.8V is removed in application schematic.
0.25	2019/05/21	VDDI, VDDIM Recommend Voltage Range updated
0.3	2019/12/18	Power Dissipation Update (Table 13, 14)
0.31	2020/04/01	Pin Description update for VDDO3 (P. 12)
0.32	2020/04/14	Recommended Operating Conditions Update (Table 9)
0.33	2020/04/20	Add Operating Temperature (P. 7)
0.34	2020/07/08	Update Operating Temperature for Consumer (P. 7)