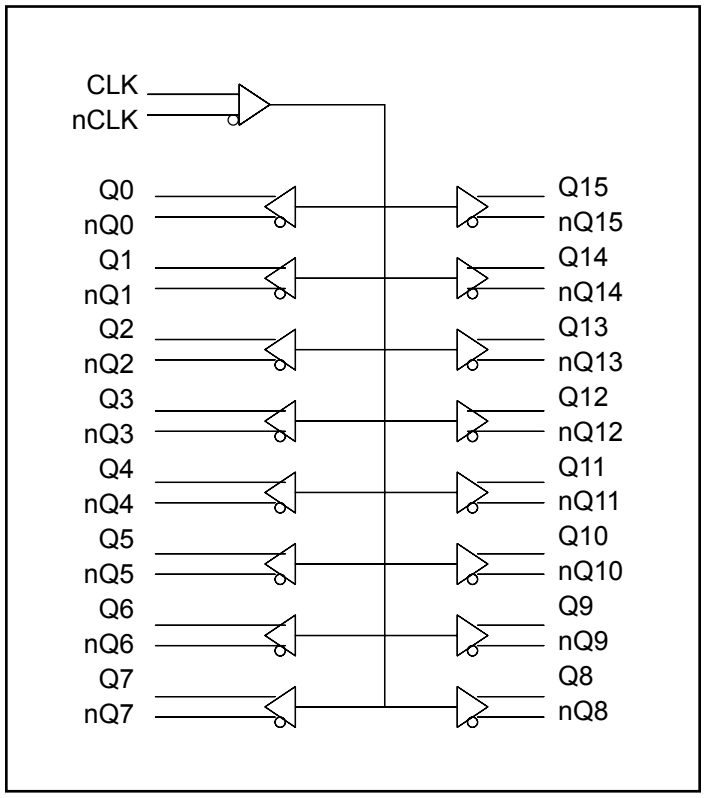
3.3V 1:16 LVPECL Fanout Buffer

Product Features

- Low voltage operation Vcc=3.3V
- 1:16 fanout
- Differential input can accept the following: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Translates any single-ended input signal to 3.3V LVPECL levels with a resistor bias on nCLK input
- Pin-to-pin compatible to ICS8530-01
- Low Output skew: 75ps
- Par-to-part skew: 250ps
- Propagation Delay: 2ns
- Maximum output frequency: 500MHz
- 3.3V output operating supply
- Package available: 48-pin LQFP (FB48)

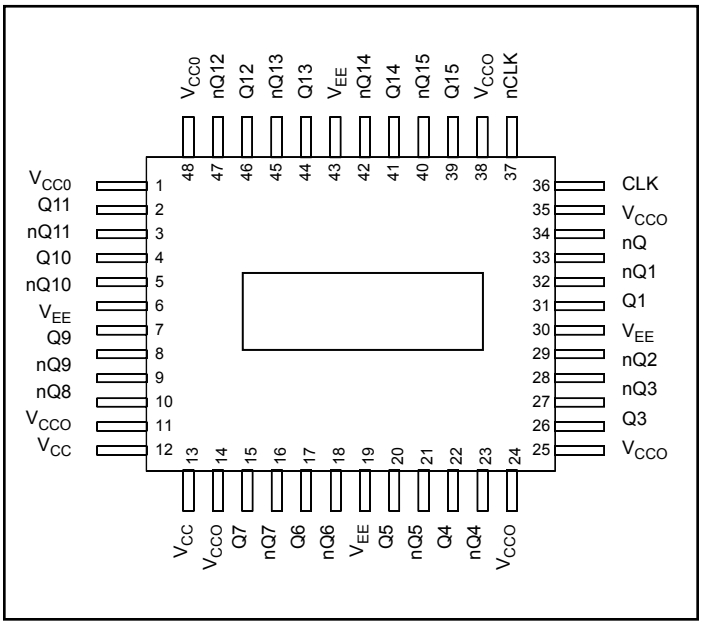
Logic Block Diagram



Product Description

The PI6C48530-01 is a high performance low skew LVPECL fanout buffer. PI6C48530-01 features a single differential LVPECL or LVDS or LVHSTL or SSTL or HCSL input and sixteen 3.3V LVPECL outputs. The input can accept single-ended signal with external bias circuit. The large fanout from a single input line reduces loading on input clock. PI6C48530-01 is ideal for both single-ended to LVPECL translations and/or LVPECL clock distribution. Typical applications are clock and signal distribution for data-communications and telecommunications.

Pin Description



Pin Description

Name	Pin #	Type	Description
V_{CCO}	1, 11, 14, 24, 25, 35, 38, 48	P	Output supply, connect to 3.3V
Qx, nQx	2, 3, 4, 5, 7, 8, 9, 10, 15, 16, 17, 18, 20, 21, 22, 23, 26, 27, 28, 29, 39, 40, 41, 42, 44, 45, 46 ,47	O	Differential output pair, 3.3V LVPECL interface level.
V_{EE}	6, 19, 30, 43	P	Ground, connect to negative supply
V_{CC}	12, 13	P	Core power supply, connect to 3.3V.
CLK	36	I_PD	Non-inverting differential clock input
nCLK	37	I_PU	Inverting differential clock input

Notes: I = Input
O = Output
P = Power supply connection
I_PD = Input with pull down
I_PU = Input with pull up

Pin Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Units
Cin	Input Capacitance				4	pF
R_pullup	Input Pullup Resistance			50		KΩ
R_pulldown	Input Pulldown Resistance			50		KΩ

Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q15	nQ0:nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; Vin=Vcc/2	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; Vin=Vcc/2	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; Vin=Vcc/2	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; Vin=Vcc/2	1	LOW	HIGH	Single Ended to Differential	Inverting

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}, V_{CCO}	Supply voltage	Referenced to GND			4.6	V
V_{IN}	Input voltage	Referenced to GND	-0.5		Vcc+0.5V	V
V_{OUT}	Output voltage	Referenced to GND	-0.5		Vcco+0.5V	V
T_{STG}	Storage temperature		-65		150	^{o}C

Notes:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3	3.3	3.6	V
V_{CCO}	Output Power Supply		3	3.3	3.6	V
T_A	Ambient Temperature		0		70	^{o}C
I_{CC}	Power Supply Current				120	mA

Differential Inputs DC Characteristics

T_A = 0^{o}C to 70^{o}C, V_{CC} = V_{CCO} = 3.0V to 3.6V unless otherwise stated below.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{IH}	Input High Current	nCLK	V_{IN} = V_{CC} = 3.6V			5	uA
		CLK	V_{IN} = V_{CC} = 3.6V			150	
I_{IL}	Input Low Current	nCLK	V_{CC}=3.6V, V_{IN}=0V	-150			
		CLK	V_{CC}=3.6V, V_{IN}=0V	-5			
V_{PP}	Peak-to-peak Voltage	CLK, nCLK		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage(1,2)	CLK, nCLK		V_{EE} + 0.05		V_{CC} - 0.85	

Notes:
1. For single ended applications, the maximum input voltage for CLK and nCLK is Vcc+0.3V
2. Common mode voltage is defined as V_{IH}.

LVPECL DC Characteristics

T_A = 0°C to 70°C, V_{CC} = V_{CCO} = 3.0V to 3.6V unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage(3,4)		V_{CCO} -1.4		V_{CCO} -1.0	V
V_{OL}	Output LOW Voltage(3,4)		V_{CCO} -2.0		V_{CCO} -1.7	
V_{SWING}	Peak-to-peak Output Voltage Swing		0.6		0.85	

Notes:

3. The PI6C48530-01 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket, or mounted on a printed circuit board.
4. Q0:Q15 and nQ0:nQ15 outputs are loaded with 50Ω to V_{CCO}-2V.

AC Characteristics

T_A = 0°C to 70°C, V_{CC} = V_{CCO} = 3.0V to 3.6V unless otherwise stated below.

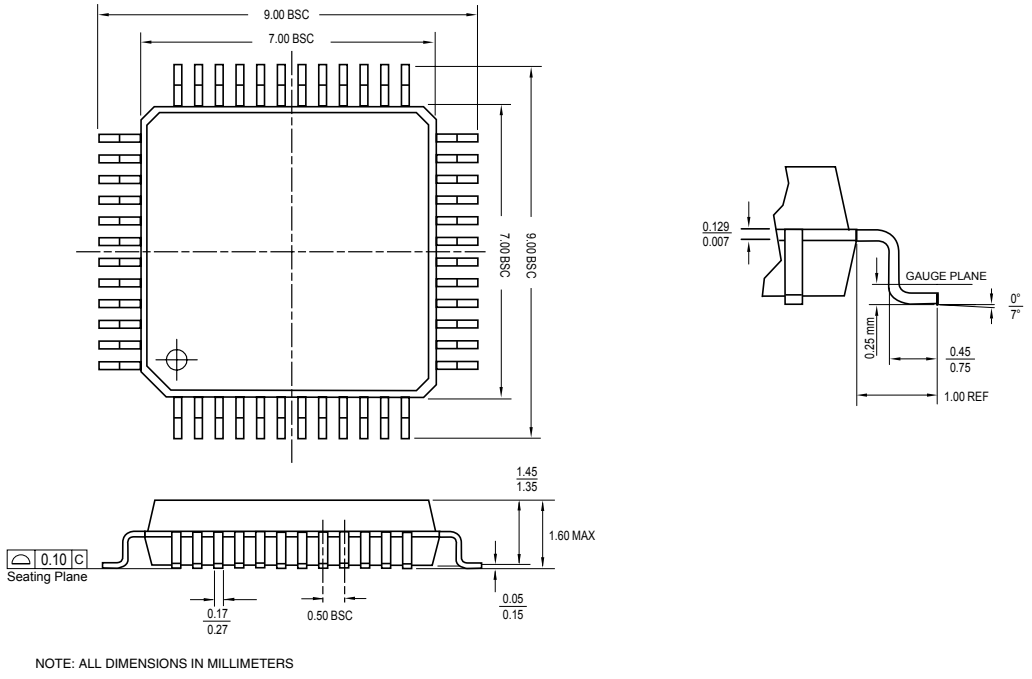
Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency				500	MHz
T_{pd}	Propagation Delay(5)	F ≤ 500MHz	1		2	ns
Tsk(o)	Output-to-output Skew(6,8)				75	ps
Tsk(pp)	Part-to-part Skew(7,8)			88	250	
t_r/t_f	Output Rise/Fall time	20% - 80% @ 50MHz	300		700	
t_{dc}	Output duty cycle		48		52	%

Notes:

All parameters are measured at 250MHz unless noted otherwise

5. Measured from the differential input crossing point to the differential output crossing point
6. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
7. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
8. This parameter is defined in accordance with JEDEC Standard

Package Mechanical: 48-pin LQFP (FB)



Ordering Information:

Ordering Code	Packaging Code	Package Type
PI6C48530-01FB	FB	48 pin LQFP
PI6C48530-01FBE	FB	Pb-free & Green, 48 pin LQFP

Notes:

1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/