

## High Performance 1:5 LVPECL Fanout Buffer

### Features

- 5 LVPECL outputs
- Up to 1.5GHz output frequency
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Two selectable inputs
- Low delay from input to output (Tpd typ. 1.5ns)
- 3.3V power supply
- Industrial temperature support
- TSSOP-20 package

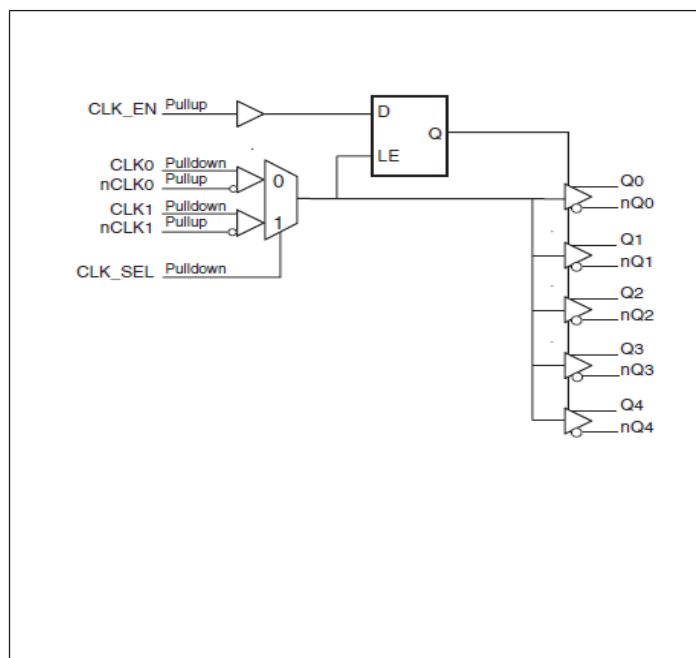
### Description

The PI6C4911505 is a high performance fanout buffer device- which supports up to 1.5GHz frequency. The device has 2 selectable clock inputs that can accept most differential clock sources. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

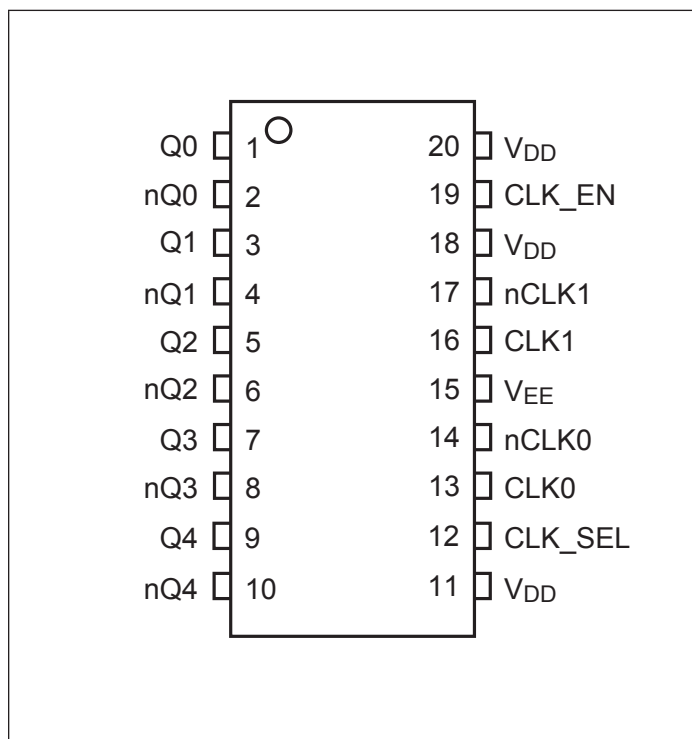
### Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

### Block Diagram



### Pin Configuration (20-Pin TSSOP)



**Pinout Table**

| Pin #      | Pin Name        | Type   |                    | Description                      |
|------------|-----------------|--------|--------------------|----------------------------------|
| 1, 2       | Q0<br>nQ0       | Output |                    | LVPECL output clock              |
| 3, 4       | Q1<br>nQ1       | Output |                    | LVPECL output clock              |
| 5, 6       | Q2<br>nQ2       | Output |                    | LVPECL output clock              |
| 7, 8       | Q3<br>nQ3       | Output |                    | LVPECL output clock              |
| 9, 10      | Q4<br>nQ4       | Output |                    | LVPECL output clock              |
| 11, 18, 20 | V <sub>DD</sub> | Power  |                    | Power supply                     |
| 12         | CLK_SEL         | Input  | Pulldown           | Clock input source selection pin |
| 13, 14     | CLK0<br>nCLK0   | Input  | Pulldown<br>Pullup | Differential clock input         |
| 15         | V <sub>EE</sub> | Power  |                    | Negative power supply            |
| 16, 17     | CLK1<br>nCLK1   | Input  | Pulldown<br>Pullup | Differential clock input         |
| 19         | CLK_EN          | Input  | Pullup             | Clock output enable/ disable     |

**Function Table**

Table 1: Input select function

| CLK_SEL | Function    |
|---------|-------------|
| 0       | CLK0, nCLK0 |
| 1       | CLK1, nCLK1 |

Table 2: Output Mode select function

| CLK_EN | Outputs       |                |
|--------|---------------|----------------|
|        | Q0:Q4         | nQ0:nQ4        |
| 0      | Disabled; LOW | Disabled; HIGH |
| 1      | Enabled       | Enabled        |

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C  
 Supply Voltage to Ground Potential ( $V_{DD}$ )..... -0.5 to +4.6V  
 Inputs (Referenced to GND) ..... -0.5 to  $V_{DD}+0.5V$   
 Clock Output (Referenced to GND)..... -0.5 to  $V_{DD}+0.5V$   
 Soldering Temperature (Max of 10 seconds) .....+260°C  
 Latch up .....200mA

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Power Supply Characteristics and Operating Conditions**

| Symbol   | Parameter                     | Test Condition       | Min.  | Typ. | Max.  | Units |
|----------|-------------------------------|----------------------|-------|------|-------|-------|
| $V_{DD}$ | Core Supply Voltage           |                      | 3.135 | 3.3  | 3.465 | V     |
| $I_{DD}$ | Power Supply Current          | All outputs unloaded |       |      | 160   | mA    |
| $T_A$    | Ambient Operating Temperature |                      | -40   |      | 85    | °C    |

**DC Electrical Specifications - Differential Inputs**

| Symbol   | Parameter                          |                  | Min.      | Typ. | Max.          | Units |
|----------|------------------------------------|------------------|-----------|------|---------------|-------|
| $I_{IH}$ | Input High current: CLK0, CLK1     | Input = $V_{DD}$ |           |      | 200           | uA    |
|          | Input High current: nCLK0, nCLK1   | Input = $V_{DD}$ |           |      | 10            | uA    |
| $I_{IL}$ | Input Low current: CLK0, CLK1      | Input = GND      | -200      |      |               | uA    |
|          | Input Low current: nCLK0, nCLK1    | Input = GND      | -200      |      |               | uA    |
| $C_{IN}$ | Input capacitance                  |                  |           | 4    |               | pF    |
| $V_{ID}$ | Input Differential Amplitude PK-PK |                  | 0.15      |      | $V_{DD}-0.85$ | V     |
| $V_{CM}$ | Common model input voltage         |                  | GND + 0.5 |      | $V_{DD}-0.85$ | V     |

**DC Electrical Specifications - LVCMOS Inputs**

| Symbol          | Parameter          | Conditions              | Min. | Typ. | Max.                 | Units |
|-----------------|--------------------|-------------------------|------|------|----------------------|-------|
| I <sub>IH</sub> | Input High current | Input = V <sub>DD</sub> |      |      | 200                  | uA    |
| I <sub>IL</sub> | Input Low current  | Input = GND             | -200 |      |                      | uA    |
| V <sub>IH</sub> | Input high voltage | V <sub>DD</sub> =3.3V   | 2.0  |      | V <sub>DD</sub> +0.3 | V     |
| V <sub>IL</sub> | Input low voltage  | V <sub>DD</sub> =3.3V   | -0.3 |      | 0.8                  | V     |

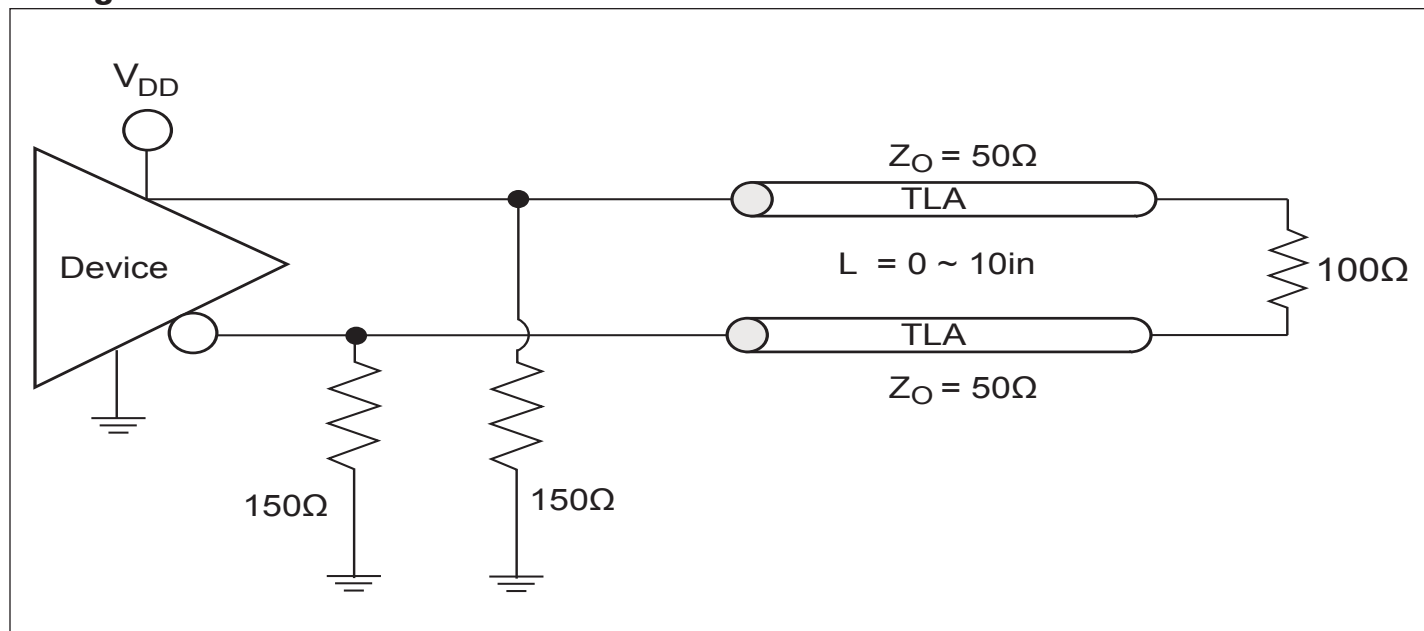
**DC Electrical Specifications- LVPECL Outputs**

| Parameter       | Description         | Conditions            | Min. | Typ. | Max. | Units |
|-----------------|---------------------|-----------------------|------|------|------|-------|
| V <sub>OH</sub> | Output High voltage | V <sub>DD</sub> =3.3V | 2.1  |      | 2.6  | V     |
| V <sub>OL</sub> | Output Low voltage  | V <sub>DD</sub> =3.3V | 1.3  |      | 1.8  | V     |

**AC Electrical Specifications**

| Parameter        | Description                | Conditions                                                       | Min. | Typ. | Max. | Units |
|------------------|----------------------------|------------------------------------------------------------------|------|------|------|-------|
| F <sub>OUT</sub> | Clock output frequency     | LVPECL                                                           |      |      | 1500 | MHz   |
| T <sub>r</sub>   | Output rise time           | From 20% to 80%                                                  |      | 150  |      | ps    |
| T <sub>f</sub>   | Output fall time           | From 80% to 20%                                                  |      | 150  |      | ps    |
| T <sub>ODC</sub> | Output duty cycle          | Frequency<650MHz                                                 | 48   |      | 52   | %     |
| V <sub>PP</sub>  | Output swing Single-ended  | LVPECL outputs                                                   | 400  |      |      | mV    |
| T <sub>j</sub>   | Buffer additive jitter RMS |                                                                  |      | 0.03 |      | ps    |
| T <sub>SK</sub>  | Output Skew                | 5 outputs devices, outputs in same bank, with same load, at DUT. |      | 40   |      | ps    |
| T <sub>PD</sub>  | Propagation Delay          |                                                                  |      | 1500 |      | ps    |

## Configuration Test Load Board Termination for LVPECL



## Application Information

### Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3\text{V}$ ,  $V_{REF}$  should be 1.25V and  $R1/R2 = 0.609$ .

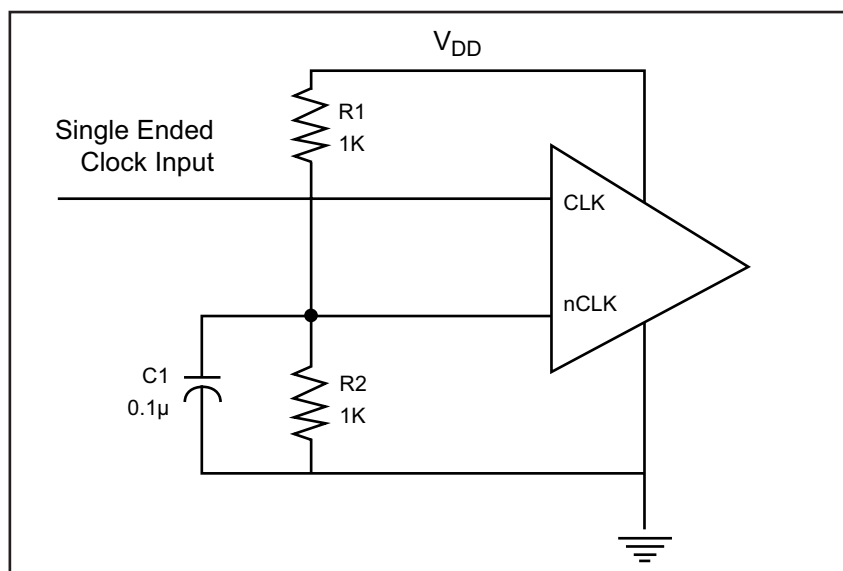
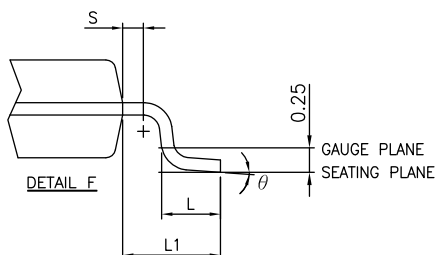
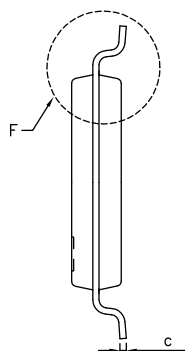
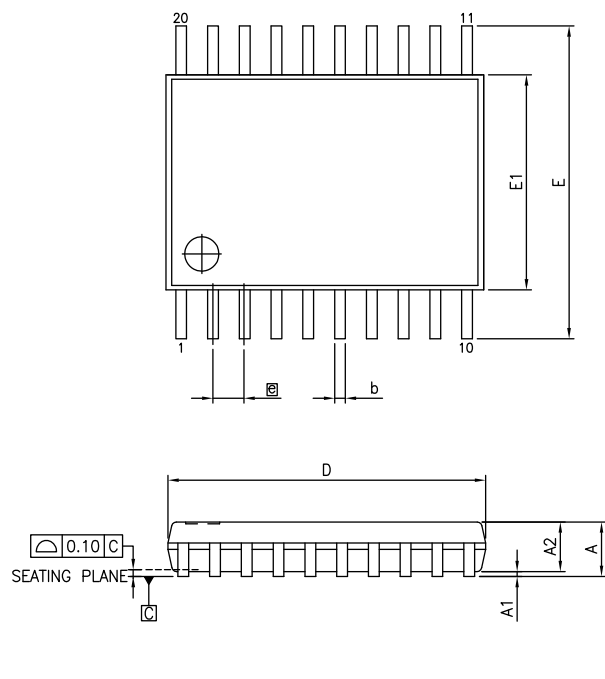


Figure 1. Single-ended input to Differential input device

## Packaging Mechanical: 20-Pin TSSOP (L)

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS  | MIN.     | NOM. | MAX. |
|----------|----------|------|------|
| A        | —        | —    | 1.20 |
| A1       | 0.05     | —    | 0.15 |
| A2       | 0.80     | —    | 1.05 |
| b        | 0.19     | —    | 0.30 |
| C        | 0.09     | —    | 0.20 |
| D        | 6.40     | 6.50 | 6.60 |
| E1       | 4.30     | 4.40 | 4.50 |
| E        | 6.40 BSC |      |      |
| e        | 0.65 BSC |      |      |
| L1       | 1.00 REF |      |      |
| L        | 0.45     | 0.60 | 0.75 |
| S        | 0.20     | —    | —    |
| $\theta$ | 0°       | —    | 8°   |



- Notes:**
- 1. Refer JEDEC MO-153F/AC
  - 2. Controlling dimensions in millimeters
  - 3. Package outline exclusive of mold flash and metal burr



DATE: 05/03/12

DESCRIPTION: 20-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1311

REVISION: F

## Ordering Information<sup>(1-3)</sup>

| Ordering Code  | Package Code | Package Description              |
|----------------|--------------|----------------------------------|
| PI6C4911505LIE | L            | 20-pin, TSSOP, Pb-Free and Green |

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel