

**High Performance 1:8 Multi-Voltage CMOS Buffer**

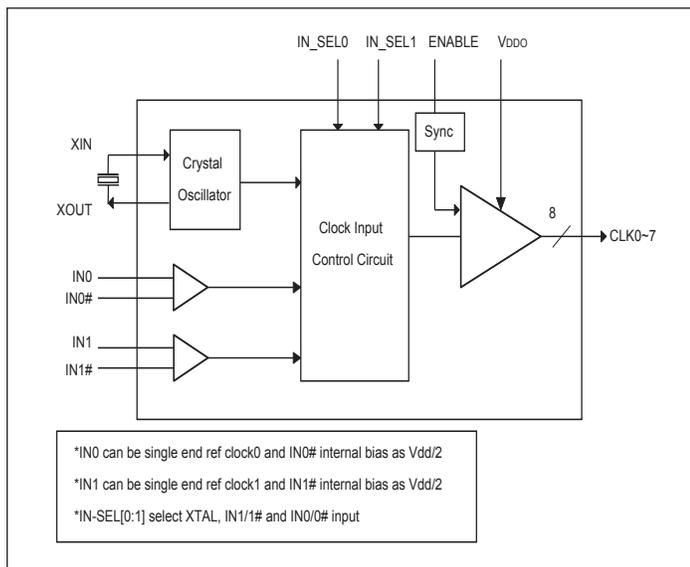
**Description**

The DIODES PI6C49X0208 is a high performance multi-voltage 8-outputs CMOS Fanout Buffer with internal Crystal Oscillator. The XTAL range is from 10MHz to 50MHz. The device has a wide range of operating voltages of 2.5V and 3.3V. The device also provides user selectable output VDD option, which provides excellent flexibility to users. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

**Application(s)**

- Networking systems including switches and routers
- High frequency backplanes based computing and telecom platforms

**Block Diagram**



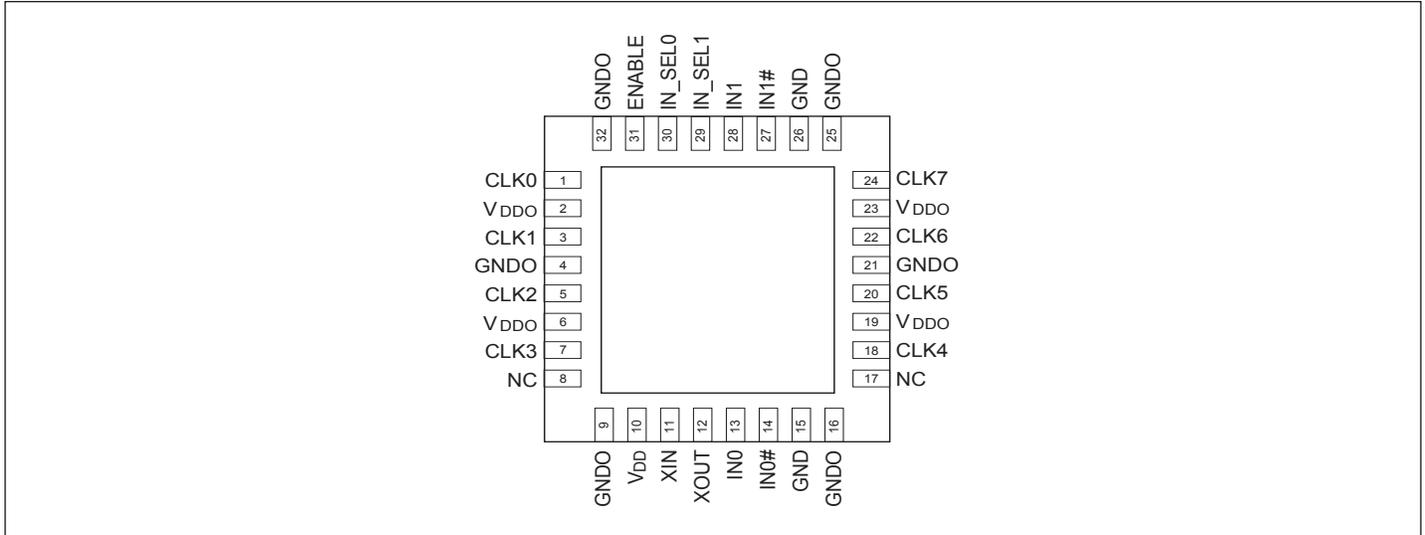
**Features**

- 8 single-ended outputs fanout buffer
- Up to 200MHz output frequency
- Ultra low output additive jitter = 0.01ps (typical)
- Selectable reference inputs support Xtal (10~50MHz), single-ended and differential
- Low output skew ~ 50ps (typical)
- 2.5V/3.3V operation
- User configurable output VDDO in different banks:
  - Mixed 3.3V core, 2.5V, 1.8V or 1.5V output operating supply
  - Mixed 2.5V core, 1.8V, 1.5V or 1.2V output operating supply
- Industrial temperature range: -40°C to +85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.
- Packaging (Pb-free & Green):
  - 32-Pin, W-QFN5050 (ZH)

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration



## Pin Description

Pin#	Pin Name	Type	Description
1, 3, 5, 7, 18, 20, 22, 24	CLK0~7	Output	Clock Outputs
2, 6, 19, 23	V <sub>DDO</sub>	Power	Output Power Supplier
4, 9, 16, 21, 25, 32	GNDO	Power	Core Ground
8, 17	NC		Not Connected
15, 26	GND	Power	Output Ground
10	V <sub>DD</sub>	Power	Core Power Supplier
11	XIN	Input	Crystal Interface
12	XOUT	Output	Crystal Interface
13	IN0	Input	Pull-down Differential or Single End
14	IN0#	Input	Pull-up/ Pull-down When IN0 is single end IN0# internal bias as V <sub>dd</sub> /2
27	IN1#	Input	Pull-up/ Pull-down When IN1 is single end IN1# internal bias as V <sub>dd</sub> /2
28	IN1	Input	Pull-down REF1 Differential or Single End
30, 29	IN_SEL[0:1]	Input	Pull-down IN-SEL[0:1] select XTAL, IN1/1# and IN0/IN0# input, trigger level is V <sub>dd</sub> /2
31	ENABLE	Input	Synchronous Active High Output Enable, LVCMOS/TTL

### Input Mode Selection Logic

IN_SEL0	IN_SEL1	Selected Input
1	1	XTAL
0	1	XTAL
1	0	IN1/1# Differential or Single End
0	0	IN0/0# Differential or Single End

### Input/Output Operation State

Input State	Output State
IN[0:1], IN[0:1]# open	Logic Low
IN[0:1], IN[0:1]# both to ground	Logic Low
IN[0:1]=High, IN[0:1]# =Low	Logic High
IN[0:1]=Low, IN[0:1]# =High	Logic Low

### Output Mode Selection

ENABLE	Output CLK0~7
GND	High-impedance
VDD	Enabled

## Power Supply DC Characteristics

$V_{DD}/V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			32	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			1	mA

$V_{DD}/V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			15	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.7	mA

$V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			29	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.6	mA

$V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			29	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.4	mA

$V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.5V \pm 0.15V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.35	1.5	1.65	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			29	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.3	mA

$V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			13	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.4	mA

$V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.5V \pm 0.15V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ 

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		1.35	1.5	1.65	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			13	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.3	mA

 $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.2V \pm 0.06V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ 

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		1.14	1.2	1.26	V
$I_{DD}$	Power Supply Current	ENABLE = '0'			13	mA
$I_{DDO}$	Output Supply Current	ENABLE = '0'			0.3	mA

## Single-Ended Input DC Characteristics

 $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ 

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V \pm 5\%$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V \pm 5\%$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V \pm 5\%$	-0.3		0.8	V
		$V_{DD} = 2.5V \pm 5\%$	-0.3		0.7	V
$V_{OH}$	Output High Voltage ( $I_{OH} = -8\text{mA}$ )	$V_{DDO} = 3.3V \pm 5\%$ <sup>(1)</sup>	2.6			V
		$V_{DDO} = 2.5V \pm 5\%$	2			V
		$V_{DDO} = 2.5V \pm 5\%$ <sup>(1)</sup>	1.8			V
		$V_{DDO} = 1.8V \pm 0.2V$ <sup>(1)</sup>	1.5			V
		$V_{DDO} = 1.5V \pm 0.15V$ <sup>(1)</sup>	1.0			V
	Output High Voltage ( $I_{OH} = -1\text{mA}$ )	$V_{DDO} = 1.2V \pm 0.06V$	0.7			V
$V_{OL}$	Output Low Voltage ( $I_{OL} = 8\text{mA}$ )	$V_{DDO} = 3.3V \pm 5\%$ <sup>(1)</sup>	2.6			V
		$V_{DDO} = 2.5V \pm 5\%$			0.5	V
		$V_{DDO} = 1.8V \pm 0.2V$ <sup>(1)</sup>			0.4	V
		$V_{DDO} = 1.5V \pm 0.15V$ <sup>(1)</sup>			0.35	V
	Output Low Voltage ( $I_{OH} = 1\text{mA}$ )	$V_{DDO} = 1.2V \pm 0.06V$			0.2	V

**Notes:**

 1. Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement section, "Load Test Circuit" diagrams.

## Differential Input DC Characteristics

$T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$I_{IH}$	Input High Current IN[0:1], IN[0:1]#	$V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			100	$\mu\text{A}$
$I_{IL}$	Input Low Current IN[0:1] IN[0:1]#	$V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ $V_{IN} = 0\text{V}$	-1			$\mu\text{A}$
		$V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ $V_{IN} = 0\text{V}$	-50			$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Input Voltage <sup>(1)</sup>	$V_{DD} = 3.3\text{V}$	0.25		1.3	V
		$V_{DD} = 2.5\text{V}$	0.25		1.3	
$V_{CMR}$	Common Mode Input Voltage <sup>(1,2)</sup>	$V_{DD} = 3.3\text{V}$	0.5		$V_{DD} - 1.35\text{V}$	V
		$V_{DD} = 2.5\text{V}$	0.5		$V_{DD} - 0.85\text{V}$	

**Notes:**

- $V_{IL}$  should not be less than  $-0.3\text{V}$ .
- Common mode voltage is defined as  $1/2(V_{IH} - V_{IL})$ .

### 3.3V Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C
V <sub>DD</sub> , V <sub>DDO</sub> Voltage.....	-0.5V to +3.6V
Output Voltage .....	-0.5V to V <sub>DD</sub> +0.5V
Input Voltage .....	-0.5V to V <sub>DD</sub> +0.5V

**Note:**  
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### AC Characteristics

Over Operating Range: V<sub>DD</sub>/V<sub>DDO</sub> = 3.3V ± 5%, T<sub>A</sub> = -40° to 85°C

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source <sup>(2)</sup>	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>				80	ps
t <sub>jit(Ø)</sub>	RMS Phase Jitter (Random)	25MHz crystal @ (Integration Range: 100Hz-1MHz)		0.05		ps
t <sub>jit(additive)</sub>	Additive RMS Phase Jitter (Random)	125MHz reference input @ (Integration Range: 12kHz-20MHz)		0.01		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time	20% to 80%	200		800	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>				5	cycles
MUX <sub>isolation</sub>	MUX Isolation	155.52MHz		64		dB

**Notes:**

1. Unless noted otherwise, all parameters are tested with xtal @ f ≤ Fxtal\_max,; outputs are terminated @ 50Ω to V<sub>DDO</sub>/2, see waveforms.
2. Differential external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as V<sub>DD</sub>/2
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

## 2.5V Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C	<b>Note:</b> Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
V <sub>DD</sub> , V <sub>DDO</sub> Voltage.....	-0.5V to +3.6V	
Output Voltage.....	-0.5V to V <sub>DD</sub> +0.5V	
Input Voltage.....	-0.5V to V <sub>DD</sub> +0.5V	

## AC Characteristics

Over Operating Range: V<sub>DD</sub>/V<sub>DDO</sub> = 2.5V ± 5%, T<sub>A</sub> = -40° to 85°C

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source <sup>(2)</sup>	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>				80	ps
t <sub>jit(Ø)</sub>	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.06		ps
t <sub>jit(additive)</sub>	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time	20% to 80%	200		800	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>				5	cycles
MUX <sub>isolation</sub>	MUX Isolation	155.52MHz		63		dB

**Notes:**

1. Unless noted otherwise, all parameters are tested with xtal @ f <= Fxtal\_max.; outputs are terminated @ 50Ω to V<sub>DDO</sub>/2, see waveforms.
2. Differential external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as V<sub>DD</sub>/2
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

## AC Characteristics

Over Operating Range:  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ$  to  $85^\circ\text{C}$

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
$f_{MAX}$	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source <sup>(2)</sup>	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
$t_{sk(o)}$	Output Skew <sup>(3)</sup>				80	ps
$t_{jit(\emptyset)}$	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.05		ps
$t_{jit(Additive)}$	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
$t_R/t_F$	Output Rise/Fall Time	20% to 80%	200		800	ps
$t_{EN}$	Output Enable Time <sup>(4)</sup>				5	cycles
$t_{DIS}$	Output Disable Time <sup>(4)</sup>				5	cycles
$MUX_{isolation}$	MUX Isolation	155.52MHz		62		dB

### Notes:

1. Unless noted otherwise, all parameters are tested with  $x_{tal} @ f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Differential external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

## AC Characteristics

Over Operating Range:  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ$  to  $85^\circ\text{C}$

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
$f_{MAX}$	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source <sup>(2)</sup>	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
$t_{sk(o)}$	Output Skew <sup>(3)</sup>				80	ps
$t_{jit(\emptyset)}$	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.06		ps
$t_{jit(Additive)}$	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
$t_R/t_F$	Output Rise/Fall Time	20% to 80%	200		900	ps
$t_{EN}$	Output Enable Time <sup>(4)</sup>				5	cycles
$t_{DIS}$	Output Disable Time <sup>(4)</sup>				5	cycles
$MUX_{isolation}$	MUX Isolation	155.52MHz		58		dB

### Notes:

1. Unless noted otherwise, all parameters are tested with  $x_{tal} @ f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Differential external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

## AC Characteristics

Over Operating Range:  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.5V \pm 0.15V$ ,  $T_A = -40^\circ$  to  $85^\circ C$

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
$f_{MAX}$	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source <sup>(2)</sup>	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
$t_{sk(o)}$	Output Skew <sup>(3)</sup>				80	ps
$t_{jit(\emptyset)}$	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.07		ps
$t_{jit(Additive)}$	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
$t_R/t_F$	Output Rise/Fall Time	20% to 80%	200		900	ps
$t_{EN}$	Output Enable Time <sup>(4)</sup>				5	cycles
$t_{DIS}$	Output Disable Time <sup>(4)</sup>				5	cycles
$MUX_{isolation}$	MUX Isolation	155.52MHz		53		dB

### Notes:

1. Unless noted otherwise, all parameters are tested with  $x_{tal}$  @  $f \leq f_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Differential external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

## AC Characteristics

Over Operating Range:  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ$  to  $85^\circ C$

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
$f_{MAX}$	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source <sup>(2)</sup>	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
$t_{sk(o)}$	Output Skew <sup>(3)</sup>				80	ps
$t_{jit(\emptyset)}$	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.06		ps
$t_{jit(Additive)}$	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
$t_R/t_F$	Output Rise/Fall Time	20% to 80%	200		900	ps
$t_{EN}$	Output Enable Time <sup>(4)</sup>				5	cycles
$t_{DIS}$	Output Disable Time <sup>(4)</sup>				5	cycles
$MUX_{isolation}$	MUX Isolation	155.52MHz		59		dB

### Notes:

1. Unless noted otherwise, all parameters are tested with  $x_{tal}$  @  $f \leq f_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Differential external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

## AC Characteristics

 Over Operating Range:  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.5V \pm 0.15V$ ,  $T_A = -40^\circ$  to  $85^\circ C$ 

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source <sup>(2)</sup>	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>				80	ps
t <sub>jit(Ø)</sub>	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.08		ps
t <sub>jit(additive)</sub>	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time	20% to 80%	200		900	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>				5	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>				5	cycles
MUX <sub>isolation</sub>	MUX Isolation	155.52MHz		55		dB

**Notes:**

1. Unless noted otherwise, all parameters are tested with  $x_{tal} @ f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Differential external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

## AC Characteristics

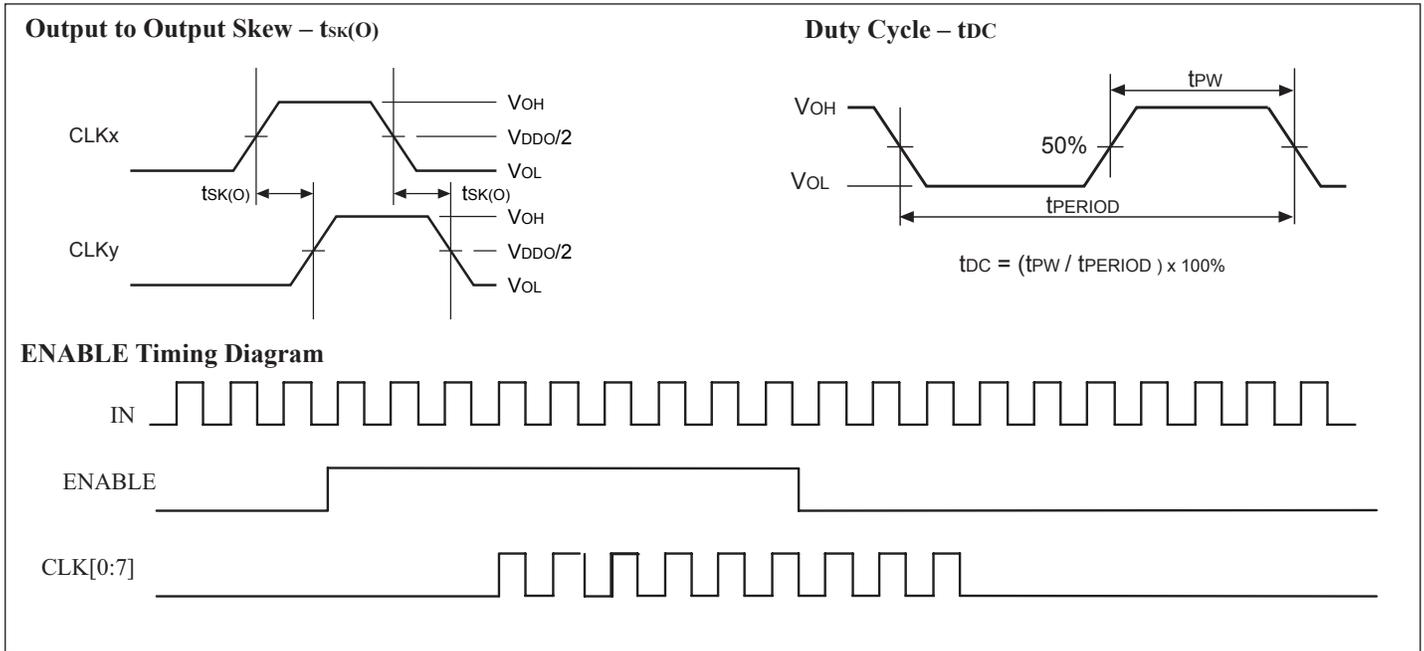
 Over Operating Range:  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.2V \pm 0.06V$ ,  $T_A = -40^\circ$  to  $85^\circ C$ 

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ	Max.	Units
f <sub>MAX</sub>	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source <sup>(2)</sup>	DC		125	
odc	Output Duty Cycle	125MHz, 5pF load	40		60	%
t <sub>sk(o)</sub>	Output Skew <sup>(3)</sup>				60	ps
t <sub>jit(Ø)</sub>	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.13		ps
t <sub>jit(additive)</sub>	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t <sub>R</sub> /t <sub>F</sub>	Output Rise/Fall Time	20% to 80%		1000	1900	ps
t <sub>EN</sub>	Output Enable Time <sup>(4)</sup>				6	cycles
t <sub>DIS</sub>	Output Disable Time <sup>(4)</sup>				6	cycles
MUX <sub>isolation</sub>	MUX Isolation	150MHz		72		dB

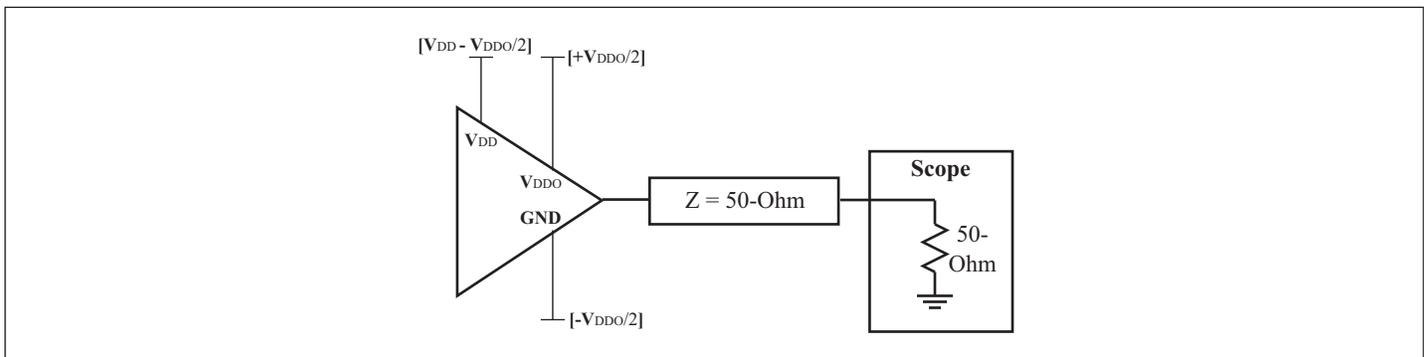
**Notes:**

1. Unless noted otherwise, all parameters are tested with  $x_{tal} @ f \leq F_{xtal\_max}$ ; outputs are terminated @  $50\Omega$  to  $V_{DDO}/2$ , see waveforms.
2. Differential external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as  $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 6 cycles. Min. setup time = 3ns.

**Waveforms**



**AC Test Circuit Load**



**Crystal Characteristic**

(link to "<https://www.diodes.com/products/connectivity-and-timing/crystal-and-crystal-oscillator/xtals-crystals/>" for more detailed and different size crystal specifications)

Parameters	Description	Min	Typ	Max.	Units
OSCMODE	Mode of Oscillation	Fundamental			
FREQ	Frequency	10	25	50	MHz
ESR <sup>(1)</sup>	Equivalent Series Resistance	30		50	$\Omega$
CLOAD	Load Capacitance		18		pF
CSHUNT	Shunt Capacitance			7	pF
DRIVE level				1	mW

**Note:**

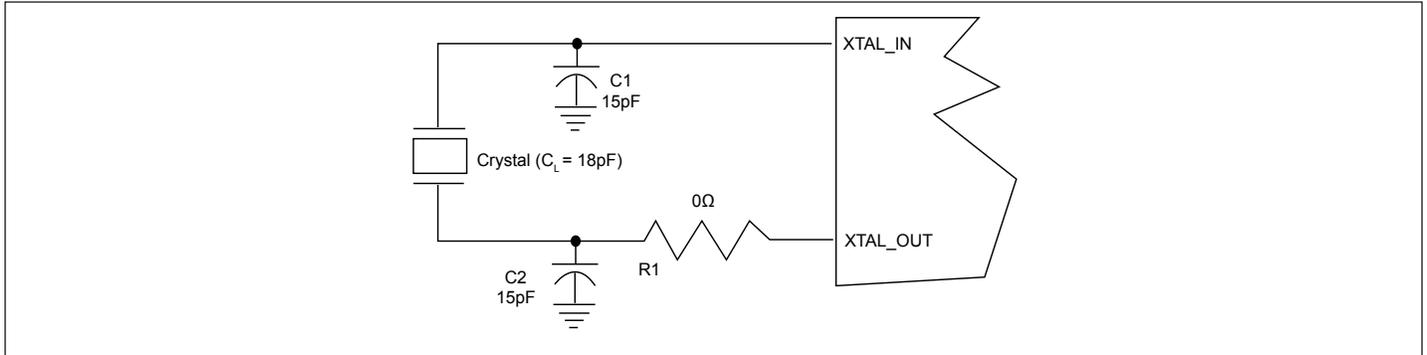
- ESR value is dependent upon frequency of oscillation

## Application Notes

### Crystal Circuit Connection

The following diagram shows PI6C49X0208 crystal circuit connection with a parallel crystal. For the  $C_L=18\text{pF}$  crystal, it is suggested to use  $C1=18\text{pF}$ ,  $C2=18\text{pF}$ .  $C1$  and  $C2$  can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.  $R1$  is not recommended.

### Crystal Oscillator Circuit



## Part Marking

PI6C49X  
0208ZHIE  
YYWWXX  
○

YY: Date Code (Year)  
WW: Date Code (Workweek)  
1st X: Assembly Site Code  
2nd X: Fab Site Code

**Packaging Mechanical**

**32-WQFN (ZH)**

SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.50 BSC		
L	0.35	0.40	0.45
D2	3.15	3.25	3.35
E2	3.15	3.25	3.35

**NOTE :**

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

**DATE: 05/25/23**

**DESCRIPTION: W-QFN5050-32**

**PACKAGE CODE: ZH (ZH32)**

**DOCUMENT CONTROL #: PD-2070** **REVISION: D**

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

Ordering Code	Package Code	Package Description
PI6C49X0208ZHIEX	ZH	W-QFN5050-32

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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