A product Line of
Diodes Incorporated

PI6C5912006

6 Output LVPECL Fanout Buffer

Features

- 6 differential LVPECL outputs
- 2 selectable reference inputs support either single-ended or differential
- Up to 2GHz output frequency
- Ultra low additive phase jitter: < 0.01 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Low skew between outputs
- Low delay from input to output (Tpd typ. < 0.7ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Package: TQFN-32 (ZH)

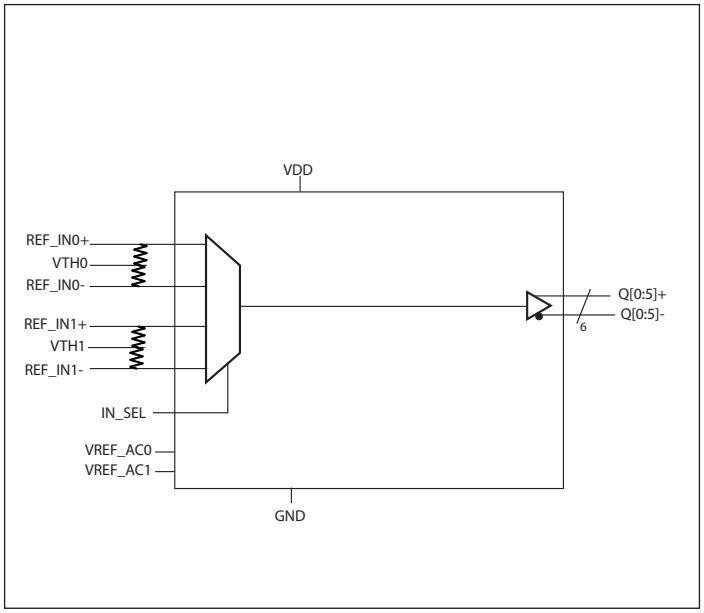
Description

The PI6C5912006 is a high performance LVPECL fanout buffer device which supports up to 2GHz frequency. This device is ideal for systems that need to distribute low jitter LVPECL clock signals to multiple destinations.

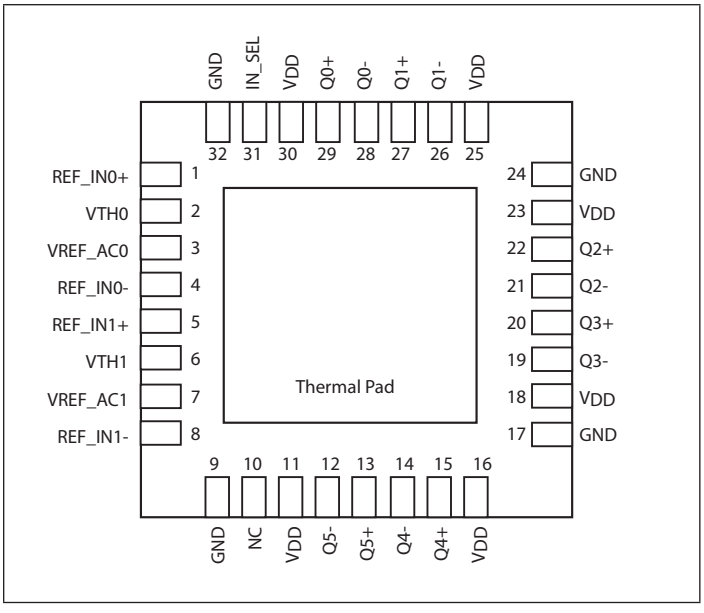
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (32-Pin TQFN)



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Description

Pin #	Pin Name	Type		Description
1, 4	REF_IN0+ REF_IN0-	Input		Reference input 0. Accepts Differential or Single Ended inputs
2	VTH0	Input		Input Termintaion Center Tap for REF_IN0. Internal 50Ω termination
3	VREF_AC0	Output		Bias voltage output.
5, 8	REF_IN1+ REF_IN1-	Input		Reference input 1. Accepts Differential or Single Ended inputs
6	VTH1	Input		Input Termintaion Center Tap for REF_IN0. Internal 50Ω termination
7	VREF_AC1	Output		Bias voltage output.
9, 17, 24, 32	GND	Power		Power supply ground
10	NC	-		No Connect
11, 16, 18, 23, 25, 30	VDD	Power		Core power supply
12, 13	Q5- Q5+	Output		LVPECL output pair 5.
14, 15	Q4- Q4+	Output		LVPECL output pair 4.
19, 20	Q3- Q3+	Output		LVPECL output pair 3.
21, 22	Q2- Q2+	Output		LVPECL output pair 2.
26, 27	Q1- Q1+	Output		LVPECL output pair 1.
28, 29	Q0- Q0+	Output		LVPECL output pair 0.
31	IN_SEL	Input	Pullup	Input clock select. See Table 1 for function. LVCMOS/LVTTL interface levels.

Function Table

Table 1: Input select function

IN_SEL	Function
0	REF_IN0 is the selected reference input
1 (default)	REF_IN1 is the selected reference input

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
C_{IN}	Input Capcitance			2		pF
R_{PULLUP}	Input Pullup Resistor			25		kΩ

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
Supply Voltage to Ground Potential ($V_{DD,}$ V_{DDO})... -0.5 to +4.6V
Inputs (Referenced to GND) ..... -0.5 to V_{DD}+0.5V
Clock Output (Referenced to GND)..... -0.5 to V_{DD}+0.5V
Latch up 200mA
ESD Protection (Input) .....2000 V min (HBM)
ESD Protection (Input) ..... 1000 V min (CDM)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Core Power Supply Current	All LVPECL outputs unloaded			105	mA
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - Differential Inputs

Symbol	Parameter		Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			20	uA
I_{IL}	Input Low current	Input = GND	-20			uA
V_{IH}	Input high voltage				V_{DD}+0.3	V
V_{IL}	Input low voltage		-0.3			V
V_{ID}	Input Differential Amplitude PK-PK		0.1			V
V_{CM}	Common model input voltage		GND + 0.5		V_{DD}-0.85	V
ISO_{MUX}	MUX isolation			-89		dBc

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
V_{IH}	Input high voltage	V_{DD}=3.3V	2.0		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=3.3V	-0.3		0.8	V
V_{IH}	Input high voltage	V_{DD}=2.5V	1.7		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=2.5V	-0.3		0.7	V

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		V_{DDO}-1.4		V_{DDO}-0.9	V
V_{OL}	Output Low voltage	V_{DD}=2.5V	V_{DDO}-1.95		V_{DDO}-1.25	V
		V_{DD}=3.3V	V_{DDO}-2.2		V_{DDO}-1.25	V

AC Electrical Specifications – Differential Inputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{IN}	Clock input frequency				2000	MHz
V_{INPP}	Differential Input peak to peak voltage	1.5GHz ≤ F_{IN} ≤ 2 GHz	0.2		1.5	V
		F_{IN} ≤ 1.5 GHz	0.1		1.5	V
ER	Input Edge Rate		1.5			V/ns

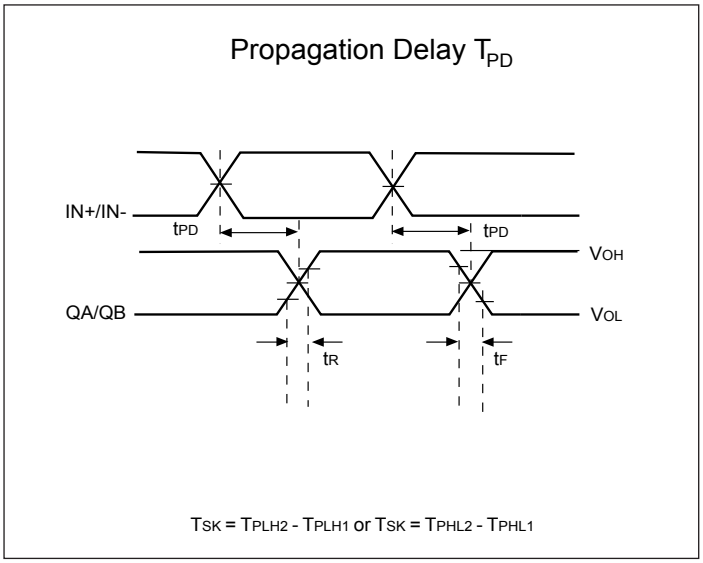
AC Electrical Specifications – LVCMOS Inputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{IN}	Clock input frequency				200	MHz
V_{INPP}	Differential Input peak to peak voltage	1.5GHz ≤ F_{IN} ≤ 2 GHz	0.2		1.5	V
		F_{IN} ≤ 1.5 GHz	0.1		1.5	V
ER	Input Edge Rate		1.5			V/ns

AC Electrical Specifications – LVPECL Outputs

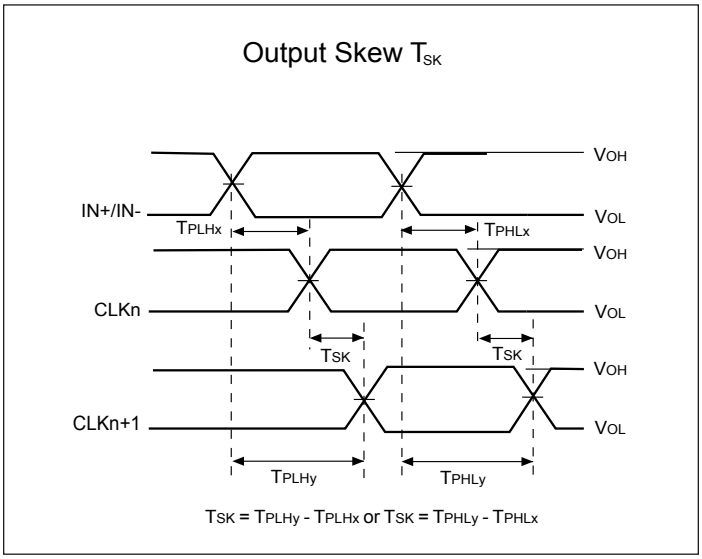
Parameter	Description	Conditions		Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL				2000	MHz
T_r	Output rise time	From 20% to 80%			150		ps
T_f	Output fall time	From 80% to 20%			150		ps
T_{ODC}	Output duty cycle			48		52	%
V_{PP}	Output swing Single-ended	1GHz < F_{IN} ≤ 2 GHz		0.25		0.85	V
		F_{IN} ≤ 1 GHz		0.5		0.95	V
T_j	Buffer additive jitter RMS	156.25MHz, 12kHz to 20MHz			0.01		ps
		156.25MHz, 10kHz to 1MHz			0.01		ps
T_{SK}	Output Skew				13	30	ps
T_{PD}	Propagation Delay				620	700	ps
T_{OD}	Valid to HiZ					100	ns
T_{OE}	HiZ to valid					100	ns
$T_{P2P\ Skew}$	Part to Part Skew[1]			-50		50	ps
V_{REF_AC}	Input bias voltage	I_{AC} = 2mA		V_{DD}-1.6		V_{DD}-1.1	V

Propagation Delay



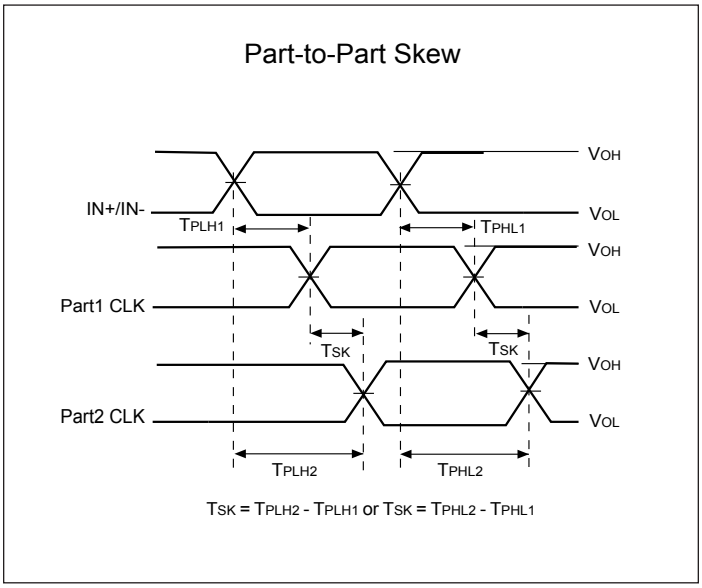
$T_{SK} = T_{PLH2} - T_{PLH1}$ or $T_{SK} = T_{PHL2} - T_{PHL1}$

Output Skew



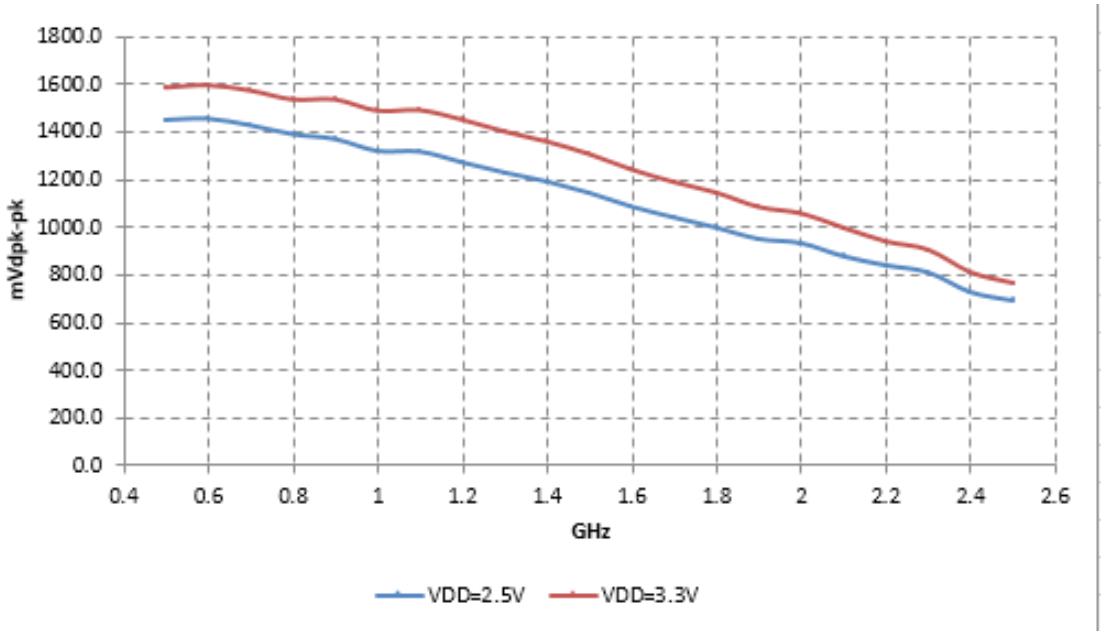
$T_{SK} = T_{PLHy} - T_{PLHx}$ or $T_{SK} = T_{PHLy} - T_{PHLx}$

Part to Part Skew



$T_{SK} = T_{PLH2} - T_{PLH1}$ or $T_{SK} = T_{PHL2} - T_{PHL1}$

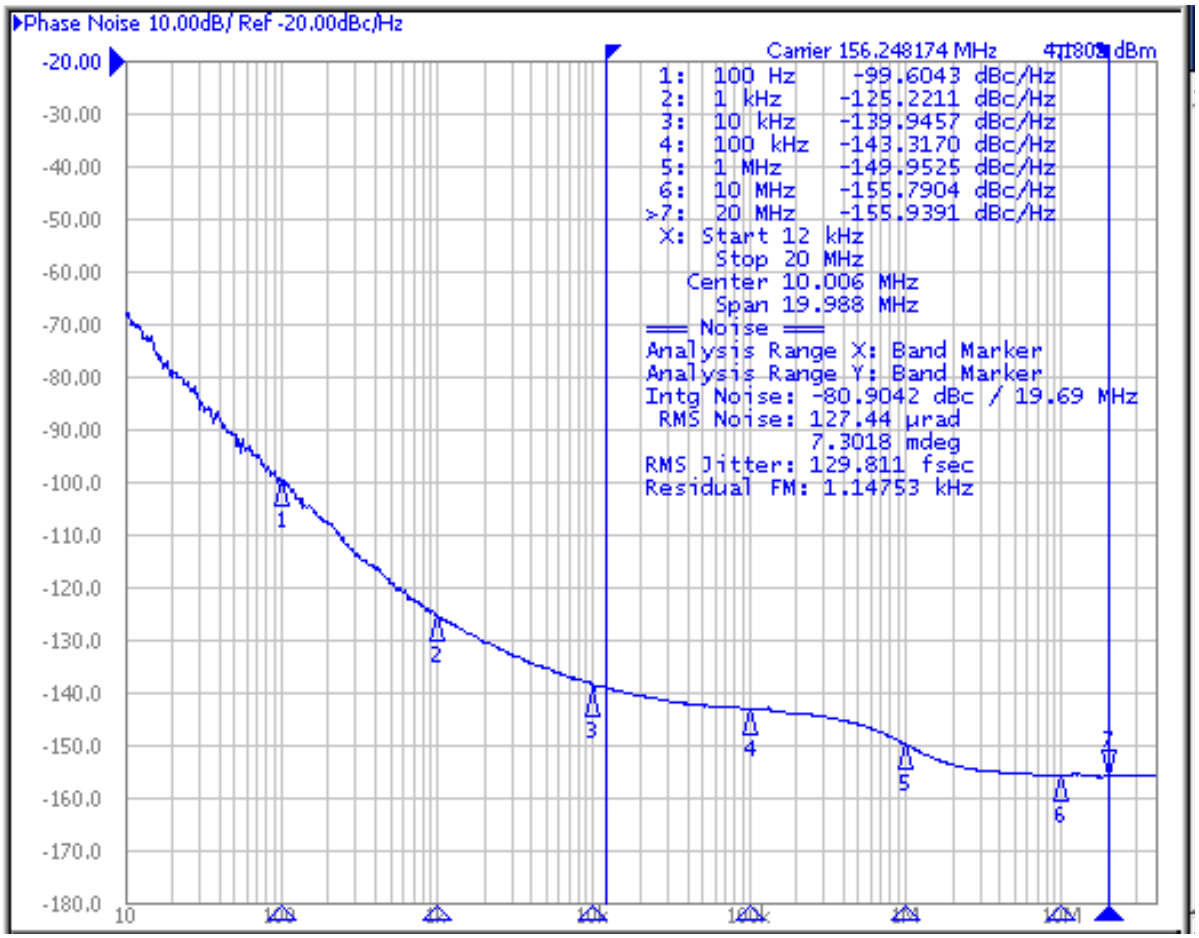
LVPECL Output Swing vs. Frequency



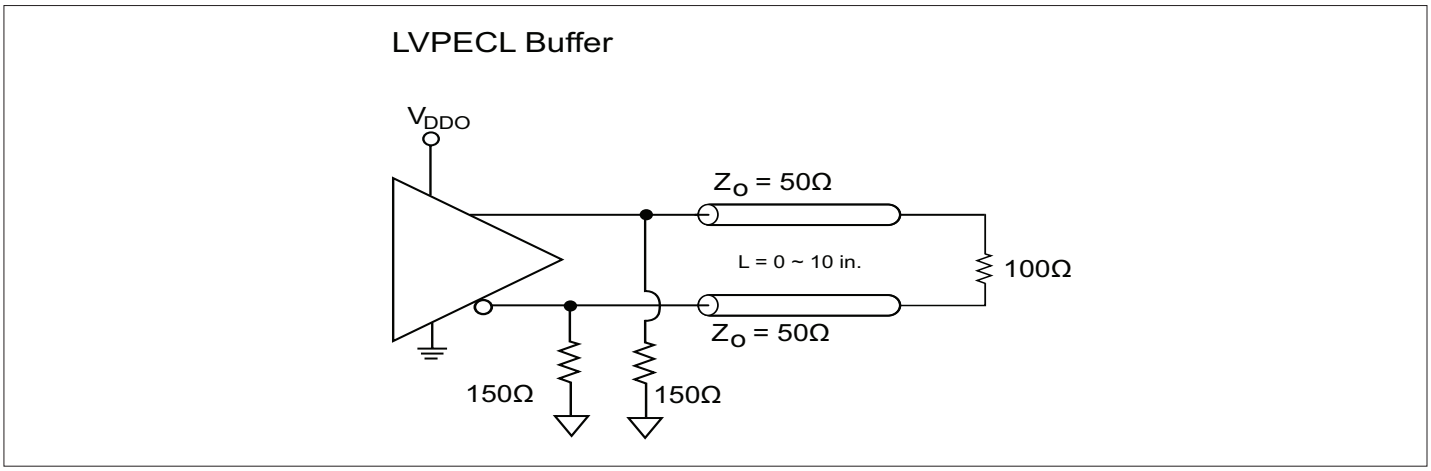
Phase Noise and Additive Jitter

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$

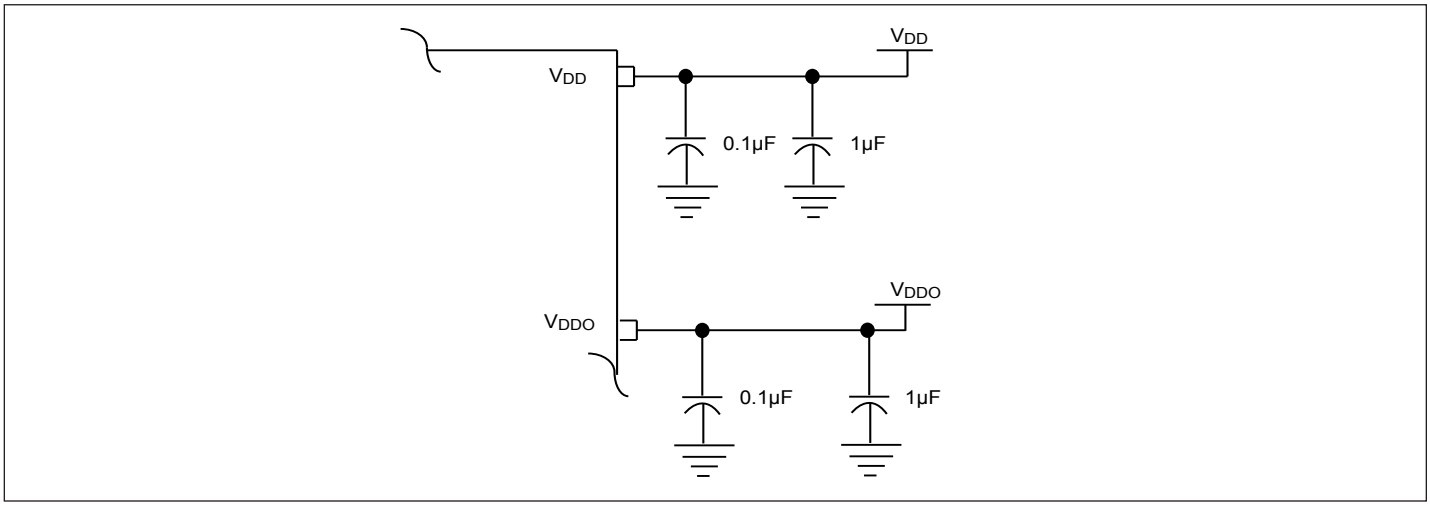


Configuration Test Load Board Termination for LVPECL Outputs

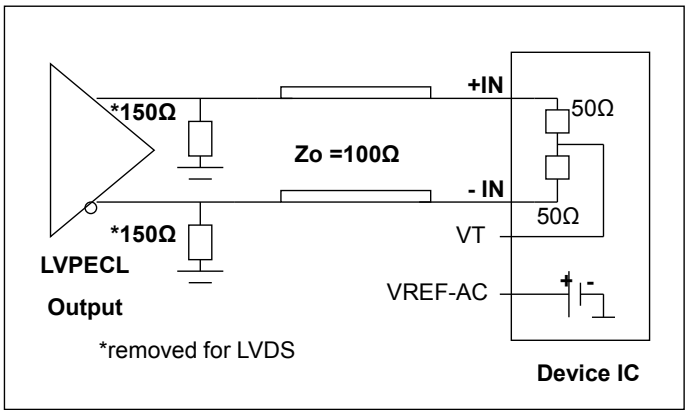


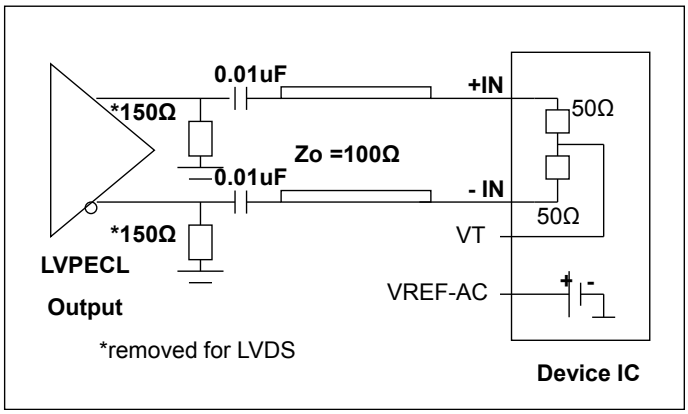
Power Supply Filtering Techniques

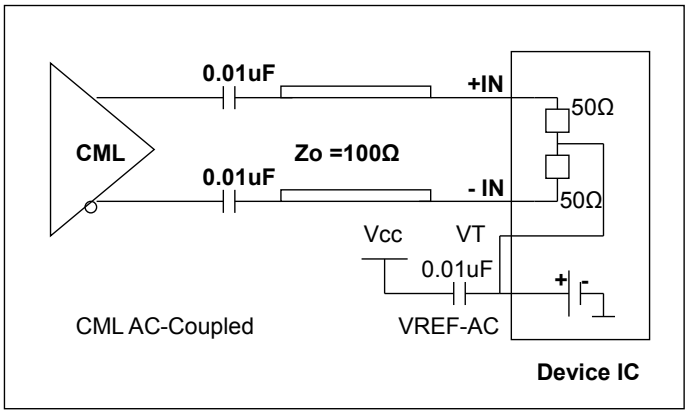
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF an 1µF bypass capacitors should be used for each pin.

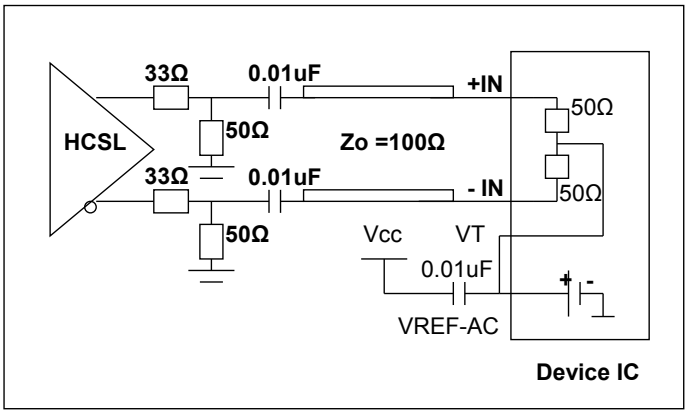


Using Differential Inputs to PI6C5912006







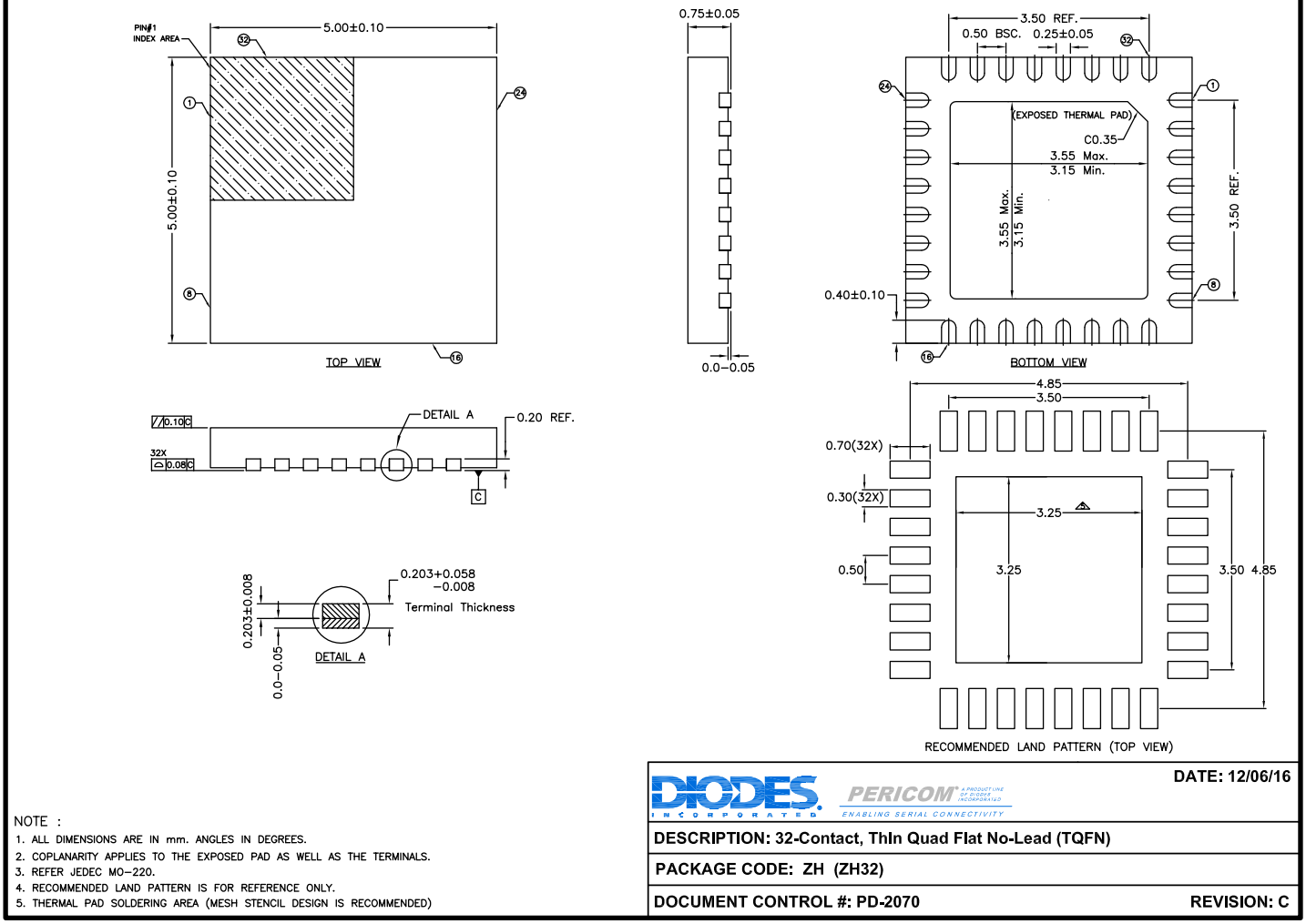


Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	44.7 °C/W
Θ_{JC}	Junction-to-case thermal resistance		21.7 °C/W

Part Marking

Packaging Mechanical: 32-TQFN (ZH)



17-0570

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C5912006ZHIEX	ZH	32-contact, Thin Quad Flat No-Lead (TQFN)	-40 °C to 85 °C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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