A product Line of
Diodes Incorporated

**PI6C5921516**

**16 Output LVDS Fanout Buffer**

## Features

- 16 Differential LVDS outputs
- 2 Selectable reference inputs support either single-ended or differential
- Up to 1.5GHz output frequency
- Ultra low additive phase jitter: < 0.01 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Low skew between outputs
- Low delay from input to output
- Separate input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TQFN-48 package

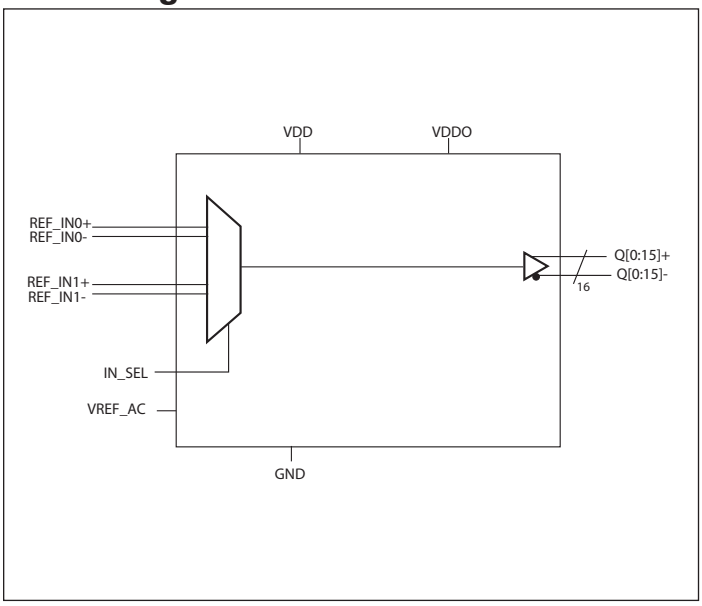
## Description

The PI6C5921516 is a high performance LVDS fanout buffer device which supports up to 1.5GHz frequency. This device is ideal for systems that need to distribute low jitter LVDS clock signals to multiple destinations.

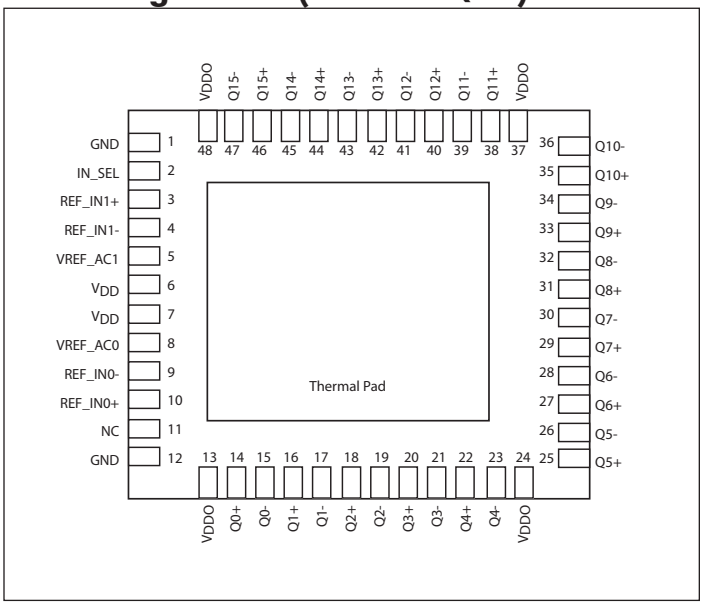
## Applications

- Networking systems including switches and routers
- High frequency backplane based computing and telecom platforms

## Block Diagram




## Pin Configuration (48-Pin TQFN)



## Pin Description

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1, 12 | GND | Power | Power supply ground |
| 2 | IN_SEL | Input | Input clock select. See Table 1 for function. LVCMOS/LVTTL interface levels. |
| 3, 4 | REF_IN1+ | Input | Reference input 1. Accepts Differential or Single Ended inputs |
| | REF_IN1- | | |
| 5 | VREF_AC1 | Output | Bias voltage output for REF_IN1 |
| 6, 7 | VDD | Power | Core power supply |
| 8 | VREF_AC0 | Output | Bias voltage output for REF_IN0 |
| 9, 10 | REF_IN0+ | Input | Reference input 0. Accepts Differential or Single Ended inputs |
| | REF_IN0- | | |
| 11 | NC | - | No Connect |
| 13, 24, 37, 48 | VDDO | Power | Output power supply |
| 14, 15 | Q0+ | Output | LVDS output pair 0. |
| | Q0- | | |
| 16, 17 | Q1+ | Output | LVDS output pair 1. |
| | Q1- | | |
| 18, 19 | Q2+ | Output | LVDS output pair 2. |
| | Q2- | | |
| 20, 21 | Q3+ | Output | LVDS output pair 3. |
| | Q3- | | |
| 22, 23 | Q4+ | Output | LVDS output pair 4. |
| | Q4- | | |
| 25, 26 | Q5+ | Output | LVDS output pair 5. |
| | Q5- | | |
| 27, 28 | Q6+ | Output | LVDS output pair 6. |
| | Q6- | | |
| 29, 30 | Q7+ | Output | LVDS output pair 7. |
| | Q7- | | |
| 31, 32 | Q8+ | Output | LVDS output pair 8. |
| | Q8- | | |
| 33, 34 | Q9+ | Output | LVDS output pair 9. |
| | Q9- | | |
| 35, 36 | Q10+ | Output | LVDS output pair 10. |
| | Q10- | | |

## Pin Description Cont.

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 38, 39 | Q11+ | Output | LVDS output pair 11. |
| | Q11- | | |
| 40, 41 | Q12+ | Output | LVDS output pair 12. |
| | Q12- | | |
| 42, 43 | Q13+ | Output | LVDS output pair 13. |
| | Q13- | | |
| 44, 45 | Q14+ | Output | LVDS output pair 14. |
| | Q14- | | |
| 46, 47 | Q15+ | Output | LVDS output pair 15. |
| | Q15- | | |
| Thermal pad | - | - | Thermal pad. Connect to ground. |

## Function Table

Table 1: Input select function

| IN_SEL | Function |
|---|---|
| 0 | REF_IN0 is the selected reference input |
| 1 | REF_IN1 is the selected reference input |
| Open | No inputs selected. Outputs Hi-Z |

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capcitance | | | 2 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 200 | | kΩ |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 200 | | kΩ |

## Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
Supply Voltage to Ground Potential ($V_{DD,}$ $V_{DDO}$)... -0.5 to +4.6V
Inputs (Referenced to GND) ..... -0.5 to $V_{DD}$+0.5V
Clock Output (Referenced to GND)..... -0.5 to $V_{DD}$+0.5V
Latch up.....200mA
ESD Protection (Input) .....2000 V min (HBM)
ESD Protection (Input) ..... 1000 V min (CDM)

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Power Supply Characteristics and Operating Conditions

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Core Power Supply Current | | | 190 | 235 | mA |
| $I_{DDO}$ | Output Power Supply Current | All LVDS outputs loaded | | | | |
| $T_A$ | Ambient Operating Temperature | | -40 | | 85 | °C |

## DC Electrical Specifications - Differential Inputs

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High current | Input = $V_{DD}$ | | | 20 | uA |
| $I_{IL}$ | Input Low current | Input = GND | -20 | | | uA |
| $V_{IH}$ | Input high voltage | | | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input low voltage | | -0.3 | | | V |
| $V_{ID}$ | Input Differential Amplitude PK-PK | | 0.1 | | | V |
| $V_{CM}$ | Common model input voltage | | GND + 0.5 | | $V_{DD}$-0.85 | V |
| $ISO_{MUX}$ | MUX isolation | | | -89 | | dBc |

## DC Electrical Specifications - LVCMOS Inputs

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High current | Input = $V_{DD}$ | | | 150 | uA |
| $I_{IL}$ | Input Low current | Input = GND | -150 | | | uA |
| $V_{IH}$ | Input high voltage | $V_{DD}$=3.3V | 2.0 | | $V_{DD}$+0.3 | V |
| | | $V_{DD}$=2.5V | 1.7 | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input low voltage | $V_{DD}$=3.3V | -0.3 | | 0.8 | V |
| | | $V_{DD}$=2.5V | -0.3 | | 0.7 | V |

## DC Electrical Specifications- LVDS Outputs

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High voltage | | | 1.4 | | V |
| $V_{OL}$ | Output Low voltage | | | 1.0 | | V |
| $V_{OD}$ | Differential output voltage | @800MHz to ≤1.5GHz | 100 | | 400 | mV |
| | | @ ≤800MHz | 250 | | 450 | mV |
| $DV_{OD}$ | Change in $V_{OD}$ between complete-ly output states | | -15 | | 15 | mV |
| Vocm | Output commode voltage | | | 1.25 | | V |
| DVocm | Change in Vocm between com-pletely output states | | | | 50 | mV |

## AC Electrical Specifications – Differential Inputs

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{IN}$ | Clock input frequency | | | | 1500 | MHz |
| $V_{INPP}$ | Differential Input peak to peak voltage | 1.5GHz ≤ $F_{IN}$ ≤ 2 GHz | 0.2 | | 1.5 | V |
| | | $F_{IN}$ ≤ 1.5 GHz | 0.1 | | 1.5 | V |
| ER | Input Edge Rate | | 1.5 | | | V/ns |

## AC Electrical Specifications – LVCMOS Inputs

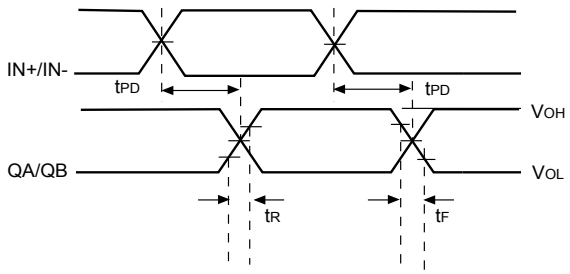
| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{IN}$ | Clock input frequency | | | | 200 | MHz |
| ER | Input Edge Rate | | 1.5 | | | V/ns |

## AC Electrical Specifications – LVDS Outputs

| Parameter | Description | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $F_{OUT}$ | Clock output frequency | LVDS | | | | 1500 | MHz |
| $T_r$ | Output rise time | From 20% to 80% | | | 150 | | ps |
| $T_f$ | Output fall time | From 80% to 20% | | | 150 | | ps |
| $T_{ODC}$ | Output duty cycle | <1.5GHz | | 48 | | 52 | % |
| $T_j$ | Buffer additive jitter RMS | 156.25MHz, 12kHz to 20MHz | | | 0.01 | | ps |
| | | 156.25MHz, 10kHz to 1MHz | | | 0.01 | | ps |
| $T_{SK}$ | Output Skew | | | | 40 | 50 | ps |
| $T_{PD}$ | Propagation Delay | | | | 620 | 700 | ps |
| $T_{OD}$ | Valid to HiZ | | | | | 100 | ns |
| $T_{OE}$ | HiZ to valid | | | | | 100 | ns |
| $T_{P2P\ Skew}$ | Part to Part Skew[1] | | | -50 | | 50 | ps |
| $V_{REF\_AC}$ | Input bias voltage | $I_{AC}$ = 2mA | | | 1.25 | | V |

## Propagation Delay

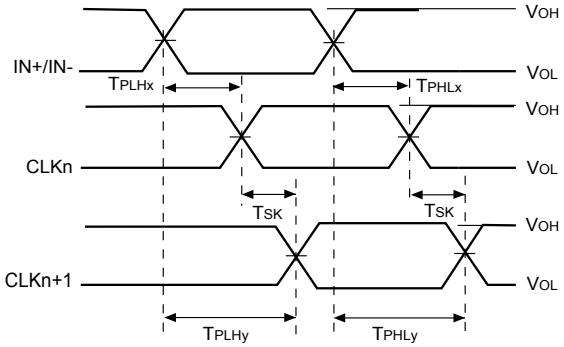
Propagation Delay $T_{PD}$




$T_{SK} = T_{PLH2} - T_{PLH1}$ or $T_{SK} = T_{PHL2} - T_{PHL1}$

## Output Skew

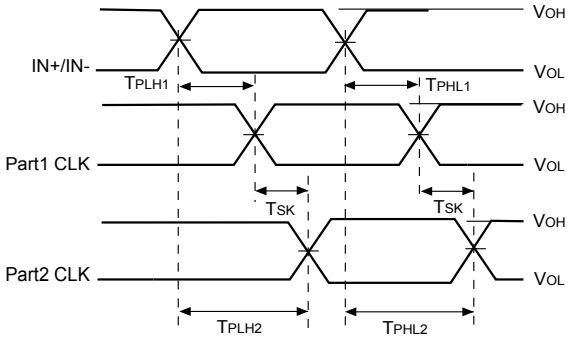
Output Skew $T_{SK}$




$T_{SK} = T_{PLHy} - T_{PLHx}$ or $T_{SK} = T_{PHLy} - T_{PHLx}$

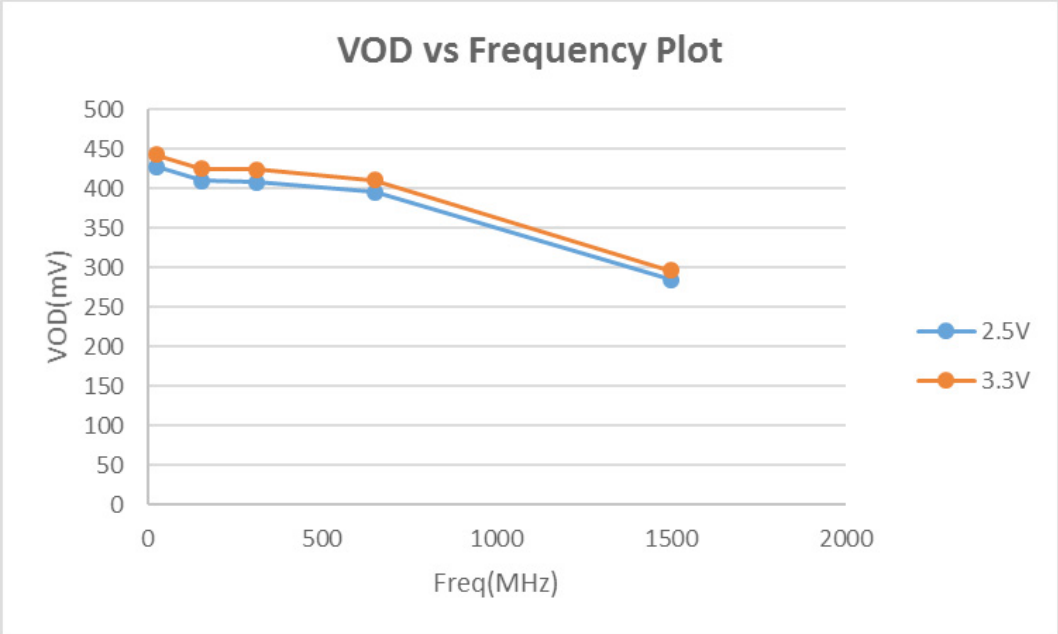
## Part to Part Skew

Part-to-Part Skew



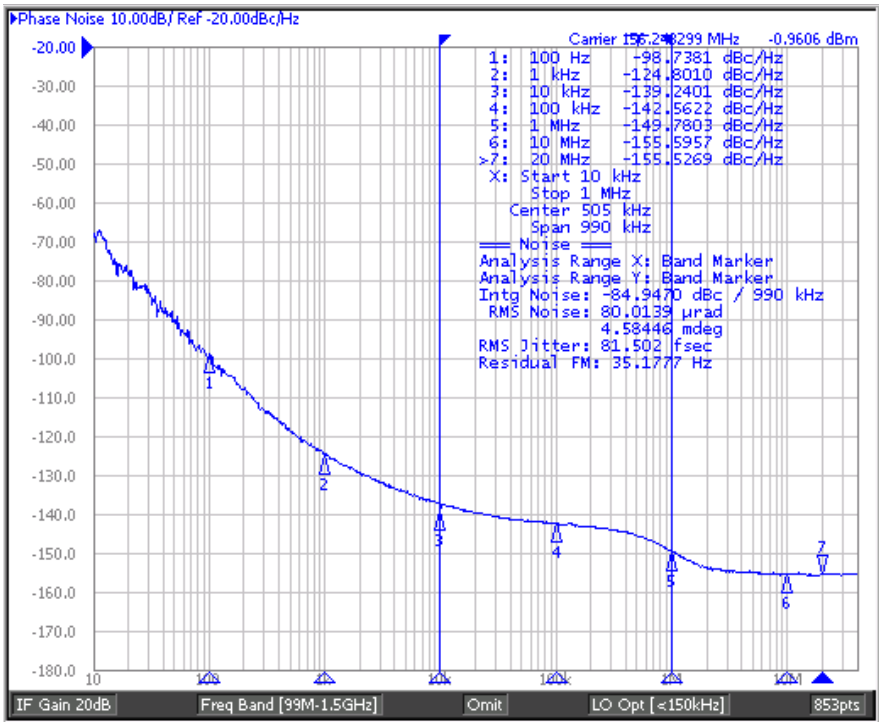

$T_{SK} = T_{PLH2} - T_{PLH1}$ or $T_{SK} = T_{PHL2} - T_{PHL1}$

## LVDS Output Swing vs. Frequency

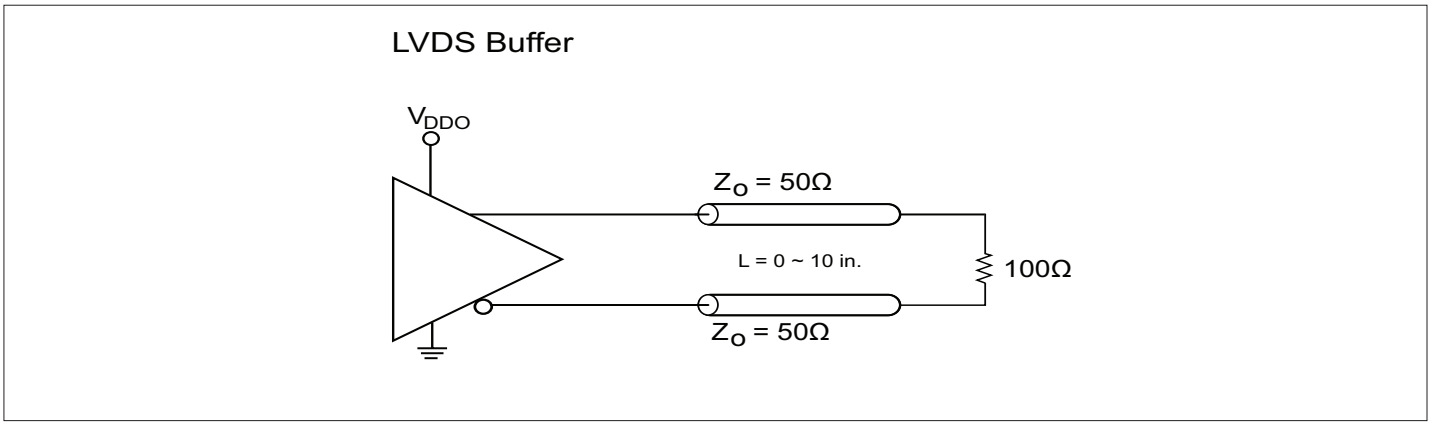


## Phase Noise and Additive Jitter

Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$




## Configuration Test Load Board Termination for LVDS/ LVDS Outputs



## Application Information

***Wiring the differential input to accept single ended levels***

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD}$ = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

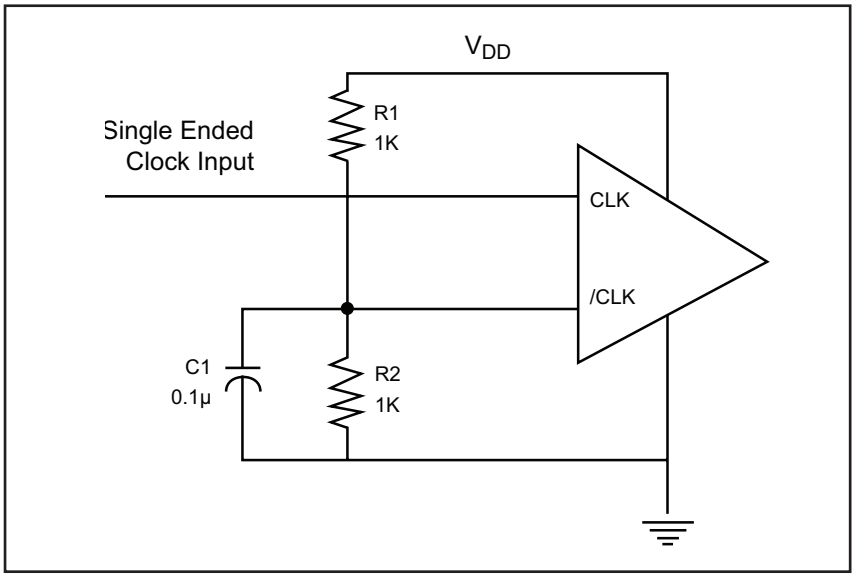
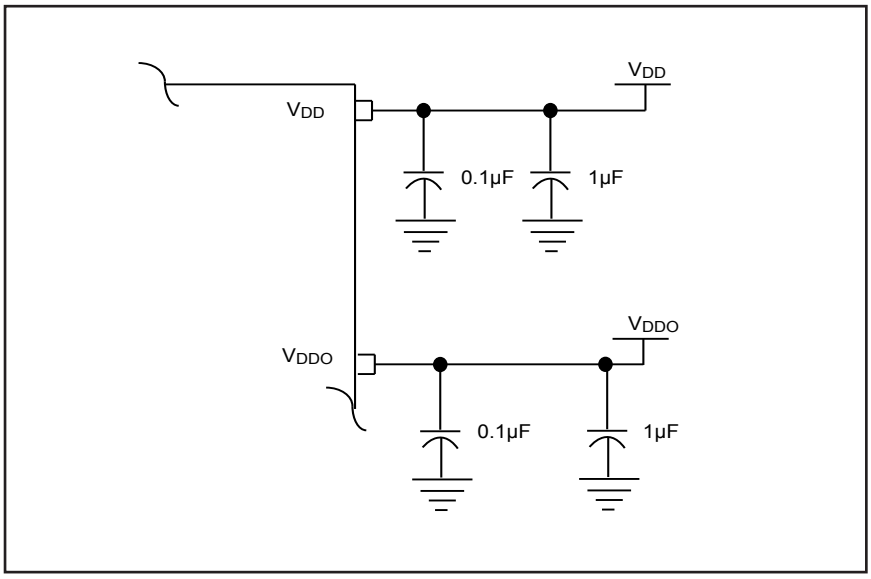


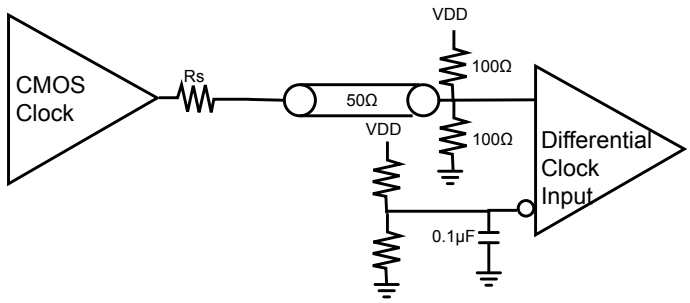

Figure 1. Single-ended input to Differential input device

## Power Supply Filtering Techniques

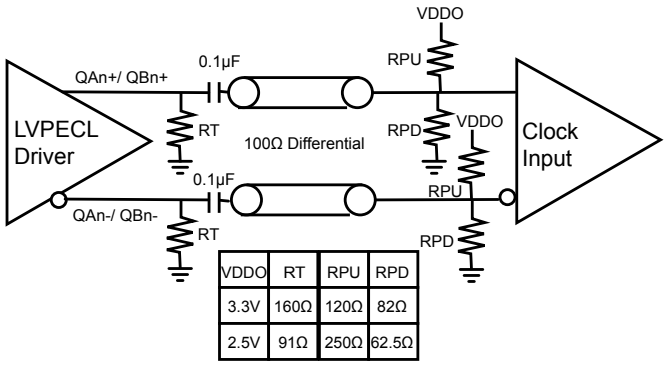
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF an 1µF bypass capacitors should be used for each pin.



## Single Ended Input, DC couple

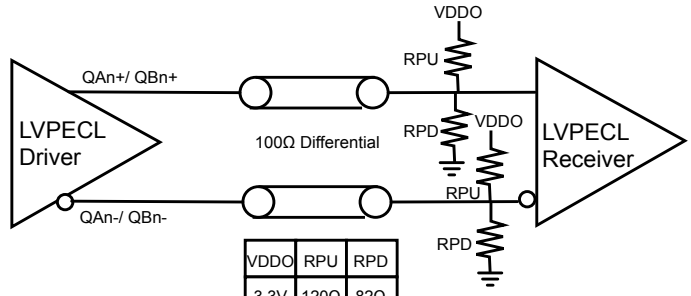



## LVDS, AC Couple, Thevenin Equivalent



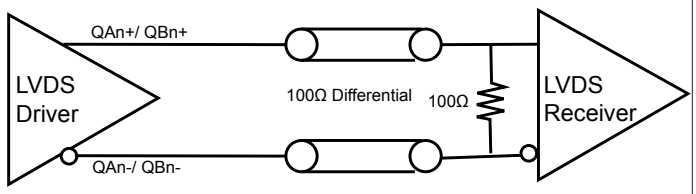

| VDDO | RT | RPU | RPD |
|---|---|---|---|
| 3.3V | 160Ω | 120Ω | 82Ω |
| 2.5V | 91Ω | 250Ω | 62.5Ω |

## LVDS, DC Couple, Thevenin Equivalent

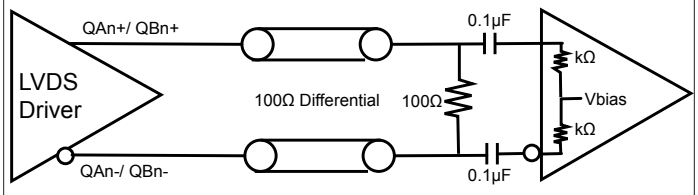



| VDDO | RPU | RPD |
|---|---|---|
| 3.3V | 120Ω | 82Ω |
| 2.5V | 250Ω | 62.5Ω |

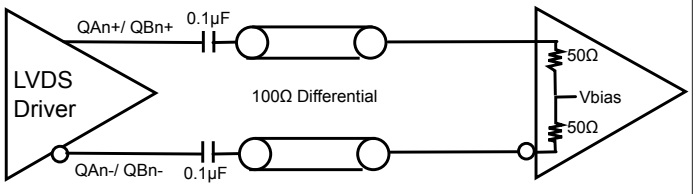
## LVDS DC Couple

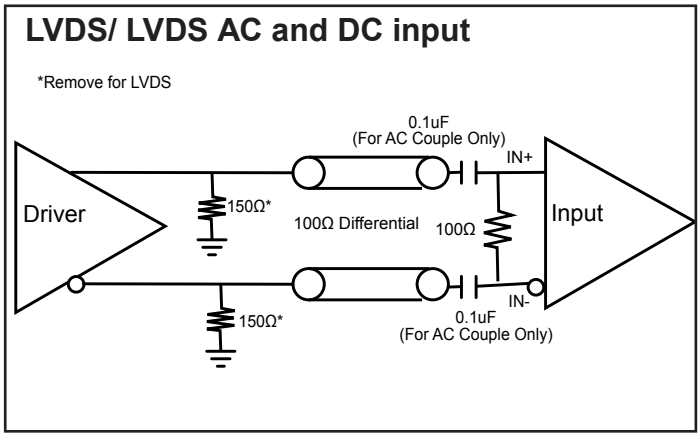



## LVDS AC Couple at Load




## LVDS AC Couple with Internal Termination





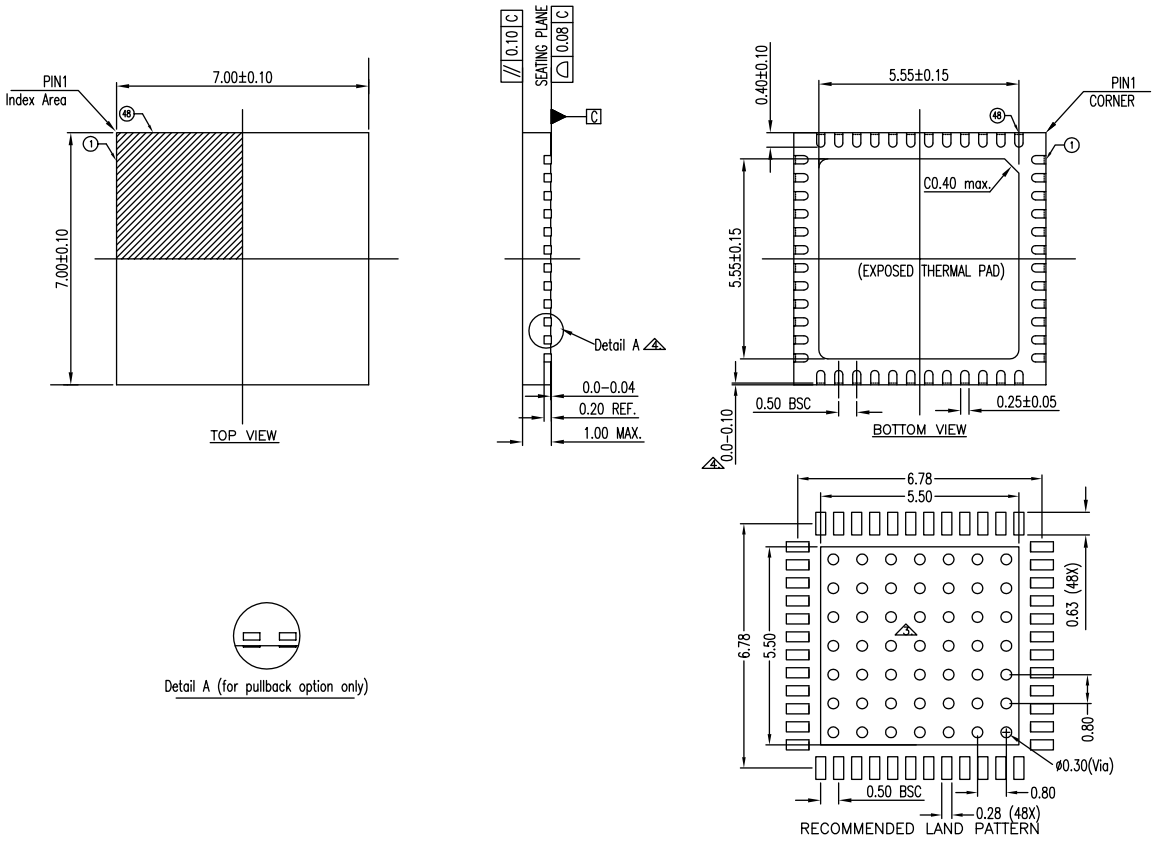

## Thermal Information

| Symbol | Description | Condition | |
|---|---|---|---|
| $\Theta_{JA}$ | Junction-to-ambient thermal resistance | Still air | 23.65 °C/W |
| $\Theta_{JC}$ | Junction-to-case thermal resistance | | 9.10 °C/W |

## Part Marking

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

## Packaging Mechanical: 48-TQFN (ZD)




NOTE :
1. All dimensions are in mm. Angles in degree.
2. Refer JEDEC MO–220
3. Thermal Pad Soldering Area
4. Depending on the method of lead termination at the edge of the package, pull back maybe present.
5. Recommended Land Pattern is for reference only.

DIODES INCORPORATED | PERICOM A PRODUCT LINE OF DIODES INCORPORATED — ENABLING SERIAL CONNECTIVITY

DATE: 07/26/16

DESCRIPTION: 48-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD48)

DOCUMENT CONTROL #: PD-2045 REVISION: F

16-0151

**For latest package info.**

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

## Ordering Information

| Ordering Code | Package Code | Package Description | Operating Temperature |
|---|---|---|---|
| PI6C5921516ZDIEX | ZD | 48-contact, Very Thin Quad Flat No-Lead (TQFN) | -40 °C to 85 °C |

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

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