

Clock Generator for Pentium Notebooks with I²C and SDRAM Support

Features

- Supports Pentium or Pentium II CPUs
- Spread spectrum capability reduces EMI
- Low power consumption
- Four CPU Clocks with Vddq2 of 3.3V or 2.5V
- Seven PCI synchronous clocks (3.3V)
- One IOAPIC Clock @14.31818 MHz with VDDQ1 of 3.3V or 2.5V (power from pin 46)
- Two 48/24 MHz clocks (3.3V)
- Six/eight SDRAM clocks (3.3V)
- Three Ref. Clocks @14.31818 MHz (3.3V)
- Ref. 14.31818 MHz crystal oscillator input
- Separate 66/60# MHz select pin
- Separate power management MODE control pin
- I²C 2-Wire Serial Interface
- 48-pin SSOP and TSSOP Packages

Description

The PI6C671E is a mixed-voltage clock generator designed to provide all timing signals for Intel Pentium/Pentium II based motherboards. It provides four CPU, seven PCI, and up to eight SDRAM clocks. Additionally, three reference clocks (same frequency as the crystal) and two selectable 24/48 MHz clocks are available.

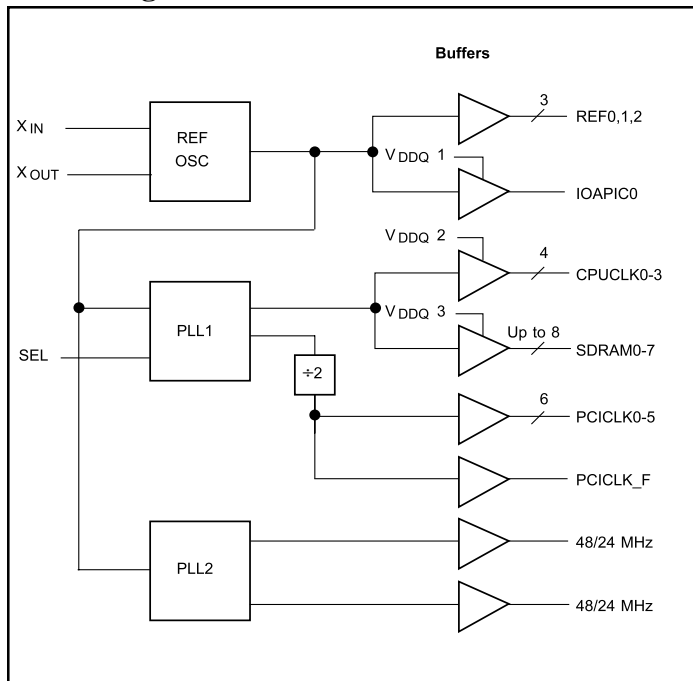
Pericom design improvements resulted in a low-power device. A special spread-spectrum feature may be enabled to minimize EMI.

The two-wire I²C serial interface can be used to reduce circuit noise and power consumption. I²C control lets you enable/disable each clock output driver, change CPU frequencies, and select 24 or 48 MHz outputs.

A power-down function (pin 44) puts the whole system in a low-power mode by stopping the crystal oscillator and both PLLs. CPU and PCI clocks may also be stopped by the "CPU_STOP#" (pin 27), and "PCI_STOP#" (pin 26) functions.

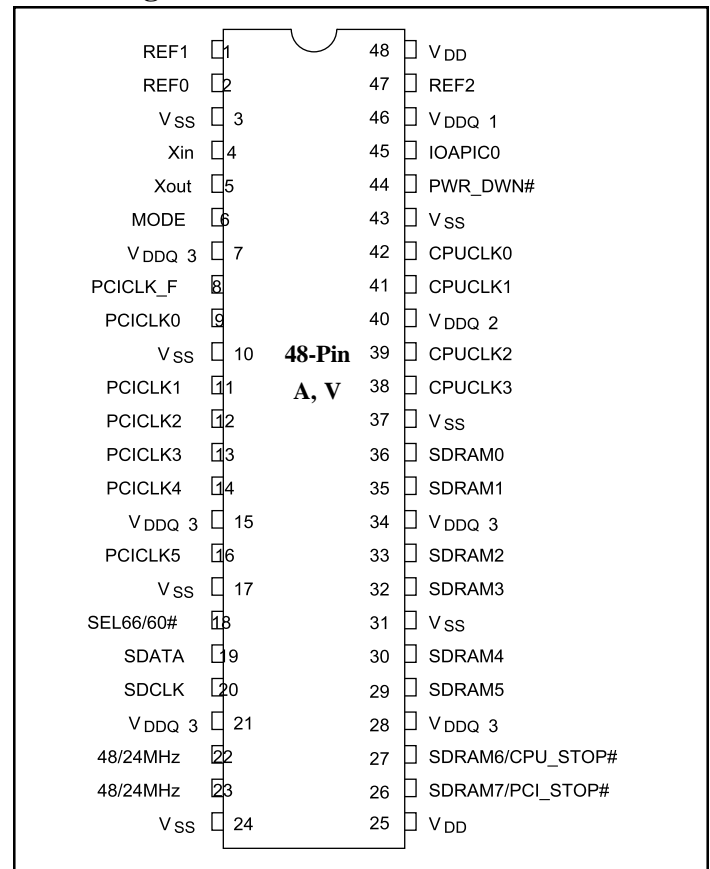
Note: Purchase of I²C components from Pericom conveys a license to use them in an I²C system as defined by Philips.

Block Diagram



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Pin Configuration



Pin Descriptions

| Signal Name | Type | Qty | Pin | Description |
|-------------------|--------|-----|---------------------|-----------------------------------------------------------------------------------------------------------|
| Xin | I | 1 | 4 | Crystal oscillator input or input for externally generated reference signal. |
| Xout | O | 1 | 5 | Crystal oscillator output. Connect to external parallel resonant crystal. |
| SEL66/60# | I | 1 | 18 | Select pin for enabling 66 MHz or 60 MHz. H=66 MHz, L=60 MHz. Has an internal pull-up resistor. |
| CPUCLK (0-3) | O | 4 | 42,41,39,38 | CPU & Host clock outputs. Powered by V _{DDQ2} , can be 2.5V or 3.3V. |
| SDRAM | O | 6 | 29,30,32,33,35,36 | SDRAM clocks 60/66 MHz. Powered by V _{DDQ3} (3.3V). |
| SDRAM6/CPU_STOP# | bi-dir | 1 | 27 | MODE=1: SDRAM6, MODE=0: CPU_STOP#. |
| SDRAM7/PCI_STOP# | bi-dir | 1 | 26 | MODE=1: SDRAM7, MODE=0: PCI_STOP#. |
| MODE | I | 1 | 6 | Mode Select pin for enabling power management features at pins 26 & 27. Has an internal pull-up resistor. |
| PCICLK(0-5) | O | 6 | 9,11,12,13,14,16 | Low skew PCI clock outputs. TTL compatible. Powered by V _{DDQ3} (3.3V). |
| PCICLK_F | O | 1 | 8 | Free running synchronous PCI clock. Stops when in shut down mode. |
| REF0,REF1,REF2 | O | 3 | 2,1,47 | 14.318 MHz buffered reference clock outputs. |
| IOAPIC0 | O | 1 | 45 | IOAPIC0 clock outputs. Powered by V _{DDQ1} , can be 2.5V or 3.3V |
| PWR_DWN# | I | 1 | 44 | PWR_DWN#, active LOW. |
| 48/24MHz | O | 2 | 22,23 | Selectable 48/24 MHz clock output. Powered by V _{DDQ3} (3.3V). |
| SDATA | I | 1 | 19 | Serial data input for I ² C control. |
| SDCLK | I | 1 | 20 | Clock input for I ² C control. |
| V _{SS} | Ground | 7 | 3,10,17,24,31,37,43 | Ground pins for the device. |
| V _{DD} | Power | 2 | 25,48 | Power supply for analog circuits and core logic. |
| V _{DDQ3} | Power | 5 | 7,15,21,28,34 | 3.3V I/O power supply. |
| V _{DDQ2} | Power | 1 | 40 | CPUCLK power supply. Can be either 2.5V or 3.3V. |
| V _{DDQ1} | Power | 1 | 46 | IOAPIC power supply. Can be either 2.5V or 3.3V. |

Driver Types

| Pin | Driver Type | Symbol | Description |
|-----------------------------|-------------|---------------------|-------------------------------------------|
| 2,47 | D | REF0 | 14.318 MHz clock output. |
| 1 | C | REF1, REF2 | 14.318 MHz clock output. |
| 8 | E | PCICLK_F | Free running clock during PCICLK stopped. |
| 9,11,12, 13,14,16 | E | PCICLK | PCI clock outputs TTL compatible 3.3V. |
| 22,23 | C | 48/24MHz | 48/24 MHz clock output 3.3V selectable. |
| 26,27,29,30, 32,33,35,36 | D | SDRAM | SDRAM clocks 60/66 MHz. |
| 38,39,41,42 | A | CPUCLK | CPU and host clock outputs: 2.5V or 3.3V |
| 45 | B | IOAPIC0, IOAPIC1 | IOAPIC clock output: 2.5V or 3.3V. |

Power Management Functions

Any or all clocks can be enabled or shut down via the I²C control interface. All clocks stop in the LOW state. CPU, SDRAM, and PCI clocks wait for one rising edge of PCICLK_F followed by a falling

edge of the clock of interest before settling in the LOW state. To reduce power consumption the PI6C671E clocks may be disabled in accordance with the following table.

| CPU_STOP# | PCI_STOP# | PWR_DWN# | CPUCLK, SDRAM | PCICLK | Other Clocks | Crystal & VCOs |
|-----------|-----------|----------|---------------|-----------|--------------|----------------|
| X | X | 0 | LOW | LOW | LOW | Off |
| 0 | 0 | 1 | LOW | LOW | Running | Running |
| 0 | 1 | 1 | LOW | 33/30 MHz | Running | Running |
| 1 | 0 | 1 | 66/60 MHz | LOW | Running | Running |
| 1 | 1 | 1 | 66/60 MHz | 33/30 MHz | Running | Running |

2-Wire I²C Control

The I²C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C671E is a slave receiver device. It can not be read back. Sub addressing is not supported. All preceding bytes must be sent in order to change one of the control bytes.

Every bite put on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiving device.

During normal data transfers SDATA changes only when SDCLK is LOW. Exceptions: A HIGH to LOW transition on SDATA while SDCLK is HIGH indicates a "start" condition. A LOW to HIGH transition on SDATA while SDCLK is HIGH is a "stop" condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ended with

a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW = write to addressed device). If the device's own address is detected, PI6C671E generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgement of the address byte (D2), two more bytes must be sent:

1. "Command Code" byte, and
2. "Byte Count" byte.

Although the data bits on these two bytes are "don't care," they must be sent and acknowledged.

The I²C interface is disabled when the PWR_DWN# pin is LOW. Preset control register contents are retained.

I²C Serial Configuration

Byte 0: Functional and Frequency Select

Clock Register (1 = enable, 0 = disable)

| Bit | Pin No. | @ Powerup | Description |
|-----|---------|-----------|-----------------------------------------------------------------------------------------------------------|
| 7 | | 0 | (Reserved) |
| 6 | | 0 | (Reserved, don't change) |
| 5 | | 0 | (Reserved, don't change) |
| 4 | | 0 | (Reserved, don't change) |
| 3 | 23 | 1 | 48/24 MHz (Freq Select) 1 = 48 MHz, 0 = 24 MHz |
| 2 | 22 | 1 | 48/24 MHz (Freq Select) 1 = 48 MHz, 0 = 24 MHz |
| 1 | | 0 | Bit1 Bit0 1 1 : Tri-State 1 0 : Spread Spectrum 0 1 : Test Mode 0 0 : Normal Operation |
| 0 | | 0 | |
| | | | |
| | | | |

Byte 1: CPU 24/48 MHz Active/Inactive Register
(1 = enable, 0 = disable)

| Bit | Pin No. | @Powerup | Description |
|-----|---------|----------|-----------------------------|
| 7 | 23 | 1 | 48/24 MHz (Active/Inactive) |
| 6 | 22 | 1 | 48/24 MHz (Active/Inactive) |
| 5 | | X | (Reserved) |
| 4 | N/A | X | CPUCLK4 (Active/Inactive) |
| 3 | 38 | 1 | CPUCLK3 (Active/Inactive) |
| 2 | 39 | 1 | CPUCLK2 (Active/Inactive) |
| 1 | 41 | 1 | CPUCLK1 (Active/Inactive) |
| 0 | 42 | 1 | CPUCLK0 (Active/Inactive) |

Byte 4: SDRAMActive/Inactive Register
(1 = enable, 0 = disable)

| Bit | Pin No. | Description |
|-----|---------|---------------------------|
| 7 | N/A | SDRAM15 (Active/Inactive) |
| 6 | N/A | SDRAM14 (Active/Inactive) |
| 5 | N/A | SDRAM13 (Active/Inactive) |
| 4 | N/A | SDRAM12 (Active/Inactive) |
| 3 | N/A | SDRAM11 (Active/Inactive) |
| 2 | N/A | SDRAM10 (Active/Inactive) |
| 1 | N/A | SDRAM9 (Active/Inactive) |
| 0 | N/A | SDRAM8 (Active/Inactive) |

Byte 2: PCI Active/Inactive Register
(1 = enable, 0 = disable)

| Bit | Pin No. | @Powerup | Description |
|-----|---------|----------|----------------------------|
| 7 | | X | (Reserved) |
| 6 | 8 | 1 | PCICLK_F (Active/Inactive) |
| 5 | 16 | 1 | PCICLK5 (Active/Inactive) |
| 4 | 14 | 1 | PCICLK4 (Active/Inactive) |
| 3 | 13 | 1 | PCICLK3 (Active/Inactive) |
| 2 | 12 | 1 | PCICLK2 (Active/Inactive) |
| 1 | 11 | 1 | PCICLK1 (Active/Inactive) |
| 0 | 9 | 1 | PCICLK0 (Active/Inactive) |

Byte 5: Peripheral Active/Inactive Register
(1 = enable, 0 = disable)

| Bit | Pin No. | @Powerup | Description |
|-----|---------|----------|--------------------------|
| 7 | | X | (Reserved) |
| 6 | | X | (Reserved) |
| 5 | | 1 | (Reserved) |
| 4 | 45 | 1 | IOAPIC (Active/Inactive) |
| 3 | | X | (Reserved) |
| 2 | 47 | 1 | REF2 (Active/Inactive) |
| 1 | 1 | 1 | REF1 (Active/Inactive) |
| 0 | 2 | 1 | REF0 (Active/Inactive) |

Byte3: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

| Bit | Pin No. | @Powerup | Description |
|-----|---------|----------|--------------------------|
| 7 | 26 | 1 | SDRAM7 (Active/Inactive) |
| 6 | 27 | 1 | SDRAM6 (Active/Inactive) |
| 5 | 29 | 1 | SDRAM5 (Active/Inactive) |
| 4 | 30 | 1 | SDRAM4 (Active/Inactive) |
| 3 | 32 | 1 | SDRAM3 (Active/Inactive) |
| 2 | 33 | 1 | SDRAM2 (Active/Inactive) |
| 1 | 35 | 1 | SDRAM1 (Active/Inactive) |
| 0 | 36 | 1 | SDRAM0 (Active/Inactive) |

Byte 6: Optional Register
for Possible Future Requirements

| Bit | Pin Number | Description |
|-----|------------|-------------|
| 7 | X | (Reserved) |
| 6 | X | (Reserved) |
| 5 | X | (Reserved) |
| 4 | X | (Reserved) |
| 3 | X | (Reserved) |
| 2 | X | (Reserved) |
| 1 | X | (Reserved) |
| 0 | X | (Reserved) |

Byte 7: Frequency Control

| Bit | @ Power up | Description |
|-----|------------|-------------|
| 7 | X | (Reserved) |
| 6 | X | (Reserved) |
| 5 | X | (Reserved) |
| 4 | X | (Reserved) |
| 3 | X | (Reserved) |
| 2 | 1 | FSEL2 |
| 1 | 1 | FSEL1 |
| 0 | 1 | FSEL0 |

| FSEL2 | FSEL1 | FSEL0 | Frequency |
|-------|-------|-------|--------------------|
| 0 | 0 | 0 | (Reserved) |
| 0 | 0 | 1 | (Reserved) |
| 0 | 1 | 0 | (Reserved) |
| 0 | 1 | 1 | 33 MHz |
| 1 | 0 | 0 | 50 MHz |
| 1 | 0 | 1 | 55 MHz |
| 1 | 1 | 0 | 60 MHz |
| 1 | 1 | 1 | From SEL66/60# pin |

DC Specifications

Absolute Maximum DC Power Supply

| Symbol | Supply Voltage | Min. | Max. | Units |
|-------------------|-----------------|------|------|-------|
| V _{DDQ3} | 3.3V Core & I/O | -0.5 | 4.6 | V |
| V _{DD} | 3.3V Core | -0.5 | 4.6 | |
| V _{DDQ2} | 2.5/3.3V I/O | -0.5 | 4.6 | |
| V _{DDQ1} | 2.5/3.3V I/O | -0.5 | 4.6 | |

DC Operating Requirements

(V_{DD}, V_{DDQ3} = 3.3V ±5%, V_{DDQ2} = 2.5V ±5%, T_A = 0 to 70°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|------------------|---------------------------|-------------------------------------|------|------|------|-------|
| V _{OH2} | 2.5V Output High Voltage | I _{OH} = -1mA | 2.1 | | | V |
| V _{OH3} | 3.3V Output High Voltage | I _{OH} = -1mA | 2.4 | | | |
| V _{OL2} | 2.5V Output Low Voltage | I _{OL} = 1mA | | | 0.4 | |
| V _{OL3} | 3.3V Output Low Voltage | I _{OL} = 1mA | | | 0.4 | |
| I _{DD} | Dynamic Supply Current | 66MHz Unloaded Outputs | | 55 | 70 | mA |
| I _{PD} | Power Down Supply Current | PWR_DWN# = 0 MODE = Float (High) | | 14 | 20 | μA |

Note: Typical values are at room temperature

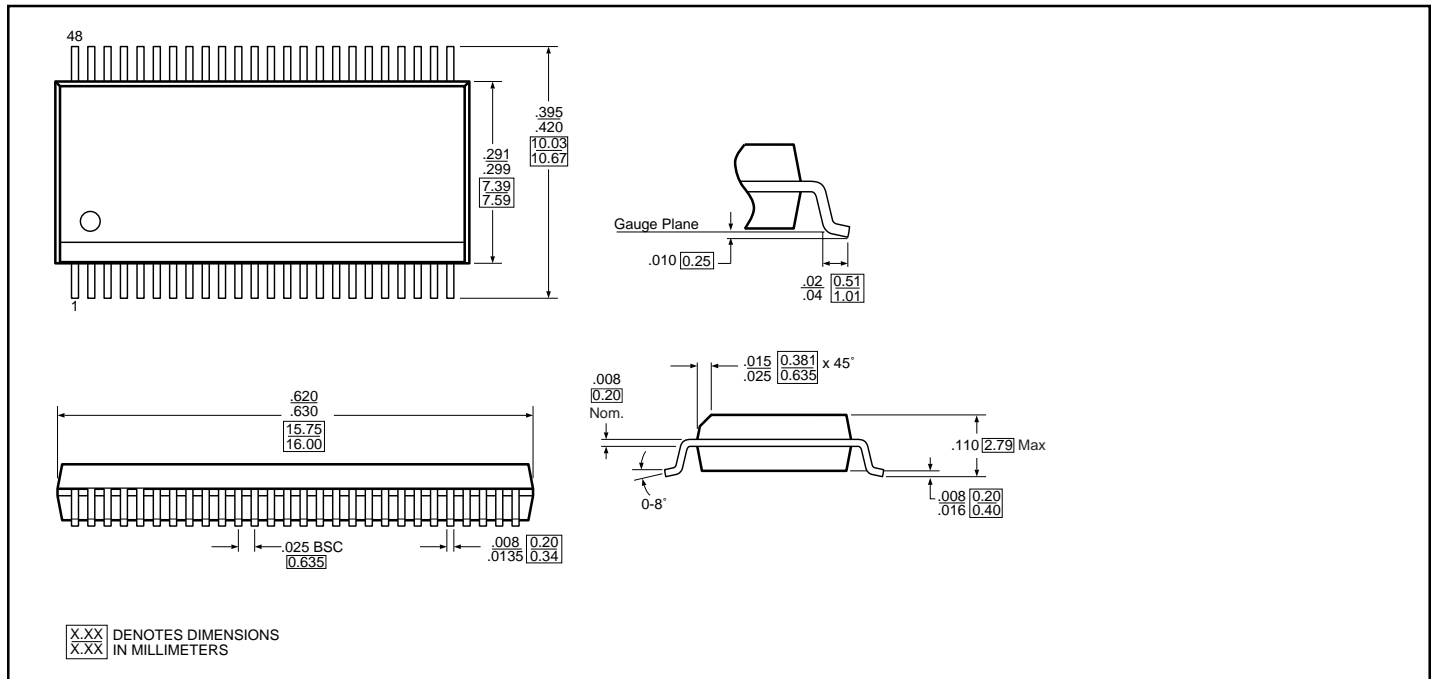
AC Timing

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------------|--------------------------------------------------------------------------------------------|------|------|------|
| t _{RF} | Host CLK rise/fall time, 0.4V - 2.0V | 0.4 | 1.6 | ns |
| t _{JITTER} | Host CLK Jitter | | 250 | ps |
| Duty Cycle | Measured the rising edge CLKs at 1.25V for the 2.5V clocks and at 1.5V for the 3.3V clocks | 45 | 55 | % |
| t _{HSKW} | Host Bus CLK skew | | 250 | ps |
| t _{HSKSD} | Host to SDRAM | | 500 | |
| t _{PKPS} | PCI CLK period stability | | 500 | |
| t _{PSKW} | PCI Bus CLK skew | | 500 | |
| t _{HPOFFSET} | Host to PCI Clock Offset | 1.0 | 4.0 | ns |
| t _{STB} | CLK Stabilization at power-up | | 3 | ms |

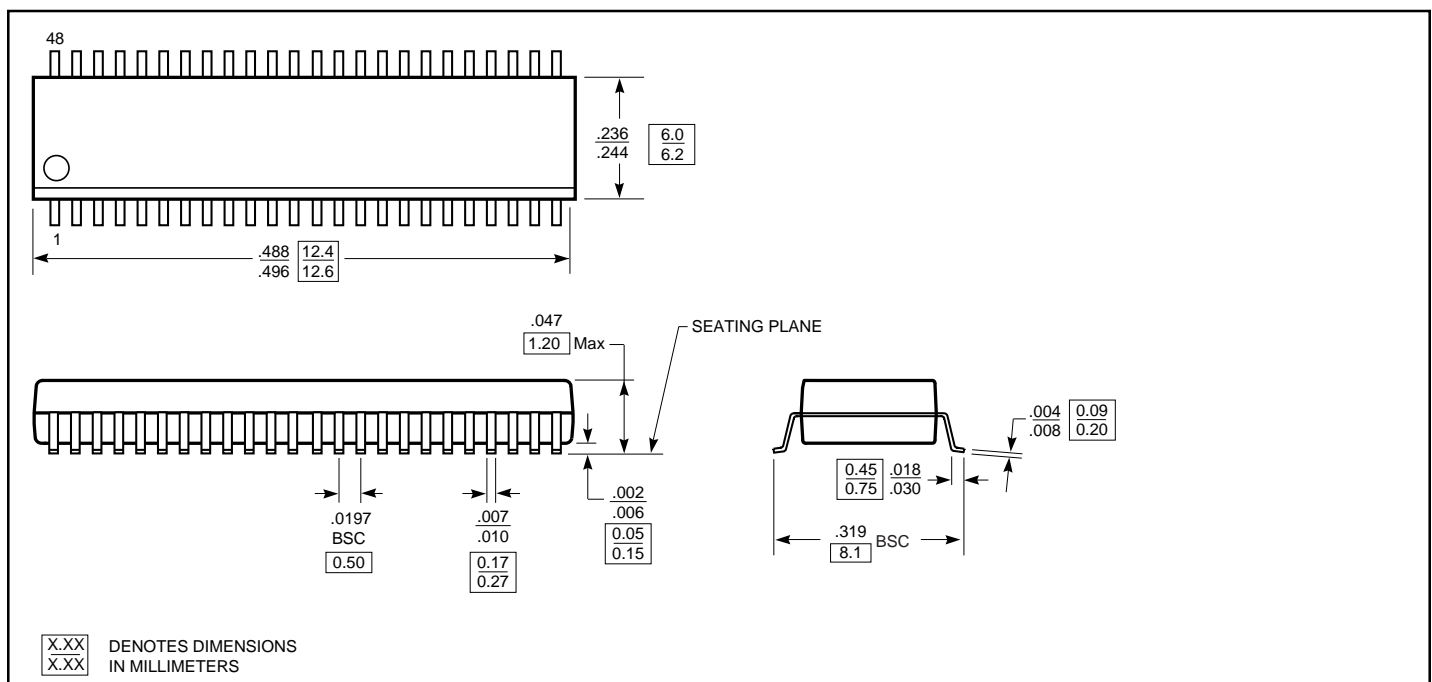
Driver Specifications

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Units |
|---------------------------------------------|-------------------|--------------|---------|---------|---------|-------|
| Type A: CPU 2.5V Buffer | | | | | | |
| Iohmin | Pull-up Current | Vout = 1.0V | -49 | | | mA |
| Iolmin | Pull-down Current | Vout = 1.2V | 48 | | | |
| Type A: CPU 3.3V Buffer | | | | | | |
| Iohmin | Pull-up Current | Vout = 1.0V | -69 | | | mA |
| Iolmin | Pull-down Current | Vout = 1.6V | 63 | | | |
| Type B: IOAPIC 2.5V Buffer | | | | | | |
| Iohmin | Pull-up Current | Vout = 1.4V | -36 | | | mA |
| Iolmin | Pull-down Current | Vout = 1.0V | 36 | | | |
| Type B: IOAPIC 3.3V Buffer | | | | | | |
| Iohmin | Pull-up Current | Vout = 1.0V | -58 | | | mA |
| Iolmin | Pull-down Current | Vout = 1.9V | 57 | | | |
| Type C: REF1, REF2, 48/24 MHz (3.3V) Buffer | | | | | | |
| Iohmin | Pull-up Current | Vout = 1.0V | -29 | | | mA |
| Iolmin | Pull-down Current | Vout = 1.95V | 29 | | | |
| Type D: REF0, SDRAM (3.3V) Buffer | | | | | | |
| Iohmin | Pull-up Current | Vout = 2.0V | -54 | | | mA |
| Iolmin | Pull-down Current | Vout = 1.0V | 54 | | | |
| Type E: PCI Clock Buffer | | | | | | |
| Iohmin | Pull-up Current | Vout = 1.0V | -33 | | | mA |
| Iolmin | Pull-down Current | Vout = 1.95V | 30 | | | |

48-Pin SSOP Package Data



48-Pin TSSOP Package Data



Ordering Information

| P/N | Description |
|-----------|----------------------|
| PI6C671EA | 48-pin TSSOP Package |
| PI6C671EV | 48-pin SSOP Package |

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