# PI6LC48S25A

## Next Generation HiFlex™ Ethernet Network Clock Generator

### Features

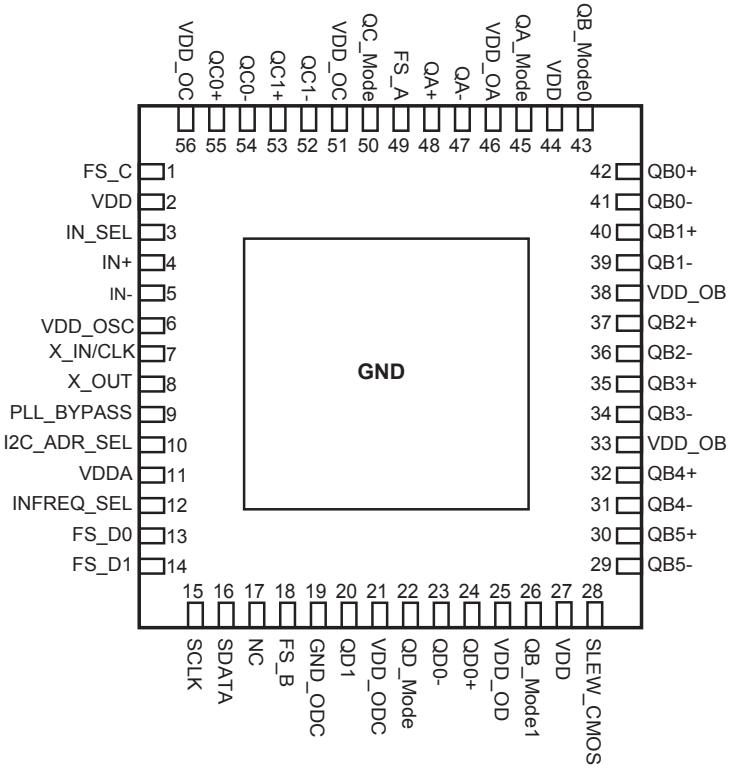
- 3.3V & 2.5V supply voltage
- Crystal/CMOS input: 25 MHz
- Differential input: 25MHz, 125MHz, and 156.25 MHz
- Output frequencies: 312.5, 156.25, 125, 100, 50, 25MHz
- 4 Output banks with selectable output signaling: LVPECL or LVDS
- Low 0.3ps typical integrated phase noise design: 156.25MHz (12kHz to 20MHz)
- PLL Bypass mode for test
- Power supply noise rejection: -52 dBc typical @ VDD
- Packaging (Pb-free & Green): 56-lead 8×8mm TQFN
- Industrial temperature support: -40C to 85C

### Description

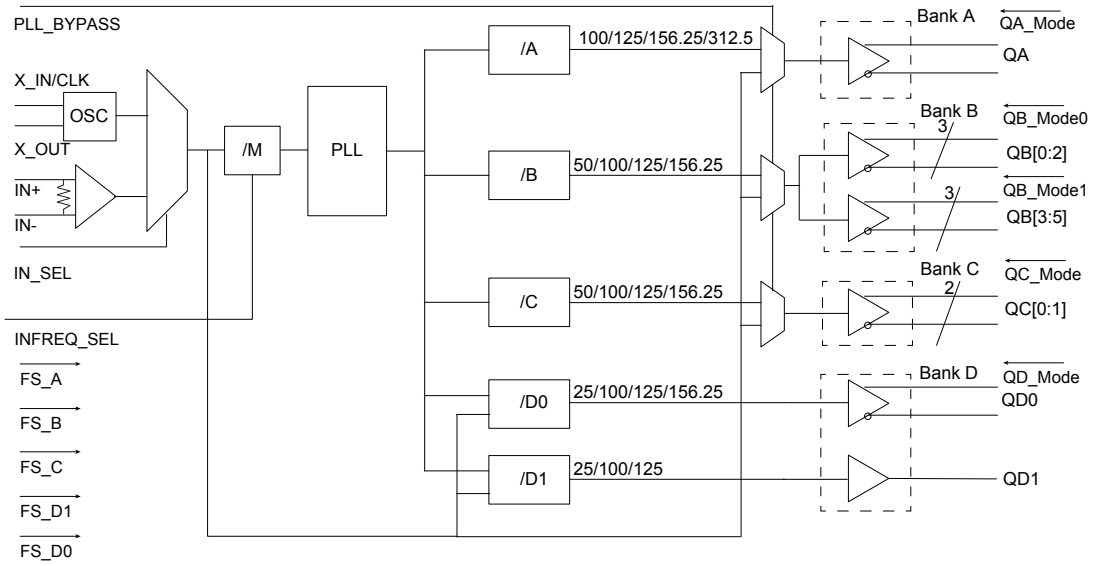
The PI6LC48S25A is an LC VCO based low phase noise design intended for 10GbE applications. Typical 10GbE usage assumes a 25MHz crystal input, while the PLL loop is used to generate the 156.25MHz and other Ethernet clock frequencies. An additional buffered crystal oscillator output is provided to serve as a low noise reference for other circuitry.

For Ethernet applications other than 10GbE, programmable dividers allow for simultaneous output of 312.5, 156.25, 125, 100, 50, and 25MHz. This device offers both pin selection and $I^2C$ interface to give more options to meet various system needs.

### Pin Configuration



## Block Diagram




Some output frequencies can be selected only in $I^2C$ mode

## Pin Description

| Pin Number | Pin Name | Type | | Description |
|---|---|---|---|---|
| 1 | FS_C | Input | Tri-level | Output frequency select for Bank C output |
| 2, 27, 44 | VDD | Power | – | Core supply |
| 3 | IN_SEL | Input | CMOS | Input select between Xtal and differential input |
| 4 | IN+ | Input | LVPECL | Differential reference input, also accepts AC-coupled LVDS, CML, HCSL or LVPECL. Differential inputs have an internal 100Ω cross resistor. |
| 5 | IN- | Input | | |
| 6 | VDD_OSC | Power | - | Power supply for Xtal Oscillator circuit |
| 7 | X_IN/CLK | Input | | Xtal or clock input, connect to a 25MHz Xtal or single-ended clock |
| 8 | X_OUT | Output | | Xtal output |
| 9 | PLL_BYPASS | Input | CMOS | PLL bypass, provide input frequency to Bank A, BankB, and Bank C |
| 10 | I2C_ADR_SEL | Input | CMOS | I2C address selection. |
| 11 | VDDA | Power | – | Analog supply |
| 12 | INFREQ_SEL | Input | Tri-level | Input frequency selection for reference input |
| 13 | FS_D0 | Input | Tri-level | Output frequency select for Bank D differential output |
| 14 | FS_D1 | Input | Tri-level | Output frequency select for Bank D CMOS output |
| 15 | SCLK | Input | | $I^2C$ clock input |
| 16 | SDATA | Input/ Output | | $I^2C$ Data line |

## Pin Description (cont.)

| Pin Number | Pin Name | Type | | Description |
|---|---|---|---|---|
| 17 | NC | | | Reserved pin. Do not connect this pin |
| 18 | FS_B | Input | Tri-level | Output frequency select for Bank B |
| 19 | GND_ODC | Power | | Ground for bank D CMOS output |
| 20 | QD1 | Output | CMOS | Bank D output 1 |
| 21 | VDD_ODC | Power | | Power supply for bank D CMOS output |
| 22 | QD_Mode | Input | Tri-level | Bank D differential output control |
| 23, 24 | QD0-, QD0+ | Output | LVPECL/ LVDS | Bank D differential output |
| 25 | VDD_OD | Power | | Power supply for bank D differential outputs |
| 26 | QB_Mode1 | Input | Tri-level | Bank B QB3 ~ QB5 differential output control |
| 28 | SLEW_CMOS | Input | CMOS | Output slew rate control for the CMOS output |
| 29, 30 | QB5-, QB5+ | Output | LVPECL/ LVDS | Bank B differential output |
| 31, 32 | QB4-, QB4+ | Output | LVPECL/ LVDS | Bank B differential output |
| 33, 38 | VDD_OB | Power | | Power supply for bank B differential outputs |
| 34, 35 | QB3-, QB3+ | Output | LVPECL/ LVDS | Bank B differential output |
| 36, 37 | QB2-, QB2+ | Output | LVPECL/ LVDS | Bank B differential output |
| 39, 40 | QB1-, QB1+ | Output | LVPECL/ LVDS | Bank B differential output |
| 41, 42 | QB0-, QB0+ | Output | LVPECL/ LVDS | Bank B differential output |
| 43 | QB_Mode0 | Input | Tri-level | Bank B QB0 ~ QB2 differential output control |
| 45 | QA_Mode | Input | Tri-level | Bank A differential output control |
| 46 | VDD_OA | Power | | Power supply for bank A differential outputs |
| 47, 48 | QA-, QA+ | Output | LVPECL/ LVDS | Bank A differential output |
| 49 | FS_A | Input | Tri-level | Output frequency select for Bank A |
| 50 | QC_Mode | Input | Tri-level | Bank C differential output control |
| 51, 56 | VDD_OC | Power | | Power supply for bank A differential outputs |
| 52, 53 | QC1-, QC1+ | Output | LVPECL/ LVDS | Bank C differential output |
| 54, 55 | QC0-, QC0+ | Output | LVPECL/ LVDS | Bank C differential output |
| E-pad | GND | Power | | Connect to ground, use thermal vias |

## Input MUX Selection

| IN_SEL | Input Source |
|---|---|
| 0 | Crystal Input (X_IN/CLK, X_OUT) |
| 1 | Differential Input (IN+, IN-) |
| NC | Crystal Input (X_IN/CLK, X_OUT) |

## Reference Input Frequency Select Table

| INFREQ_SEL | Reference Input |
|---|---|
| 0 | 25MHz |
| 1 | 125MHz |
| NC | 156.25MHz |

## PLL Bypass Control Function

| PLL_BYPASS | PLL operation |
|---|---|
| 0 | PLL enabled |
| 1 | PLL bypassed |

## Bank A/B/C/D Differential Output Control

| QA_ Mode | QA | QB_ Mode0 | QB[2:0] | QB_ Mode1 | QB[5:3] | QC_ Mode | QC[1:0] | QD_ Mode | QD0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | LVPECL | 0 | LVPECL | 0 | LVPECL | 0 | LVPECL | 0 | LVPECL |
| 1 | LVDS | 1 | LVDS | 1 | LVDS | 1 | LVDS | 1 | LVDS |
| NC | Hi-Z | NC | Hi-Z | NC | Hi-Z | NC | Hi-Z | NC | Hi-Z |

## Bank A/B/C Output Frequency Control Table

| FS_A | Bank A Output Freq. | FS_B | Bank B Output Freq. | FS_C | Bank C Output Freq. |
|---|---|---|---|---|---|
| 0 | 156.25MHz | 0 | 156.25MHz | 0 | 156.25MHz |
| 1 | 125MHz | 1 | 125MHz | 1 | 125MHz |
| NC | 312.5MHz | NC | 50MHz | NC | 100MHz |

## Bank D Output Frequency Control Table

| FS_D0 | Bank D Diff. Output Freq. | FS_D1 | Bank D CMOS Output Freq. |
|---|---|---|---|
| 0 | 156.25MHz | 0 | Hi-Z |
| 1 | 125MHz | 1 | 125MHz |
| NC | $f_{IN}$ | NC | $f_{IN}$ |

## Output Slew Rate Control Table

| SLEW_CMOS | Output Slew rate |
|---|---|
| 0 | Normal mode |
| 1 | Slow mode |

## I2C Address Selection Table

| $I^2C$_ADR_SEL | I2C Address |
|---|---|
| 0 | DC (h) |
| 1 | DE (h) |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, $V_{DD}$ .....–0.5V to +4.6V
ESD Protection (HBM) ..... 2000 V

**Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

## Operating Conditions

| Symbol | Parameters | Conditions | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Power Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| $V_{DD\_OX}$ | Output Power Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDA}$ | Analog Power Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | | | | 50 | mA |
| $I_{DD\_O}$ | Power Supply Current for Outputs | All outputs loaded, Diff. outputs are LVPECL | | | 525 | mA |
| | | All outputs loaded, Diff. outputs are LVDS | | | 242 | mA |
| $I_{DDA}$ | Analog Power Supply Current | | | | 45 | mA |
| $T_A$ | Ambient Temperature | | –40 | | 85 | °C |

## Input Electrical Characteristics

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $R_{pu}$ | Internal pull up resistance | | | 51 | | KΩ |
| $R_{dn}$ | Internal pull down resistance | | | 51 | | KΩ |
| $C_{XTAL}$ | Internal capacitance on X_IN and X_OUT pins | | | 12 | | pF |

## LVCMOS DC Electrical Characteristics

| Symbol | Parameters | Conditions | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | $V_{DD}$ = 3.3V ±10% | 2 | | $V_{DD}$ +0.3 | V |
| | | $V_{DD}$ = 2.5V ±5% | 1.7 | | $V_{DD}$ +0.3 | V |
| $V_{IL}$ | Input Low Voltage | $V_{DD}$ = 3.3V ±10% | -0.3 | | 0.8 | V |
| | | $V_{DD}$ = 2.5V ±5% | -0.3 | | 0.5 | V |
| $I_{IH}$ | Input High Current | $V_{IN}$ = $V_{DD\ max.}$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage | $V_{DD}$ = $V_{DD\_ODC}$ =3.3V ±10%; $I_{OH}$ = -12mA | 2.6 | | | V |
| | | $V_{DD}$ = $V_{DD\_ODC}$ =2.5V ±5%; $I_{OH}$ = -8mA | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$ = $V_{DD\_ODC}$ =3.3V ±10%; $I_{OH}$ = 12mA | | | 0.5 | V |
| | | $V_{DD}$ = $V_{DD\_ODC}$ =2.5V ±5%; $I_{OH}$ = 8mA | | | 0.5 | V |
| $T_{DC}$ | Input Duty Cycle | | 35 | | 65 | % |
| $R_{OUT}$ | CMOS Output impedance | $V_{DD\_ODC}$ =3.3V | | 24 | | Ω |
| | | $V_{DD\_ODC}$ =2.5V | | 30 | | |
| $C_{IN}$ | Input Capacitance | | | 3.5 | | pF |

## Differential Input DC Characteristics

| Symbol | Parameters | Conditions | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | | $V_{DD}$ - 0.7 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD}$ - 2.0 | | | V |
| $V_{CM}$ | Input Bias Voltage | | 0.5 | | $V_{DD}$ - 0.85 | V |
| $R_{IN}$ | Input Differential Impedance[1] | | 80 | 100 | 120 | Ω |
| $V_{IN-PP}$ | Input Differential Swing | Differential peak to peak | 0.3 | | 2.6 | V |

**Note: 1.** Differential input can be AC or DC coupled.

## Crystal Characteristic

| Parameters | Description | Min. | Typ | Max. | Units |
|---|---|---|---|---|---|
| OSCmode | Mode of Oscillation | Fundamental | | | |
| FREQ | Frequency | 10 | 25 | 40 | MHz |
| ESR[1] | Equivalent Series Resistance | | | 50 | Ω |
| Cload | Load Capacitance | | 18 | | pF |
| Cshunt | Shunt Capacitance | | | 7 | pF |
| | Drive Level | | | 250 | uW |

**Note: 1.** ESR value is dependent upon frequency of oscillation

## LVPECL Output DC Characteristics (1)

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OPP}$ | Output peak-peak Voltage | Single-ended | | 0.78 | | V |
| $V_{OH}$ | Output High Voltage | Outputs terminated with 50Ω to $V_{DD\_OX}$ - 2V | $V_{DD\_OX}$ - 1.4 | | $V_{DD\_OX}$ - 0.7 | V |
| $V_{OL}$ | Output Low Voltage | | $V_{DD\_OX}$ - 2.0 | | $V_{DD\_OX}$ - 1.3 | V |

## LVDS Output DC Characteristics (1)

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OPP}$ | Output Peak-peak Voltage | Single-ended | 0.247 | | 0.454 | V |
| $DV_{OPP}$ | $V_{OPP}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Output Offset Voltage | | 1.125 | | 1.375 | V |
| $DV_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

## AC Output Characteristics (see test configurations) (1)

$T_A$=-40C to 85C; $V_{DD}$=3.3V±10%, $V_{DD\_O}$=3.3V±10%

| Symbol | Parameters | Condition | | Min.. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | LVCMOS | | | | 125 | MHz |
| | | LVPECL | | | | 312.5 | MHz |
| | | LVDS | | | | 312.5 | MHz |
| $t_{R\ /\ tF}$ | Rise and Fall Time; 20% ~80% | LVCMOS | Normal Mode(2) | 150 | 400 | 850 | ps |
| | | | Slow Mode(3) | | | 2.0 | ns |
| | | LVPECL, LVDS | | | 250 | 400 | ps |
| $t_{DC}$ | Duty Cycle | LVCMOS | | 45 | | 55 | % |
| | | LVPECL, LVDS | | 48 | | 52 | % |
| | | Bank A at 312.5MHz only | | 47 | | 53 | % |
| $tj_{PHASE}$ | Integrated phase jitter (RMS) | 12kHz-20MHz @ 156.25MHz, 25MHz Xtal input | | | 0.3 | | ps |
| | | 10kHz-5MHz @ 25MHz, 25MHz Xtal input | | | 0.33 | | ps |
| $f_N$ | Single-Side Band Phase Noise | 156.25MHz, 25MHz Xtal input | Offset 1kHz | | -117 | | dBc/ Hz |
| | | | Offset 10kHz | | -130 | | |
| | | | Offset 100kHz | | -134 | | |
| | | | Offset 1MHz | | -139 | | |
| | | | Offset 10MHz | | -154 | | |
| PSNR | Power Supply Noise Rejection | $V_{DD}$, 50mVpp, 10k-1.5MHz | | | -52 | | dBc |
| | | $V_{DDA}$, 50mVpp, 10k-1.5MHz | | | -65 | | |
| | | $V_{DD\_Ox}$, 50mVpp, 10k-1.5MHz | | | -50 | | |
| $t_{STARTUP}$ | Start time | | | | | 10 | ms |
| $t_{LOCK}$ | PLL lock time | | | | | 20 | ms |

**Note:**

1. $V_{DD\_O}$= 3.3 is not valid with $V_{DD}$= 2.5V

2. Normal mode: All measurements are based on 20% to 80% of the single-ended waveform, Load is 4" trace and 4pF.

3. Slow mode: All measurements are based on 20% to 80% of the single-ended waveform, Load is 8" trace and 7pF.

## Serial Data Interface ($I^2C$ compatible)

PI6LC48S25A is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

For full electrical I2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

### Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 1 | $I^2C$_ADR_SEL | 1/0 |

### How to Write

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | | 8 bits | 1 bit | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Address | W(0) | Ack | Data Byte (D) | Ack | Data Byte (D+1) | Ack | ..... | Data Byte (D+N) | NAck | Stop bit |

### How to Read

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | | 8 bits | 1 bit | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Address | R(1) | Ack | Data Byte (D) | Ack | Data Byte (D+1) | Ack | ..... | Data Byte (D+N) | Ack | Stop bit |

## Output Frequency I2C bit Control Table

| FS_A (2-bit) | Bank A Freq. |
|---|---|
| 0 0 | 156.25MHz |
| 0 1 | 312.5MHz |
| 1 0 | 125MHz |
| 1 1 | 100MHz |

| FS_B (2-bit) | Bank B Freq. |
|---|---|
| 0 0 | 156.25MHz |
| 0 1 | 50MHz |
| 1 0 | 125MHz |
| 1 1 | 100MHz |

| FS_C (2-bit) | Bank C Freq. |
|---|---|
| 0 0 | 156.25MHz |
| 0 1 | 100MHz |
| 1 0 | 125MHz |
| 1 1 | 50MHz |

## Output Frequency I2C bit Control Table (cont.)

| FS_D0 (2-bit) | Diff Freq. |
|---|---|
| 0 0 | 156.25MHz |
| 0 1 | $f_{IN}$ |
| 1 0 | 125MHz |
| 1 1 | 100MHz |

| FS_D1 (2-bit) | CMOS Freq. |
|---|---|
| 0 0 | Output disabled |
| 0 1 | $f_{IN}$ |
| 1 0 | 125MHz |
| 1 1 | 100MHz |

## Input Freq. I2C bit Control Table

| INFREQ_SEL (2-bit) | Input Freq. |
|---|---|
| 0 0 | 25MHz |
| 0 1 | 156.25MHz |
| 1 0 | 125MHz |
| 1 1 | 100MHz |

## Byte 0: Output Frequency Selection Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | FS_C (1) | Bank C output divider | RW | 0 | See FS_C $I^2C$ control table | |
| 6 | FS_C (0) | | RW | 0 | | |
| 5 | FS_B (1) | Bank B output divider | RW | 0 | See FS_B $I^2C$ control table | |
| 4 | FS_B (0) | | RW | 0 | | |
| 3 | FS_A (1) | Bank A output divider | RW | 0 | See FS_A $I^2C$ control table | |
| 2 | FS_A (0) | | RW | 0 | | |
| 1 | Vendor ID | | RW | 0 | | |
| 0 | Vendor ID | | RW | 0 | | |

## Byte 1: Output Frequency Selection and Misc. Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | $I^2C$ pin control | Determine external pins or $I^2C$ control mode | RW | 0 | External pins | $I^2C$ |
| 6 | I2C_ADR_SEL | Select $I^2C$ write address | RW | 0 | DC(h) | DE(h) |
| 5 | INFREQ_SEL (1) | Input frequency selection | RW | 0 | See INFREQ_SEL $I^2C$ control table | |
| 4 | INFREQ_SEL (0) | | RW | 0 | | |
| 3 | FS_D1 (1) | Bank D CMOS output divider | RW | 1 | See FS_D1 $I^2C$ control table | |
| 2 | FS_D1 (0) | | RW | 1 | | |
| 1 | FS_D0 (1) | Bank D Diff. output divider | RW | 1 | See FS_D0 $I^2C$ control table | |
| 0 | FS_D0 (0) | | RW | 1 | | |

## Byte 2: Output Enable Selection for Bank A and Bank B Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | | |
| 6 | OE for QB5 | Output enable bit for QB5 | RW | 0 | Enable | Disable |
| 5 | OE for QB4 | Output enable bit for QB4 | RW | 0 | Enable | Disable |
| 4 | OE for QB3 | Output enable bit for QB3 | RW | 0 | Enable | Disable |
| 3 | OE for QB2 | Output enable bit for QB2 | RW | 0 | Enable | Disable |
| 2 | OE for QB1 | Output enable bit for QB1 | RW | 0 | Enable | Disable |
| 1 | OE for QB0 | Output enable bit for QB0 | RW | 0 | Enable | Disable |
| 0 | OE for QA | Output enable bit for QA | RW | 0 | Enable | Disable |

## Byte 3: Output Enable and Output Type Selection for Bank C and D Register

| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | | |
| 6 | QD0 | Output Type Select QD Diff. output | RW | 0 | LVPECL | LVDS |
| 5 | QC1 | Output Type Select QC1 | RW | 0 | LVPECL | LVDS |
| 4 | QC0 | Output Type Select QC0 | RW | 0 | LVPECL | LVDS |
| 3 | OE for QD1 | Output enable bit for QD1 | RW | 0 | Enable | Disable |
| 2 | OE for QD0 | Output enable bit for QD0 | RW | 0 | Enable | Disable |
| 1 | OE for QC1 | Output enable bit for QC1 | RW | 0 | Enable | Disable |
| 0 | OE for QC0 | Output enable bit for QC0 | RW | 0 | Enable | Disable |

## Byte 4: Output Type Selection for Bank A and Bank B Register

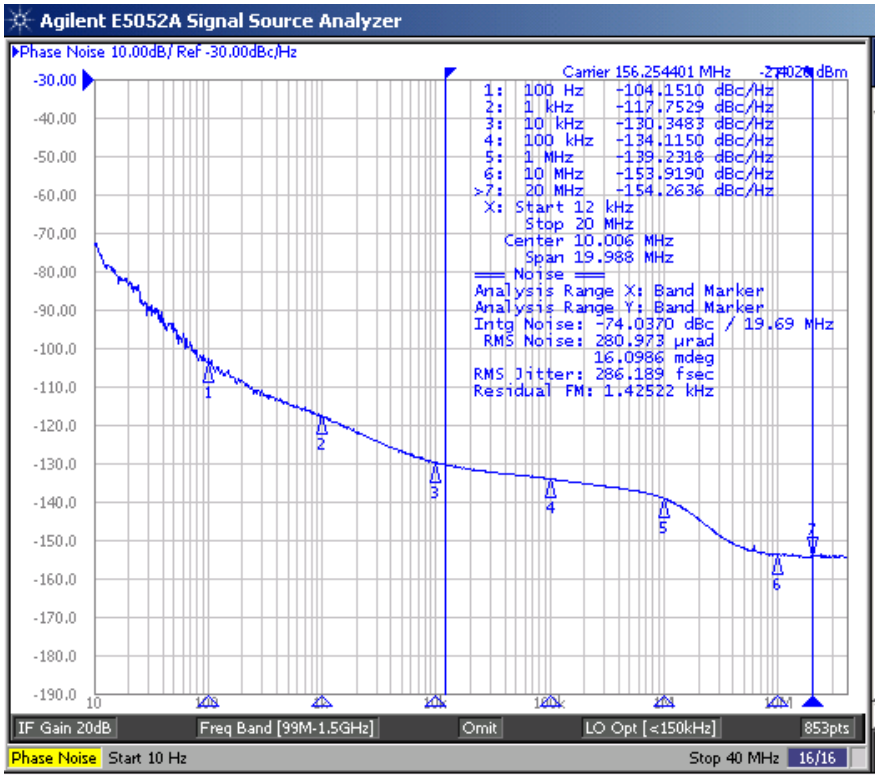
| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | | |
| 6 | QB5 | Output Type Select QB5 | RW | 0 | LVPECL | LVDS |
| 5 | QB4 | Output Type Select QB4 | RW | 0 | LVPECL | LVDS |
| 4 | QB3 | Output Type Select QB3 | RW | 0 | LVPECL | LVDS |
| 3 | QB2 | Output Type Select QB2 | RW | 0 | LVPECL | LVDS |
| 2 | QB1 | Output Type Select QB1 | RW | 0 | LVPECL | LVDS |
| 1 | QB0 | Output Type Select QB0 | RW | 0 | LVPECL | LVDS |
| 0 | QA | Output Type Select QA | RW | 0 | LVPECL | LVDS |

## Byte 5: Misc. Register

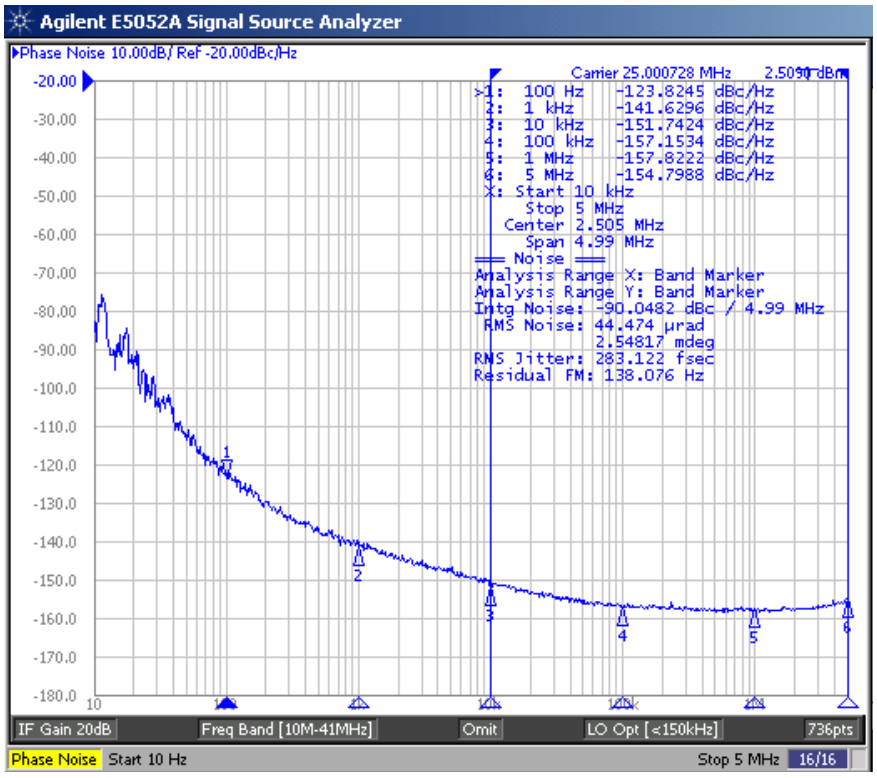
| Bit | Control Function | Description | Type | Power Up Condition | 0 | 1 |
|---|---|---|---|---|---|---|
| 7 | Reserved | | | | | |
| 6 | Reserved | | | 0 | | |
| 5 | Reserved | | | 0 | | |
| 4 | Reserved | | | 0 | | |
| 3 | PLL_BYPASS | PLL bypass function | RW | 0 | PLL is enabled | PLL is by-passed |
| 2 | SLEW_CMOS | Output slew rate control for the CMOS output | RW | 0 | Normal mode | Slow mode |
| 1 | Reserved | | | 0 | | |
| 0 | IN_SEL | Input selection | RW | 0 | Crystal | Reference |

## Phase Noise Plots

### 156.25MHz LVDS Clock




### 25MHz LVPECL Clock



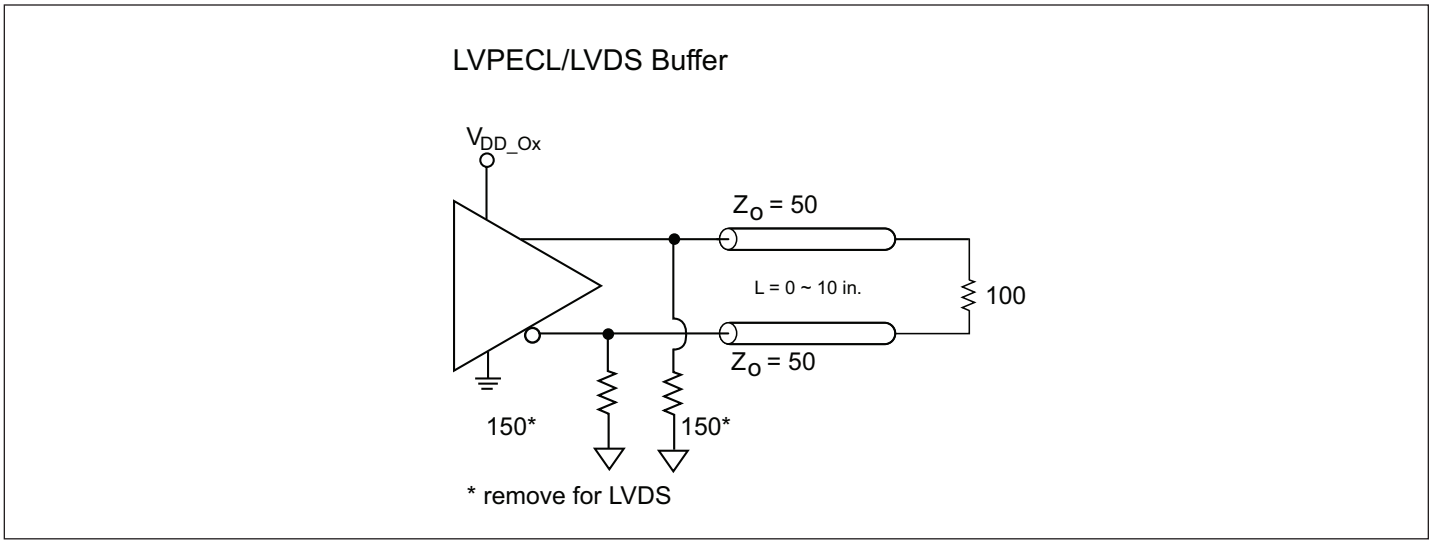



**Figure 1. LVPECL and LVDS Test Circuit**

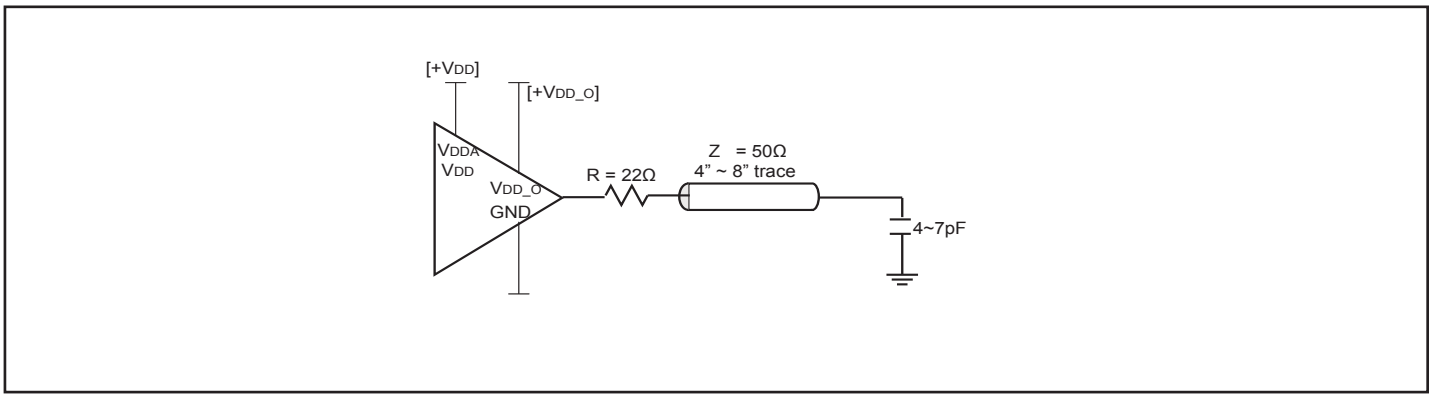



**Figure 2. CMOS Test Circuit**

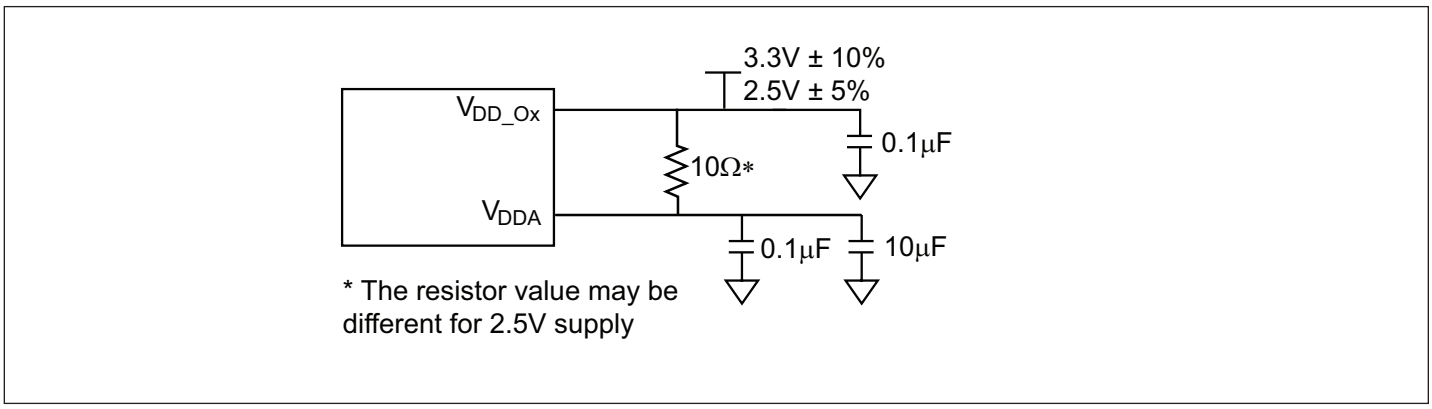
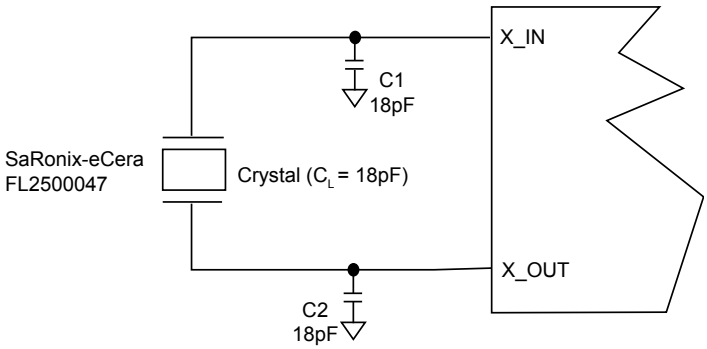



**Figure 3. Power Supply Filter**

## Crystal circuit connection

The following diagram shows PI6LC48S25A crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1=18pF, C2=18pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

## Crystal Oscillator Circuit




## Crystal Circuit Oscillator

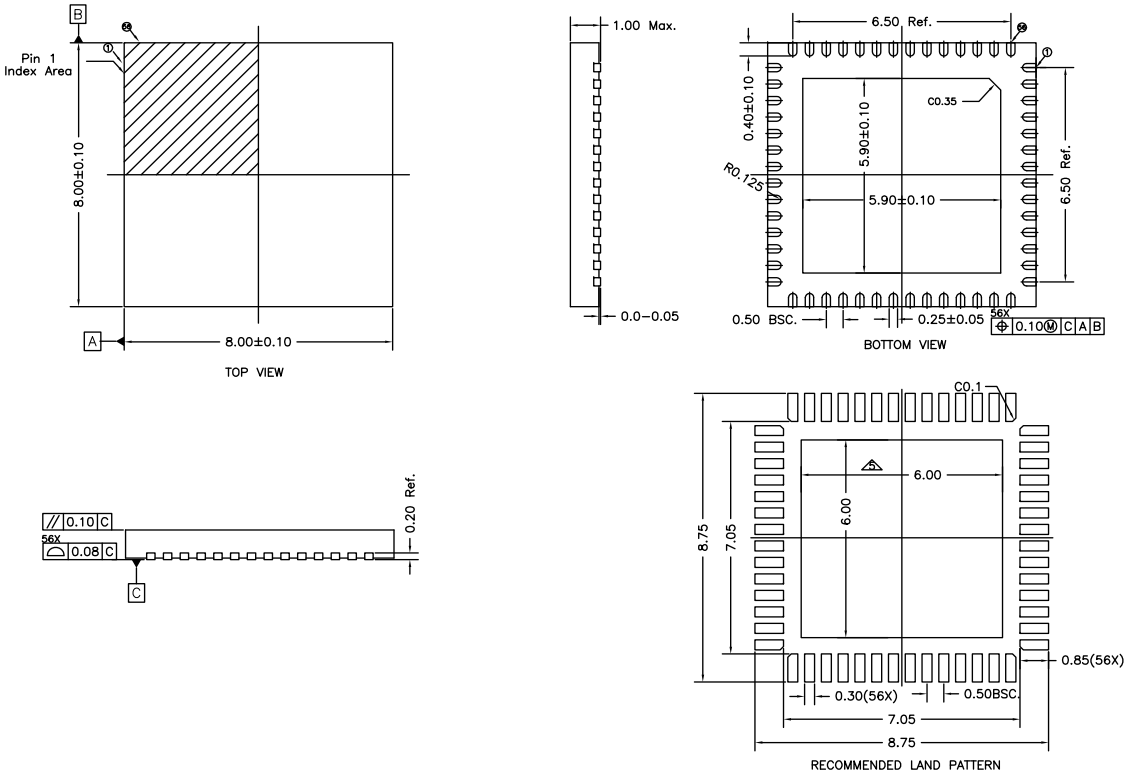
## Recommended Crystal Specification

**Pericom recommends:**

a) FY2500081, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

b) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

## Packaging Mechanical: 56-Pin TQFN (ZBB)




NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

PERICOM Enabling Serial Connectivity — DATE: 02/21/14

DESCRIPTION: 56-PIn, TQFN 8X8mm (1.0mm max)

PACKAGE CODE: ZBB (ZBB56)

DOCUMENT CONTROL #: PD-2180 REVISION: --

**Note:**

1. For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

## Ordering Information(1-3)

| Ordering Code | Package Code | Package Description | Operating Temperature |
|---|---|---|---|
| PI6LC48S25AZBBIE | ZBB | 56-Pin, Pb-free & Green (TQFN) | Industrial |

**Notes:**

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel