# 12-Bit To 24-Bit Multiplexed D-Type Latch with 3-State Outputs

## Product Features

- PI74ALVCH16260 is designed for low voltage operation
- $V_{CC}$ = 2.3V to 3.6V
- Hysteresis on all inputs
- Typical $V_{OLP}$ (Output Ground Bounce)
  < 0.8V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot)
  < 2.0V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Bus Hold retains last active bus state during 3-State, eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 300 mil wide plastic SSOP (V)



## Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The PI74ALVCH16260 is a 12-bit to 24-bit multiplexed D-type latch designed for 2.3V to 3.6 $V_{CC}$ operation. It is used in applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single data path.

Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface and in memory-interleaving.

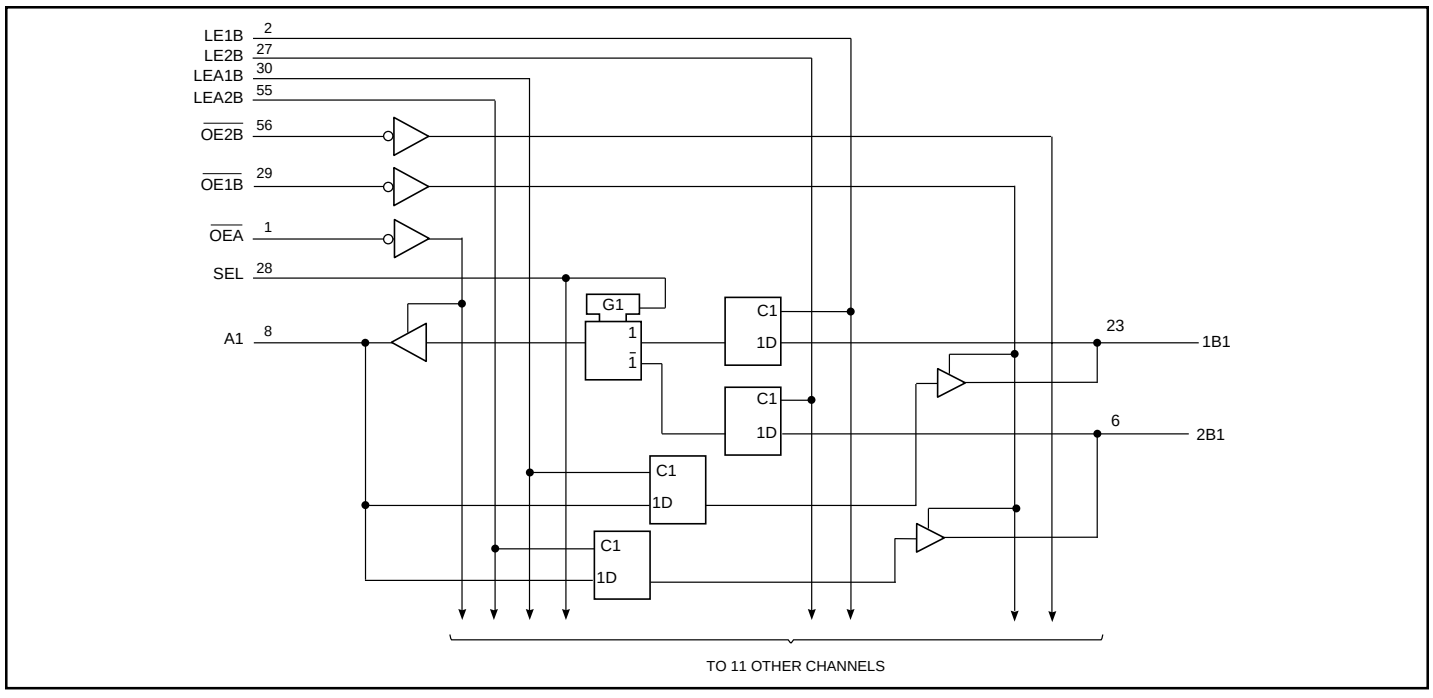
Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is HIGH, the latch is transparent. When the latch-enable input goes LOW, the data present at the inputs is latched and remains latched until the latch-enable input is returned HIGH.

To ensure high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor whose minimum value is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## Logic Block Diagram





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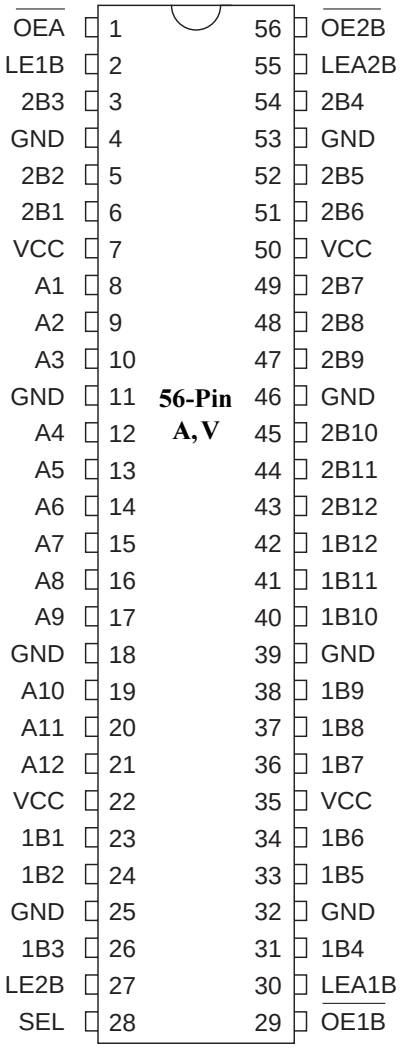
## Product Pin Description

| Pin Name | Description |
|---|---|
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| SEL | Select |
| LE | Latch Enable |
| A,1B,2B | Data Inputs |
| A,1B,2B | 3-State Outputs |
| GND | Ground |
| $V_{CC}$ | Power |



## Product Pin Configuration




## Truth Tables[1]

**B to A ($\overline{OEB}$ = H)**

| Inputs | | | | | | Output |
|---|---|---|---|---|---|---|
| 1B | 2B | SEL | LE1B | LE2B | $\overline{OEA}$ | A |
| H | X | H | H | X | L | H |
| L | X | H | H | X | L | L |
| X | X | H | L | X | L | A0 |
| X | H | L | X | H | L | H |
| X | L | L | X | H | L | L |
| X | X | L | X | L | L | A0 |
| X | X | X | X | X | H | Z |

**A to B ($\overline{OEA}$ = H)**

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| A | LEA1B | LEA2B | $\overline{OE1B}$ | $\overline{OE2B}$ | 1B | 2B |
| H | H | H | L | L | H | H |
| L | H | H | L | L | L | L |
| H | H | L | L | L | H | 2B0 |
| L | H | L | L | L | L | 2B0 |
| H | L | H | L | L | 1B0 | H |
| L | L | H | L | L | 1B0 | L |
| X | L | L | L | L | 1B0 | 2B0 |
| X | X | X | H | H | Z | Z |
| X | X | X | L | H | Active | Z |
| X | X | X | H | L | Z | Active |
| X | X | X | L | L | Active | Active |

**Note:**

1. H = High Signal Level
   L = Low Signal Level
   X = Irrelevant
   Z = High Impedance

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied ..... –40°C to +85°C
Input Voltage Range, $V_{IN}$ ..... –0.5V to $V_{CC}$ +0.5V
Output Voltage Range, $V_{OUT}$ ..... –0.5V to $V_{CC}$ +0.5V
DC Input Voltage ..... –0.5V to +5.0V
DC Output Current ..... 100mA
Power Dissipation ..... 1.0W

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



## DC Electrical Characteristics (Over the Operating Range, $T_A$ = –40°C to +85°C, $V_{CC}$ = 3.3V ± 10%)

| Parameters | Description | Test Conditions[1] | Min. | Typ.[2] | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 2.3 | | 3.6 | V |
| $V_{IH}$[3] | Input HIGH Voltage | $V_{CC}$ = 2.3V to 2.7V | 1.7 | | | |
| | | $V_{CC}$ = 2.7V to 3.6V | 2.0 | | | |
| $V_{IL}$[3] | Input LOW Voltage | $V_{CC}$ = 2.3V to 2.7V | | | 0.7 | |
| | | $V_{CC}$ = 2.7V to 3.6V | | | 0.8 | |
| $V_{IN}$[3] | Input Voltage | | 0 | | $V_{CC}$ | |
| $V_{OUT}$[3] | Output Voltage | | 0 | | $V_{CC}$ | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = -100µA, $V_{CC}$ = Min. to Max. | $V_{CC}$ -0.2 | | | |
| | | $V_{IH}$ = 1.7V, $I_{OH}$ = –6mA, $V_{CC}$ = 2.3V | 2.0 | | | |
| | | $V_{IH}$ = 1.7V, $I_{OH}$ = –12mA, $V_{CC}$ = 2.3V | 1.7 | | | |
| | | $V_{IH}$ = 2.0V, $I_{OH}$ = –12mA, $V_{CC}$ = 2.7V | 2.2 | | | |
| | | $V_{IH}$ = 2.0V, $I_{OH}$ = –12mA, $V_{CC}$ = 3.0V | 2.4 | | | |
| | | $V_{IH}$ = 2.0V, $I_{OH}$ = –24mA, $V_{CC}$ = 3.0V | 2.0 | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 100µA, $V_{IL}$ = Min. to Max. | | | 0.2 | |
| | | $V_{IL}$ = 0.7V, $I_{OL}$ = 6mA, $V_{CC}$ = 2.3V | | | 0.4 | |
| | | $V_{IL}$ = 0.7V, $I_{OL}$ = 12mA, $V_{CC}$ = 2.3V | | | 0.7 | |
| | | $V_{IL}$ = 0.8V, $I_{OL}$ = 12mA, $V_{CC}$ = 2.7V | | | 0.4 | |
| | | $V_{IL}$ = 0.8V, $I_{OL}$ = 24mA, $V_{CC}$ = 3.0V | | | 0.55 | |
| $I_{OH}$[3] | Output HIGH Current | $V_{CC}$ = 2.3V | | | –12 | mA |
| | | $V_{CC}$ = 2.7V | | | –12 | |
| | | $V_{CC}$ = 3.0V | | | –24 | |
| $I_{OL}$[3] | Output LOW Current | $V_{CC}$ = 2.3V | | | 12 | |
| | | $V_{CC}$ = 2.7V | | | 12 | |
| | | $V_{CC}$ = 3.0V | | | 24 | |

## DC Electrical Characteristics-Continued (Over the Operating Range, $T_A = -40°C$ to $+85°C$, $V_{CC} = 3.3V \pm 10\%$)

| Parameters | Description | Test Conditions(1) | Min. | Typ.(2) | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IN}$ | Input Current | $V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.6V$ | | | ±5 | µA |
| $I_{IN}$ (HOLD) | Input Hold Current | $V_{IN} = 0.7V$, $V_{CC} = 2.3V$ | 45 | | | |
| | | $V_{IN} = 1.7V$, $V_{CC} = 2.3V$ | –45 | | | |
| | | $V_{IN} = 0.8V$, $V_{CC} = 3.0V$ | 75 | | | |
| | | $V_{IN} = 2.0V$, $V_{CC} = 3.0V$ | –75 | | | |
| | | $V_{IN} = 0$ to $3.6V$, $V_{CC} = 3.6V$ | | | ±500 | |
| $I_{OZ}$ | Output Current (3-State Outputs) | $V_{OUT} = V_{CC}$ or GND, $V_{CC} = 3.6V$ | | | ±10 | |
| $I_{CC}$ | Supply Current | $V_{CC} = 3.6V$, $I_{OUT} = 0µA$, $V_{IN} =$ GND or $V_{CC}$ | | | 40 | |
| $\Delta I_{CC}$ | Supply Current per Input @ TTL HIGH | $V_{CC} = 3.0V$ to $3.6V$, One Input at $V_{CC} - 0.6V$, Other Inputs at $V_{CC}$ or GND | | | 750 | |
| $C_I$ | Control Inputs | $V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3V$ | | 3.5 | | pF |
| $C_O$ | Outputs | $V_O = V_{CC}$ or GND, $V_{CC} = 3.3V$ | | 9 | | |



**Notes:**
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$, +25°C ambient and maximum loading.
3. Unused Control Inputs must be held HIGH or LOW to prevent them from floating.

## Timing Requirements over Operating Range

| Parameters | Description | $V_{CC} = 2.5V \pm 0.2V$ | | $V_{CC} = 2.7V$ | | $V_{CC} = 3.3V \pm 0.3V$ | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_W$ | Pulse duration, LE1B, LE2B, LEA1B, or LEA2B High | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{SU}$ | Setup time, data before LE1B, LE2B, LEA1B, or LEA2B | 1.4 | | 1.1 | | 1.1 | | |
| $t_H$ | Hold time, data after LE1B, LE2B, LEA1B or LEA2B | 1.6 | | 1.9 | | 1.5 | | |
| $\Delta t/\Delta v$(1) | Input Transition Rise or Fall | 0 | 10 | 0 | 10 | 0 | 10 | ns/V |

**Note**:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

## Switching Characteristics over Operating Range[1]

| Parameters | From (Input) | To (Output) | $V_{CC}$ = 2.5V ± 0.2V | | $V_{CC}$ = 2.7V | | $V_{CC}$ = 3.3V ± 0.3V | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max.[2] | |
| $t_{PD}$ | A or B | B or A | 1.2 | 6.0 | | 5.1 | 1.2 | 4.3 | ns |
| | LE | A or B | 1.0 | 6.2 | | 5.2 | 1.0 | 4.4 | |
| | SEL | A | 1.2 | 7.5 | | 6.6 | 1.1 | 5.6 | |
| $t_{EN}$ | $\overline{OE}$ | A or B | 1.0 | 7.2 | | 6.4 | 1.0 | 5.4 | |
| $t_{DIS}$ | $\overline{OE}$ | A or B | 1.7 | 5.9 | | 5.0 | 1.3 | 4.6 | |



**Notes:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

## Operating Characteristics, $T_A$ = 25°C

| Parameter | | Test Conditions | $V_{CC}$ = 2.5V ± 0.2V | $V_{CC}$ = 3.3V ± 0.3V | Units |
|---|---|---|---|---|---|
| | | | Typical | | |
| $C_{PD}$ Power Dissipation Capacitance | Outputs Enabled | $C_L$ = 50pF, f = 10 MHz | 87 | 120 | pF |
| | Outputs Disabled | | 80.5 | 118 | |

## Power Supply Characteristics

| Parameters | Description | Test Conditions[1] | Min. | Typ[2] | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., Iout = 0V, Vin = GND or $V_{CC}$ | | | 40 | µA |
| $\Delta I_{CC}$ | Supply Current per Input @TTL HIGH | $V_{CC}$ = 3.0V to 3.6V, One input at $V_{CC}$ – 0.6V Other inputs at $V_{CC}$ or GND | | | 750 | |

**Note:**
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.