

**Product Features**

- PI74ALVTC family is designed for low voltage operation,  $V_{DD} = 1.8V$  to  $3.6V$
- Supports Live Insertion
- 3.6V I/O Tolerant Inputs and Outputs
- Bus Hold
- High Drive,  $-32/64mA @ 3.3V$
- Uses patented noise reduction circuitry
- Power-off high impedance inputs and outputs
- Industrial operation at  $-40^{\circ}C$  to  $+85^{\circ}C$
- Packages available:
  - 48-pin 240 mil wide plastic TSSOP (A)
  - 48-pin 173 mil wide plastic TVSOP (K)
  - 48-pin 300 mil wide plastic SSOP (V)

**Product Description**

Pericom Semiconductor’s PI74ALVTC series of logic circuits are produced in the Company’s advanced 0.35 micron CMOS technology, achieving industry leading speed.

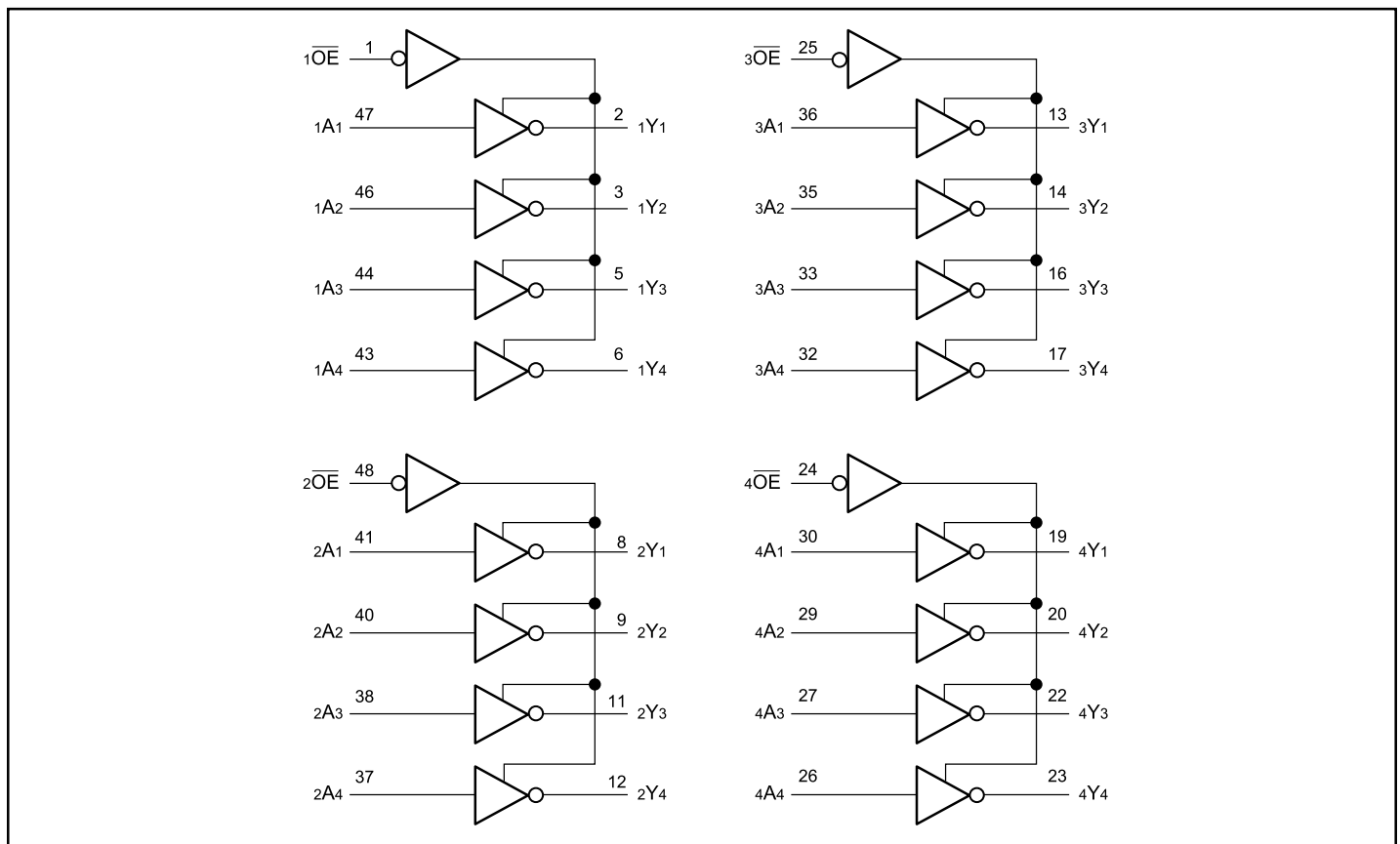
The PI74ALVTC16240 buffer/driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{DD}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The family offers both I/O Tolerant, which allows it to operate in mixed 1.8/3.6V systems, and “Bus Hold,” which retains the data input’s last state whenever the data input goes to high-impedance, preventing “floating” inputs and eliminating the need for pullup/down resistors.

**Logic Block Diagram**



### Product Pin Description

Pin Name	Description
$\overline{nOE}$	3-State Output Enable Inputs (Active LOW)
$nAx$	Inputs
$nYx$	3-State Outputs
GND	Ground
VCC	Power

### Truth Table<sup>(1)</sup>

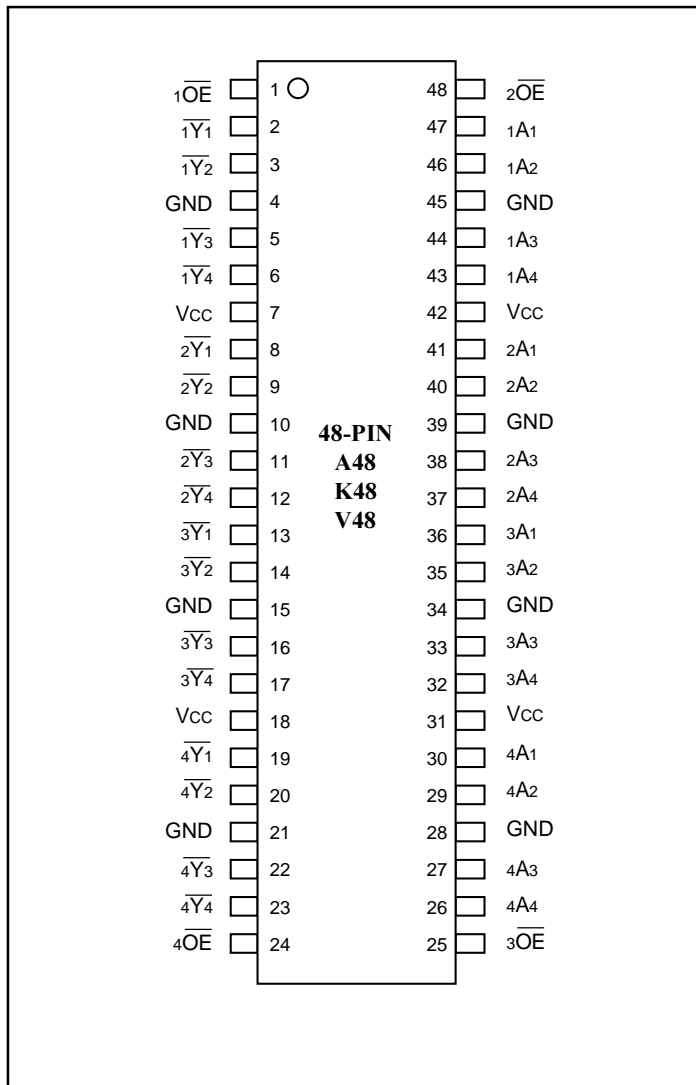
Inputs		Outputs
$\overline{nOE}$	$nAx$	$\overline{nYx}$
L	H	L
L	L	H
H	X	Z

#### Notes:

- H = High Signal Level  
L = Low Signal Level  
X = Don't Care or Irrelevant  
Z = High Impedance

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### Product Pin Configuration



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, $V_{DD}$ .....	-0.5V to 4.6V
Input Voltage Range, $V_I$ .....	-0.5V to 4.6V
Output Voltage Range, $V_O$ (3-States) .....	-0.5V to 4.6V
Output Voltage Range, $V_O^{(1)}$ (Active) .....	-0.5V to $V_{DD} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$ .....	-50mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$ .....	-50mA
$V_O > V_{DD}$ .....	$\pm 50mA$
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ ) .....	-64/128mA
DC $V_{DD}$ or GND Current per Supply Pin ( $I_{CC}$ or GND) .....	$\pm 100mA$
Storage Temperature Range, $T_{stg}$ .....	-65°C to 150°C

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended Operating Conditions<sup>2</sup>

			Min.	Max.	Units
$V_{DD}$	Supply voltage	Operating	1.8	3.6	V
		Data Retention Only	1.2	3.6	
$V_{IH}$	High-level input voltage	$V_{DD} = 2.7V$ to 3.6V	2.0		
$V_{IL}$	Low-level input voltage	$V_{DD} = 2.7V$ to 3.6V		0.8	
$V_I$	Input voltage		-0.3	3.6	
$V_O$	Output voltage	Active State	0	$V_{DD}$	
		Off State	0	3.6	
	Output current in $I_{OH}/I_{OL}$	$V_{DD} = 3.0V$ to 3.6V $V_{DD} = 3.0V$ to 3.6V $V_{DD} = 2.3V$ to 2.7V $V_{DD} = 1.8V$		-32/64 $\pm 24$ $\pm 18$ $\pm 6$	mA
$\Delta t/\Delta v$	Input transition rise or fall rate <sup>(3)</sup>		0	10	ns/V
$T_A$	Operating free-air temperature		-40	85	C

#### Notes

1. Absolute maximum of  $I_O$  must be observed.
2. Unused control inputs must be held HIGH or LOW to prevent them from floating.
- 3 As measured between 0.8V and 2.0V,  $V_{DD} = 3.0V$ .

**Electrical Characteristics over Recommended Operating Free-Air Temperature Range**

(unless otherwise noted)

**DC Characteristics (2.7V <math>V\_{DD}</math> ≤ 3.6V)**

	Parameter	Conditions	$V_{DD}$	Min.	Typ.	Max.	Units
$V_{IH}$	HIGH Level Input Voltage		2.7 - 3.6	2.0			V
$V_{IL}$	LOW Level Input Voltage					0.8	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100\mu A$		$V_{DD} - 0.2$			
		$I_{OH} = -12mA$	2.7	2.2			
		$I_{OH} = -18mA$	3.0	2.4			
		$I_{OH} = -24mA$		2.2			
		$I_{OH} = -32mA$		2.0			
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100\mu A$	2.7 - 3.6			0.2	
		$I_{OL} = 12mA$	2.7			0.4	
		$I_{OL} = 18mA$	3.0			0.4	
		$I_{OL} = 24mA$		0.45			
		$I_{OL} = 32mA$		0.5			
		$I_{OL} = 64mA$		0.55			
$I_I$	Input Leakage Current	$V_I = V_{DD}$ , or GND	3.6			±5.0	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$V_O = 3.6V$	2.7			±10	
$I_{OFF}$	Power-OFF Leakage Current	$V_I$ or $V_O \leq 3.6V$	0			10	
$I_{ODL}$	Output Current Low	$V_{IN} = V_{IH}$ or $V_{IL}$ , $V_O = 1.5V^{(1)}$	3.6	150		334	mA
$I_{ODH}$	Output Current High	$V_{IN} = V_{IH}$ or $V_{IL}$ , $V_O = 1.5V^{(1)}$		-58		-114	
$I_{HOLD}$	Bus Hold Current A or B Outputs	$V_I = 0.8V$	3.0	75			$\mu A$
		$V_I = 2.0V$		-75			
		$V_I = 0$ to 3.6V	3.6			±500	
$I_{DD}$	Quiescent Supply Current	$V_I = V_{DD}$ or GND	2.7 - 3.6			50	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				±50	
$\Delta I_{DD}$	Increase in $I_{DD}$ per input	$V_{IH} = V_{DD} - 0.6V$ , Other inputs at $V_{DD}$ or Gnd					

**Notes**

1. Duration of test must not exceed 1 second with only 1 output tested at a time.

**Electrical Characteristics over Recommended Operating Free-Air Temperature Range**  
(unless otherwise noted)

**DC Characteristics (2.3V <math>V\_{DD}</math> ≤ 2.7V)**

Description	Parameters	Conditions	$V_{DD}$	Min.	Typ.	Max.	Units
$V_{IH}$	HIGH Level Input Voltage		2.3 - 2.7	1.6			V
$V_{IL}$	LOW Level Input Voltage					0.7	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$		$V_{DD} - 0.2$			
		$I_{OH} = -12 \text{ mA}$	2.3	1.8			
		$I_{OH} = -18 \text{ mA}$		1.7			
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 2.7			0.2	
		$I_{OL} = 12 \text{ mA}$	2.3			0.4	
		$I_{OL} = 18 \text{ mA}$				0.5	
		$I_{OL} = 24 \text{ mA}$				0.55	
$I_I$	Input Leakage Current	$V_I = V_{DD}$ or GND	2.7			±5.0	
$I_{OZ}$	3-STATE Output Leakage	$V_O = 3.6V$	2.3			±10	
$I_{OFF}$	Power-OFF Leakage Current	$V_I$ or $V_O \leq 3.6V$	0			10	
$I_{ODL}$	Output Current Low	$V_{IN} = V_{IH}$ or $V_{IL}$ , $V_O = 1.5V^{(2)}$	2.7	110		264	mA
$I_{ODH}$	Output Current High	$V_{IN} = V_{IH}$ or $V_{IL}$ , $V_O = 1.5V^{(2)}$			-30		
$I_{HOLD}^{(1)}$	Bus Hold Current A or B Outputs	$V_I = 0.7V$	2.5		90		$\mu A$
		$V_I = 1.7V$			-90		
$I_{DD}$	Quiescent Supply Current	$V_I = V_{DD}$ or GND	2.3 - 2.7			20	$\mu A$
		$V_{DD} \leq (V_P, V_O) \leq 3.6V$				±20	
$\Delta I_{DD}$	Increase in $I_{DD}$ per input	$V_{IH} = V_{DD} - 0.6V$ , Inputs at $V_{DD}$ or Gnd					

**Notes:**

1. Not Guaranteed
2. Duration of test must not exceed 1 second with only 1 output tested at a time.

**Electrical Characteristics over Recommended Operating Free-Air Temperature Range**  
(unless otherwise noted)

**DC Characteristics (1.8V <math>V\_{DD}</math> ≤ 2.3V)**

Description	Parameters	Conditions	$V_{DD}$	Min.	Typ.	Max.	Units	
$V_{IH}$	HIGH Level Input Voltage		1.8 - 2.3	$0.7 \times V_{DD}$			V	
$V_{IL}$	LOW Level Input Voltage					$0.2 \times V_{DD}$		
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100\mu A$	1.8	$V_{DD} - 0.2$				
		$I_{OH} = -6mA$		1.4				
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100\mu A$				0.2		
		$I_{OL} = 6mA$				0.3		
$I_I$	Input Leakage Current	$V_I = V_{DD}$ or GND	2.3			±5.0	μA	
$I_{OZ}$	3-STATE Output Leakage	$V_O = 3.6V$	1.8			±10		
$I_{OFF}$	Power-OFF Leakage Current	$V_I = V_O \leq 3.6V$	0			10		
$I_{ODL}$	Output Current Low	$V_{IN} = V_{IH}$ or $V_{IL}$ , $V_O = 0.9V^{(2)}$	1.8	50		137	mA	
$I_{ODH}$	Output Current High	$V_{IN} = V_{IH}$ or $V_{IL}$ , $V_O = 0.9V^{(2)}$		-14		-34		
$I_{HOLD}^{(1)}$	Bus Hold Current A or B Outputs	$V_I = 0.4$	1.8		50		μA	
		$V_I = 1.3$			-50			
$I_{DD}$	Quiescent Supply Current	$V_I = V_{DD}$ or GND						20
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$						±20
$\Delta I_{DD}$	Increase in $I_{DD}$ per input	$V_I = V_{DD} - 0.6V$ , Other inputs at $V_{DD}$ or GND						400

**Notes:**

1. Not Guaranteed
2. Duration of test must not exceed 1 second with only 1 output tested at a time.

**AC Electrical Characteristics**

Symbol	Parameter	TA = -40°C to +85°C, CL = 50pF, RL = 500Ω						Units
		VDD = 3.3V ±0.3V		VDD = 2.5V ±0.2V		VDD = 1.8V		
		Min.	Max.	Min.	Max.	Min.	Max.	
tPHL, tPLH	Prop Delay	0.5	2.6	1.0	2.9	1.5	3.5	ns
tPZL, tPZH	Output Enable Time	1.0	3.0	1.0	4.2	1.5	4.8	
tPLZ, tPHZ	Output Disable Time	1.5	3.4	1.0	3.0	1.5	3.8	
tOSHL tOSLH	Output to Output Skew <sup>(1)</sup>		0.5		0.5		0.5	

**Note:**

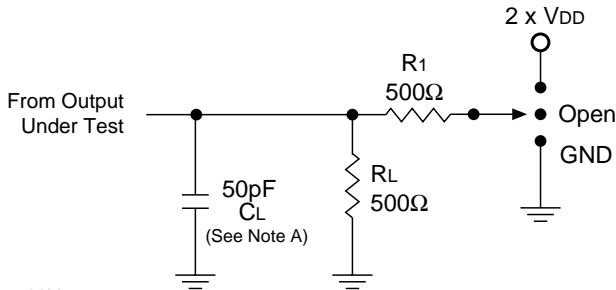
1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH or LOW (tOSHL) or LOW to HIGH (tOSLH).

**Capacitance**

Symbol	Parameter	Conditions	TA = +25°C Typical	Units
CIN	Input Capacitance	VDD = 1.8, 2.5V or 3.3V, VI = 0V or VDD	6	pF
COUT	Output Capacitance	VI = 0V or VDD, VDD = 1.8V, 2.5V or 3.3V	7	
C <sub>PD</sub>	Power Dissipation Capacitance	VI = 0V or VDD, F = 10 MHz VDD = 1.8V, 2.5V or 3.3V	20	

### Test Circuits and Switching Waveforms

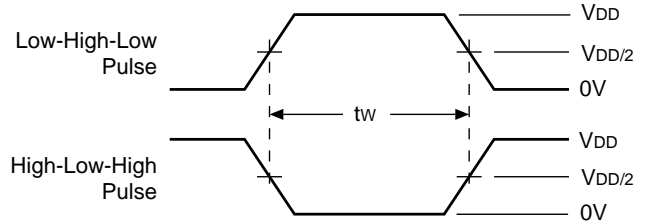
#### Parameter Measurement Information ( $V_{DD} = 1.8V - 3.6V$ )



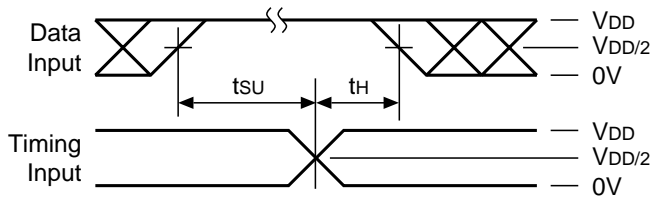
#### Switch Position

Test	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{DD}$
$t_{PHZ}/t_{PZH}$	GND

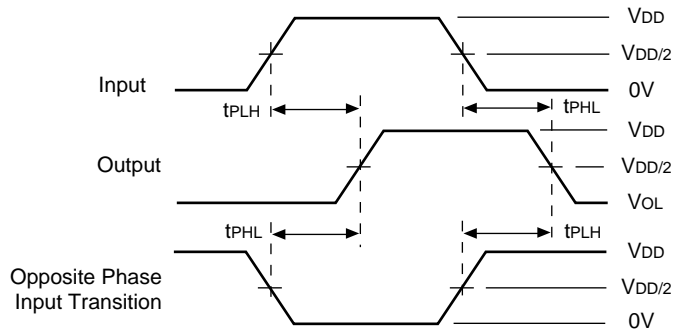
#### Pulse Width



#### Setup, Hold, and Release Timing



#### Propagation Delay



#### Notes:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50\Omega$ ,  $t_r \leq 2\text{ns}$ ,  $t_f \leq 2\text{ns}$ , *measured from 10% to 90%, unless otherwise specified.*
- D. The outputs are measured one at a time with one transition per measurement.

#### Enable Disable Timing

