Fast CMOS 16-Bit Heavy Buffer/Line Drivers

Product Features:

- Very high-speed buffer drivers for 150 pF heavy load and all 16-bit switching in 4.8ns max
- Meets JEDEC specification for DRAM DIMM module buffer propagation delay
- Low noise drivers: minimal undershoot/ringback and typical V_{OLP} (output ground bounce) < 0.6V
- Packages available:
  – 48-pin 240-mil wide plastic TSSOP (A)
  – 48-pin 300-mil wide plastic SSOP (V)

Product Description:

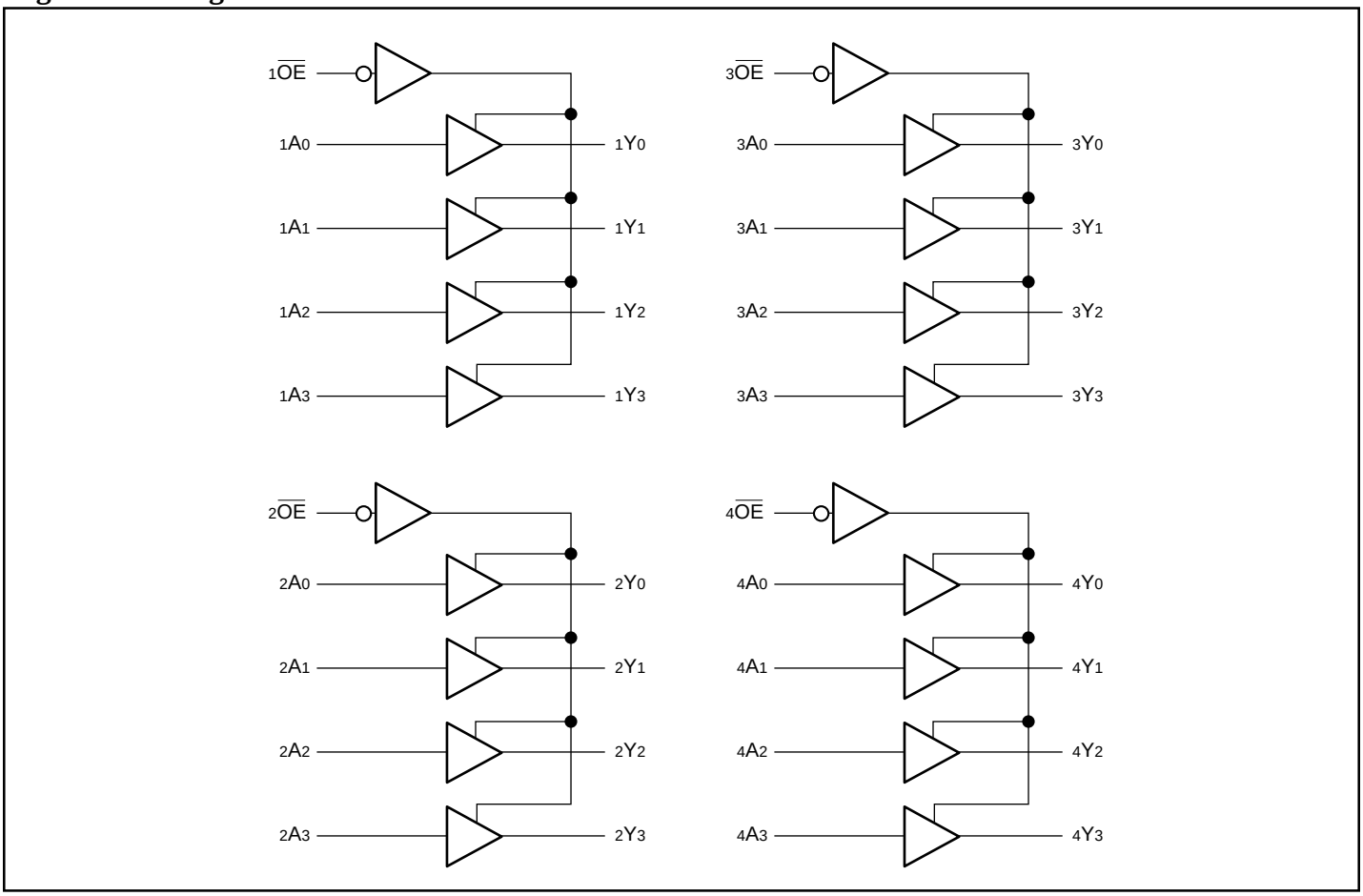
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced CMOS technology, achieving industry leading speed grades.

The PI74FCT162244MT is a non-inverting 16-bit buffer/line driver designed specifically for applications driving heavy loads—ideally for DRAM modules/arrays and heavy load bus applications. This very high-speed, high-drive, low noise buffer driver device meets the JEDEC specification for DRAM DIMM module buffer drivers.

The PI74FCT162244MT offers a flow-through organization for ease of board layout. This part is plug-in compatible with the 74ABT16244/162244 and excels in applications where much higher speed and lower power dissipation are required.

The output drivers of the PI74FCT162244MT have the features of a balanced drive and controlled edge rate, resulting in minimal undershoot/ringback and ground bounce. This eliminates the need for external series termination resistors.

Logic Block Diagram



Product Pin Description

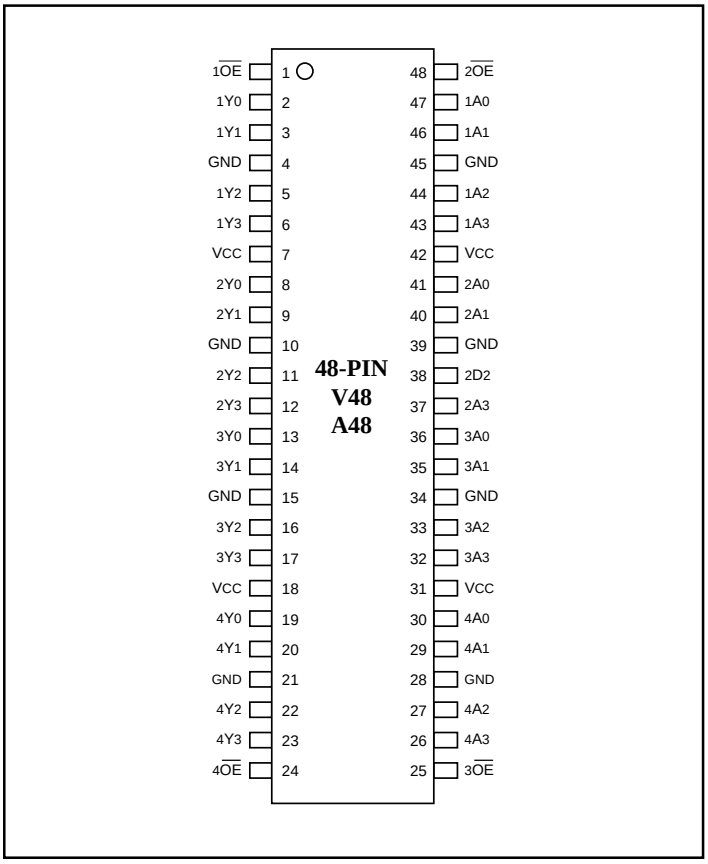
Pin Name	Description
x$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
xAx	Inputs
xYx	3-State Outputs
GND	Ground
VCC	Power

Truth Table

Inputs[1]		Outputs[1]
x$\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

Note: 1. H = High Voltage Level
X = Don't Care
L = Low Voltage Level
Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current	V_{CC} = Max.	V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max.[3], V_{OUT} = 2.5V		–50		–180	mA
V_H	Input Hysteresis				100		mV

Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24.0 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.3	0.55	V
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} OR V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} OR V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10 MHz 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		0.6	1.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		0.9	2.3[5]	
		V_{CC} = Max., Outputs Open f_i = 2.5 MHz 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND		2.4	4.5[5]	
			V_{IN} = 3.4V V_{IN} = GND		6.4	16.5[5]	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range - High-LoadCondition

Parameters	Description	Conditions[1]	162244MT Com. Min	162244MT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay[2] xAx to xYx	C_L = 150 pF All 16 Bits Switching	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xAx or xYx	C_L = 50 pF R_L = 500Ω	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] x$\overline{OE}$ to xAx or xYx		1.5	5.6	ns
$t_{SK}(o)$	Output Skew[4]		—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Application Note

Almost all propagation delay specifications in standard data books are specified for one single bit switching, not multiple-bit switching. The propagation delay t_{PLH}/t_{PHL} of a buffer driver increases very significantly for all 16 bits switching simultaneously, as compared with one single bit switching.

For realistic heavy load applications such as DRAM modules and per JEDEC DRAM module specification, the driver propagation delay should be specified for all 16 bits switching worst case. The specification for one single bit switching in standard data books has no useful meaning.

The following PI74FCT162244MT test data are tested ***under 150 pF heavy loads and all 16 bits switching simultaneously:***

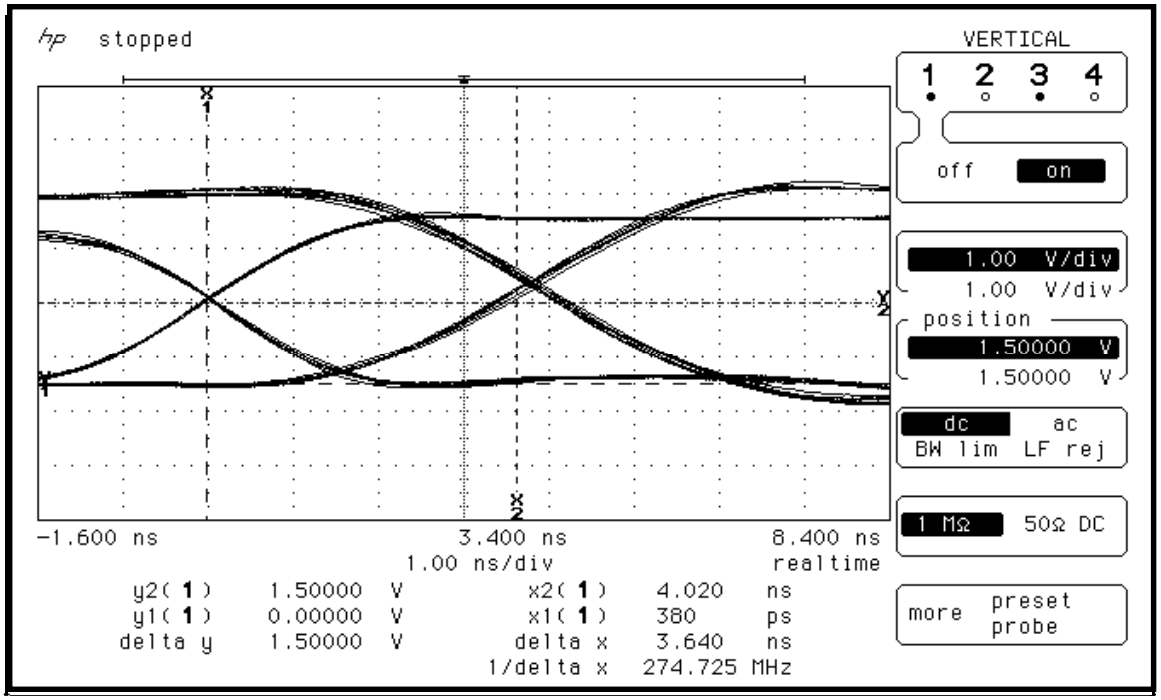


Figure 1. Vertical voltage scale is 1.0V/div. Reference voltage level y2 at the middle is 1.5V. Horizontal time scale is 1.0 ns/div. For PI74FCT162244MT with 150 pF loads, all 16 bits switching, the propagation delay t_{PLH} is 3.64 ns. Minimal undershoot and overshoot.

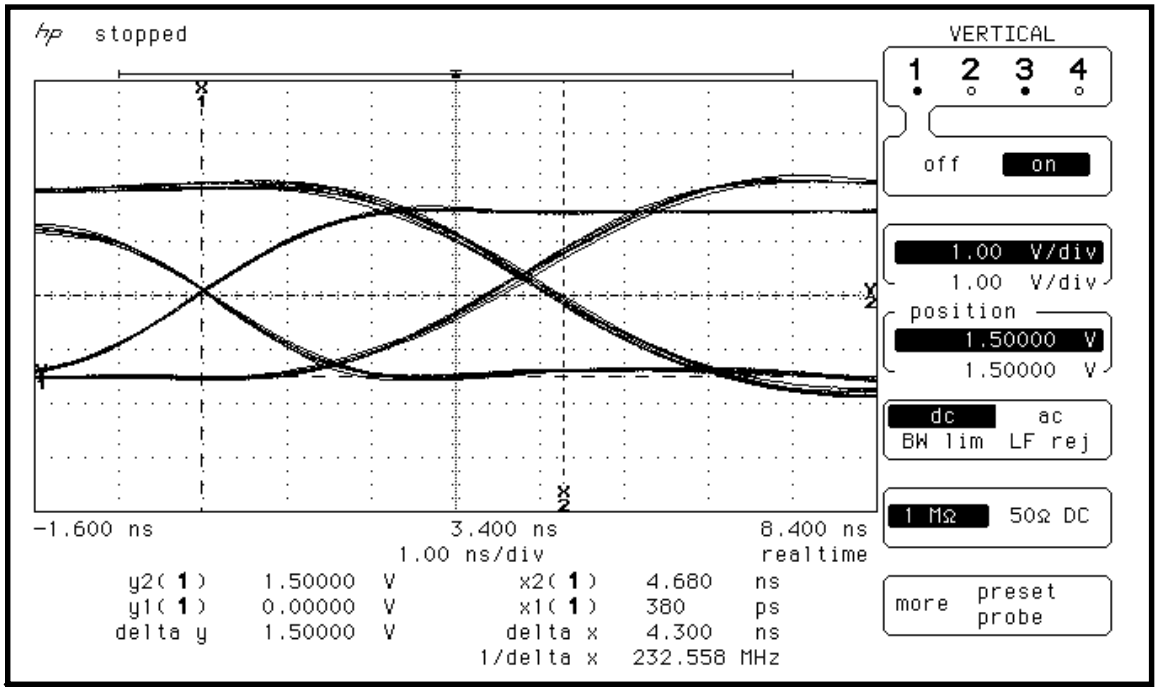


Figure 2. For PI74FCT162244MT, with 150pF load, all 16 bits switching, the propagation delay t_{PHL} is 4.3ns.

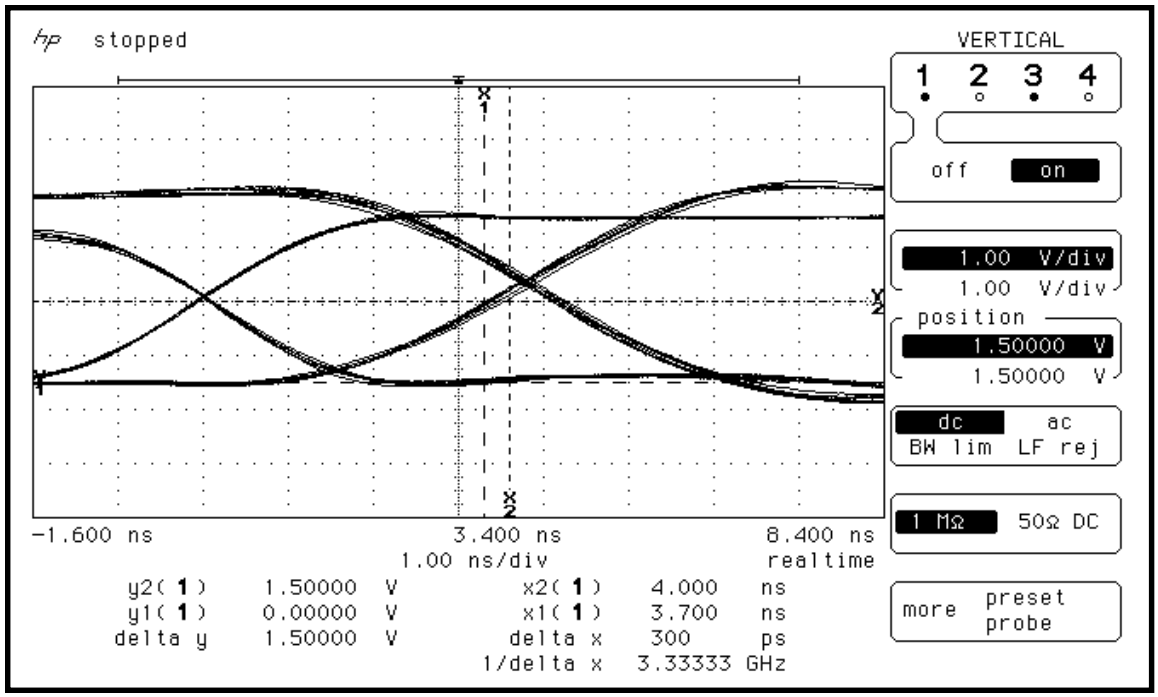


Figure 3. For PI74FCT162244MT, Output Skew t_{LH} of less than 300 ps under 150 pF load, and all 16 bits switching.

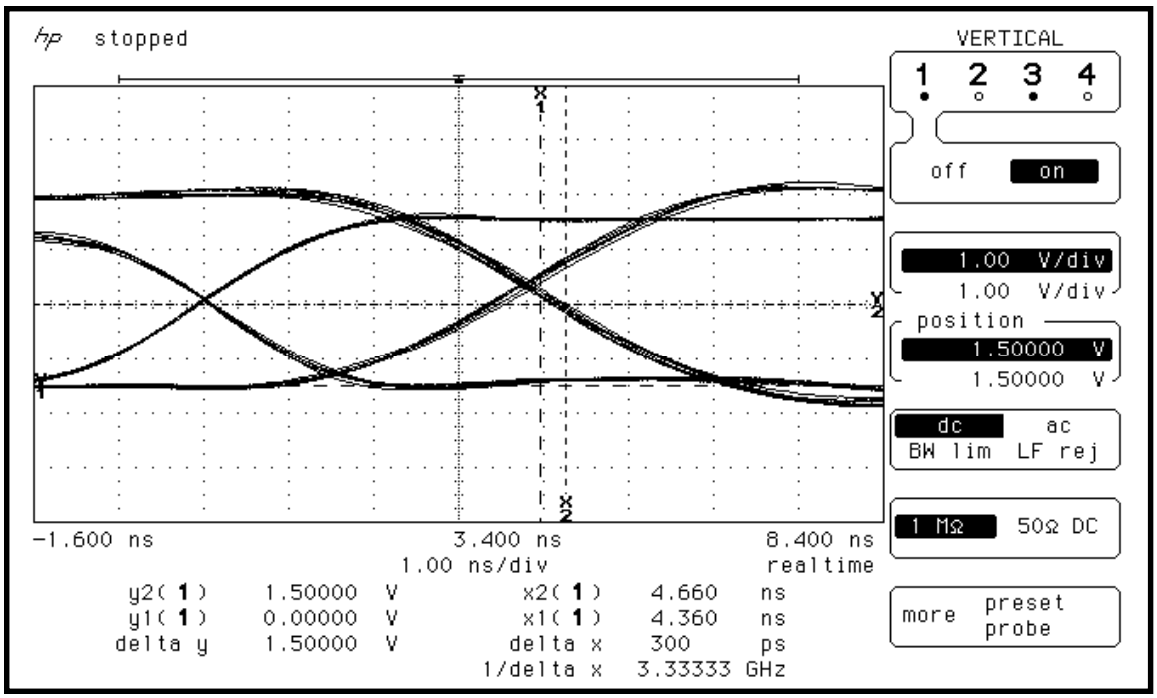


Figure 4. For PI74FCT162244MT, Output Skew t_{HL} is less than 300 ps under 150 pF load, and all 16 bits switching.