

Product Features

- Compatible with LCX™ and LVT™ families of products
- Supports 5V tolerant mixed signal mode operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced low power CMOS operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Packages available:
 - 24-pin 173-mil wide plastic TSSOP (L)
 - 24-pin 150-mil wide plastic QSOP (Q)
 - 24-pin 150-mil wide plastic TQSOP (R)
 - 24-pin 300-mil wide plastic SOIC (S)

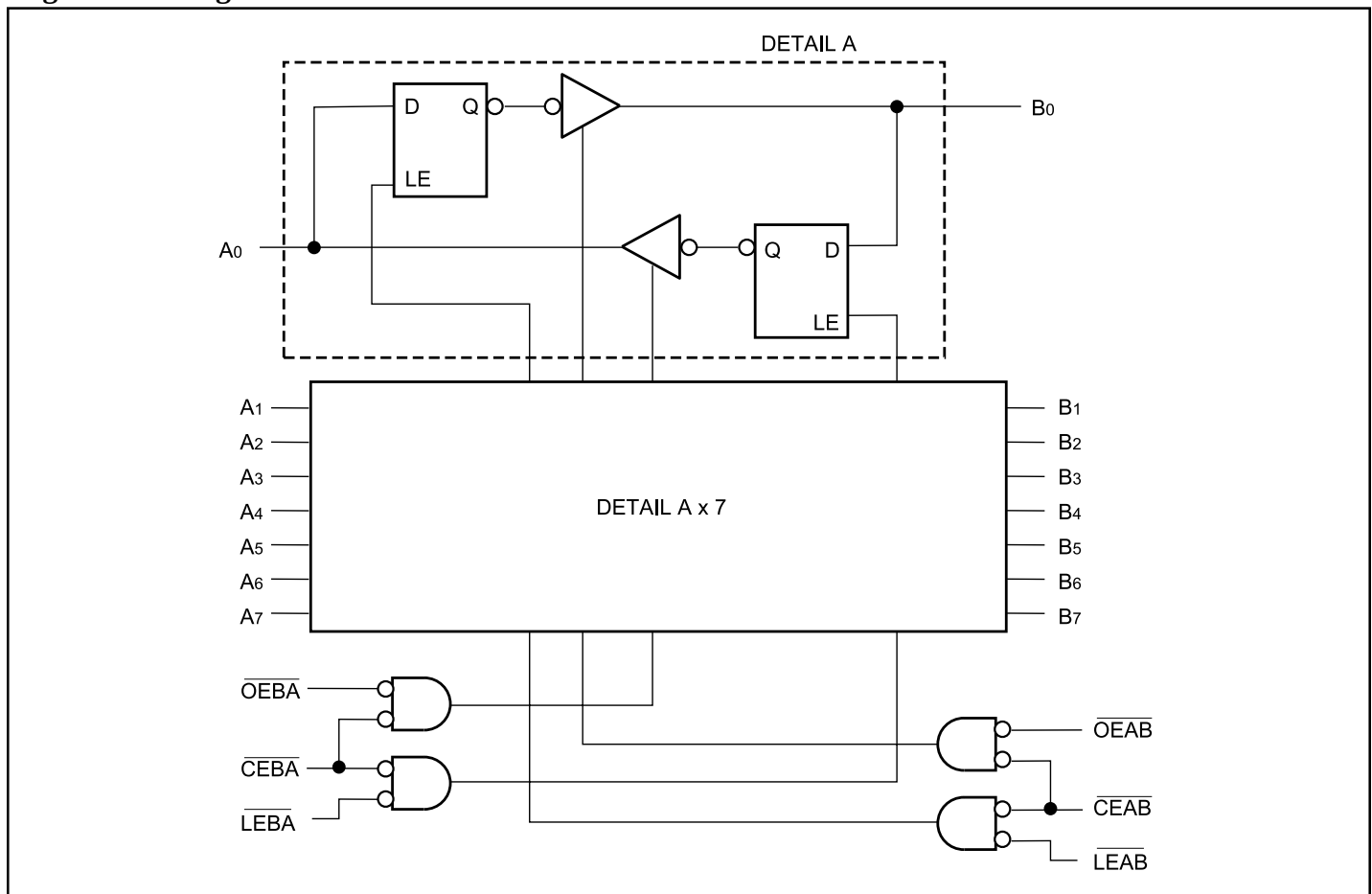
Product Description

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

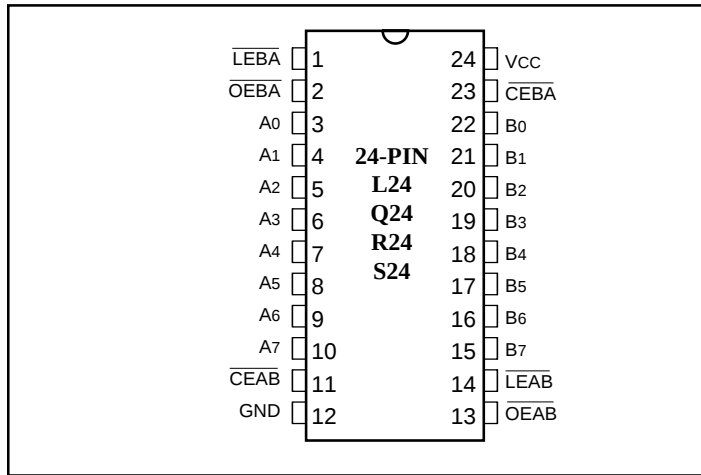
The PI74LPT543 is an 8-bit wide non-inverting transceiver designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (CEAB) input must be LOW in order to enter data from A0–A7 or to take data from B0–B7, as indicated in the Truth Table. With $\overline{\text{CEAB}}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With CEAB and $\overline{\text{OEAB}}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{\text{CEAB}}$, $\overline{\text{LEAB}}$, and $\overline{\text{OEAB}}$ inputs.

The PI74LPT543 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A0-A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0-B7	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
VCC	Power

Truth Table (Non-Inverting)^(1,2) For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0-B7
H	X	X	Storing	High-Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

Notes:

- *Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care or Irrelevant
- A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) ..	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	5.5	V
V _{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max.	V _{IN} = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)	V _{CC} = Max.	V _{IN} = V _{CC}	—	—	±1	μA
I _{IL}	Input LOW Current (Input pins)	V _{CC} = Max.	V _{IN} = GND	—	—	±1	μA
	Input LOW Current (I/O pins)	V _{CC} = Max.	V _{IN} = GND	—	—	±1	μA
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = Max.	V _{OUT} = 5.5V	—	—	±1	μA
I _{OZL}		V _{CC} = Max.	V _{OUT} = GND	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = –18 mA		—	–0.7	–1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾		–36	–60	–110	mA
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾		50	90	200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = –0.1 mA	V _{CC} –0.2	—	—	V
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = –3 mA	2.4	3.0	—	V
		V _{CC} = 3.0V,	I _{OH} = –8 mA	2.4 ⁽⁵⁾	3.0	—	V
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = –24 mA	2.0	—	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 0.1 mA	—	—	0.2	V
		V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16 mA	—	0.2	0.4	V
			I _{OL} = 24 mA	—	0.3	0.5	V
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		–60	–85	–240	mA
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V		—	—	±100	μA
V _H	Input Hysteresis			—	150	—	mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} – 0.6V at rated current.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ.	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} – 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open <u>CEAB</u> and <u>OEAB</u> = GND <u>CEBA</u> = V _{CC} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle <u>CEAB</u> and <u>OEAB</u> = GND <u>CEBA</u> = V _{CC} One Bit Toggling	V _{IN} = V _{CC} – 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle <u>CEAB</u> and <u>OEAB</u> = GND <u>CEBA</u> = V _{CC} 8 Bits Toggling	V _{IN} = V _{CC} – 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (f_{CP}/2 + f_iN_i)
I_{CC} = Quiescent Current (I_{CC}L, I_{CC}H and I_{CC}Z)
ΔI_{CC} = Power Supply Current for a TTL High Input
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
N_{CP} = Number of Clock Inputs at f_{CP}
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT543		LPT543A		LPT543C		Units
			Com.		Com.		Com.		
			Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.	
tPLH tPHL	Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	$C_L = 50\text{ pF}$ $R_L = 500\Omega$	2.5	8.5	2.5	6.5	2.5	5.3	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to A_N , $\overline{LEAB}$ to B_N		2.5	12.5	2.5	8.0	2.5	7.0	ns
tpZH tpZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N		2.0	12.0	2.0	9.0	2.0	8.0	ns
tpZH tpZL	Output Disable Time ⁽³⁾ $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N		2.0	9.0	2.0	7.5	2.0	6.5	ns
tsu	Setup Time, $\overline{HIGH}$ or $\overline{LOW}$ A_N or B_N to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	2.0	—	2.0	—	ns
th	Hold Time, $\overline{HIGH}$ or $\overline{LOW}$ A_N or B_N to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	ns
tw	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width $\overline{LOW}$ ⁽³⁾		5.0	—	5.0	—	5.0	—	ns

Notes:

1. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, normal range. For $V_{CC} = 2.7V$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.