

**3.3V 8-Bit Bi-Directional Transceiver  
with 3-State Outputs**
**Product Features**

- Advanced low power CMOS design for 2.7V to 3.6V  $V_{CC}$  operation
- Supports 5V input/output tolerance in mixed signal mode operation
- Function compatible with LVT family of products
- Balanced  $\pm 24\text{mA}$  output drive
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8\text{V}$  at  $V_{CC}=3.3\text{V}$ ,  $T_A=25^\circ\text{C}$
- $I_{off}$  and Power Up/Down 3-State support live insertion
- Latch-up performance exceeds 200mA Per JESD78
- ESD protection exceeds JESD 22
  - 2000V Human-Body Model (A114-B)
  - 200V Machine Model (A115-A)
- Packages (Pb-free available):
  - 20-pin 209-mil wide plastic SSOP (H)
  - 20-pin 173-mil wide plastic TSSOP (L)
  - 20-pin 300-mil wide plastic SOIC (S)

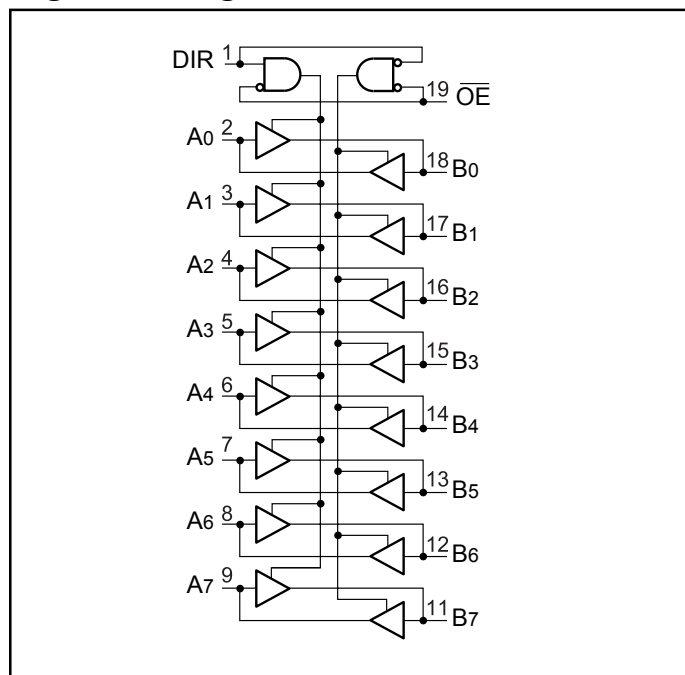
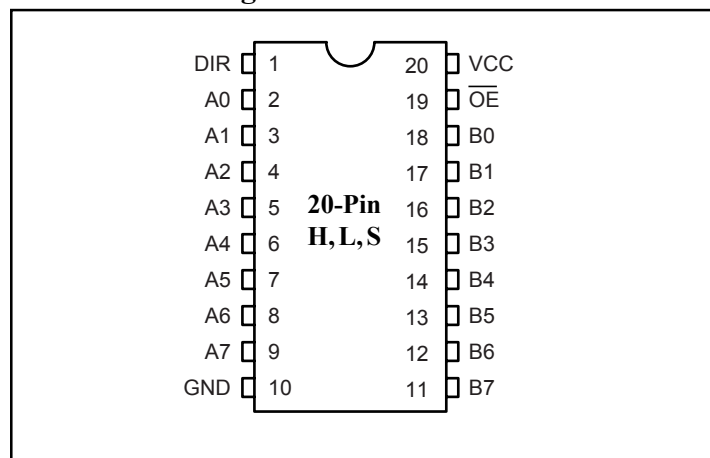
**Product Description**

Pericom Semiconductor's PI74LVTC series of logic circuits are produced using the Company's advanced CMOS technology, achieving industry leading speed.

The PI74LVTC245 is a non-inverting 8-bit Bidirectional Transceiver designed for low-voltage 2.7V to 3.6V  $V_{CC}$  operation, with the capability of interfacing to the 5V system environment. This transceiver is designed for asynchronous two-way communication between data buses. The direction control input pin (DIR) determines the direction of the dataflow from the A bus to the B bus or from the B bus to the A bus. The output enable ( $\overline{OE}$ ) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

When  $V_{cc}$  is between 0 to 1.5V during power up or power down, the outputs of the device are in the high-impedance state. To ensure the high-impedance state above 1.5V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The device fully supports live-insertion with its  $I_{off}$  and power-up/down 3-state. The  $I_{off}$  circuitry disables the outputs when the power is off, preventing the backflow of damaging current through the device. Power-up/down 3-state places the outputs in the high-impedance state during power up or power down, preventing driver conflict.

**Logic Block Diagram**

**Product Pin Configuration**




**Recommended Operating Conditions<sup>(5)</sup>**

		Min.	Max.	Units	
V <sub>CC</sub>	Supply Voltage	Operating	2.7	3.6	V
V <sub>IH</sub>	High-level Input Voltage	V <sub>CC</sub> = 2.7V to 3.6V	2.0		
V <sub>IL</sub>	Low-level Input Voltage	V <sub>CC</sub> = 2.7V to 3.6V		0.8	
V <sub>I</sub>	Input Voltage	0	5.5		
V <sub>O</sub>	Output Voltage	High or Low State	0	V <sub>CC</sub>	
		3-State	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7V		- 12	mA
		V <sub>CC</sub> = 3.0V to 3.6V		- 24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7V		12	
		V <sub>CC</sub> = 3.0V to 3.6V		24	
Δt/ΔV	Input transition rise or fall rate			6	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		150		μs/V
T <sub>A</sub>	Operating free-air temperature		- 40	85	°C

**Notes:**

5. All unused inputs must be held at V<sub>CC</sub> or GND to ensure proper device operation.

**DC Electrical Characteristics** (Over the Operating Range,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

Parameters	Description		Test Conditions		Min.	Max.	Units
$V_{IK}$	Clamp Diode Voltage		$V_{CC} = 2.7\text{V}$	$I_I = -18\text{mA}$		-1.2V	V
$V_{OH}$	Output High Voltage		$V_{CC} = 2.7\text{V to } 3.6\text{V}$	$I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2\text{V}$		
			$V_{CC} = 2.7\text{V}$	$I_{OH} = -12\text{mA}$	2.2		
			$V_{CC} = 3\text{V}$	$I_{OH} = -12\text{mA}$	2.4		
				$I_{OH} = -24\text{mA}$	2.2		
$V_{OL}$	Output Low Voltage		$V_{CC} = 2.7\text{V to } 3.6\text{V}$	$I_{OL} = 100\mu\text{A}$		0.2	
			$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$		0.4	
			$V_{CC} = 3\text{V}$	$I_{OL} = 12\text{mA}$		0.4	
				$I_{OL} = 24\text{mA}$		0.55	
$I_I$	Input Leakage Current	Control Inputs	$V_{CC} = 0\text{V to } 3.6\text{V}$	$V_I = 0\text{V to } 5.5\text{V}$		$\pm 5$	
		A or B Ports <sup>(6)</sup>	$V_{CC} = 3.6\text{V}$	$V_I = 5.5\text{V}$		$\pm 5$	
				$V_I = V_{CC}$			
$V_I = \text{GND}$							
$I_{OFF}$	Power Off Output Leakage Current		$V_{CC} = 0\text{V}$	$V_I$ or $V_O = 0\text{V to } 5.5\text{V}$		$\pm 5$	
$I_{OZPU}$	Power-Up 3-State Current		$V_{CC} = 0\text{V to } 1.5\text{V}$	$V_O = 0.5\text{V to } 5.5\text{V}$ , $\overline{OE} = \text{don't care}$		$\pm 5$	
$I_{OZPD}$	Power-Down 3-State Current		$V_{CC} = 1.5\text{V to } 0\text{V}$	$V_O = 0.5\text{V to } 5.5\text{V}$ , $\overline{OE} = \text{don't care}$		$\pm 5$	
$I_{CC}$	Quiescent Power Supply Current		$V_{CC} = 2.7\text{V to } 3.6\text{V}$	$V_I = V_{CC}$ or GND $3.6\text{V} \leq V_I \leq 5.5\text{V}^{(7)}$	$I_O = 0$	100	
$\Delta I_{CC}$	Increase in $I_{CC}$		$V_{CC} = 3.0\text{V to } 3.6\text{V}$	One input at $V_{CC} - 0.6\text{V}^{(8)}$ , Other inputs at $V_{CC}$ or GND		500	

**Notes:**

6. For I/O ports, Input Leakage Current ( $I_I$ ) includes the 3-state Output Leakage Current. Unused pins are at  $V_{CC}$  or GND.
7. This applies in the disabled state only.
8. This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

### Capacitance

Parameters	Description	Test Conditions	Typ. <sup>(9)</sup>	Units
C <sub>IN</sub>	Control Input Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = V <sub>CC</sub> or GND	3.3	pF
C <sub>IO</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>O</sub> = V <sub>CC</sub> or GND	7.8	
C <sub>PD</sub>	Power Dissipation Capacitance <sup>(10)</sup>	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0 or V <sub>CC</sub> , f=10 MHz	33	

**Notes:**

9. All typical values are measured at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

10. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle, C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression: I<sub>CCD</sub> = (C<sub>PD</sub>)(V<sub>CC</sub>)(f<sub>IN</sub>)+(I<sub>CCstatic</sub>).

### Switching Characteristics Over Operating Range

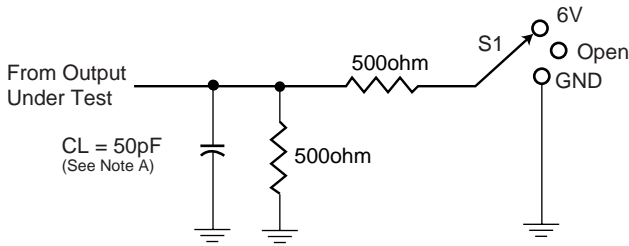
Parameters	Description	From (Input)	To (Output)	V <sub>CC</sub> = 3.3V ±0.3V		V <sub>CC</sub> = 2.7V		Units
				C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ohm		C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ohm		
				Min	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay	A or B	B or A	1.0	5.4	1.0	5.8	ns
t <sub>PHL</sub>				1.0	5.4	1.0	5.8	
t <sub>PZH</sub>	Output Enable Time	$\overline{OE}$	A or B	1.0	7.0	1.0	7.9	
t <sub>PZL</sub>				1.0	7.0	1.0	7.9	
t <sub>PHZ</sub>	Output Disable Time	$\overline{OE}$	A or B	1.0	5.4	1.0	5.8	
t <sub>PLZ</sub>				1.0	5.4	1.0	5.8	
t <sub>SK(O)</sub>	Output to Output Skew <sup>(11)</sup>				0.5			

**Notes:**

11. Skew between any two outputs, switching in the same direction.

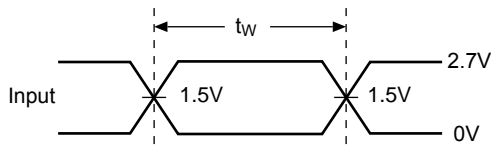
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.7V$  and  $3.3V \pm 0.3V$

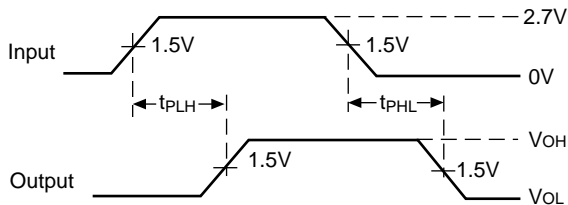


Test	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6V
$t_{PHZ}/t_{PZH}$	GND

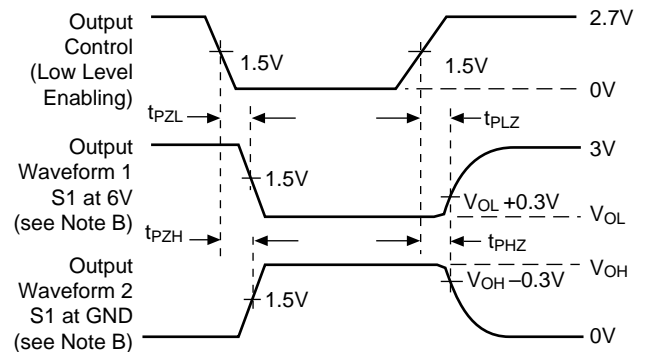
**Load Circuit**



**Voltage Waveforms  
Pulse Duration**



**Voltage Waveforms  
Propagation Delay Times**



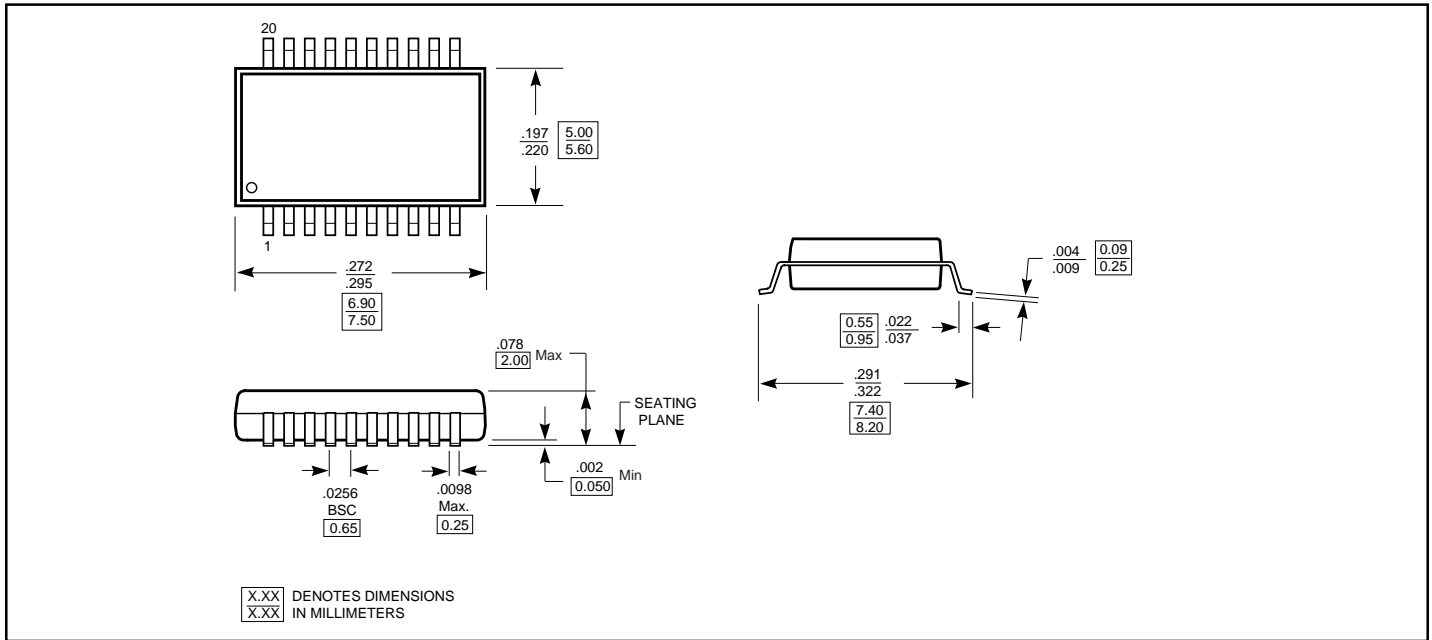
**Voltage Waveforms  
Enable and Disable Times**

**Figure 1. Load Circuit and Voltage Waveforms**

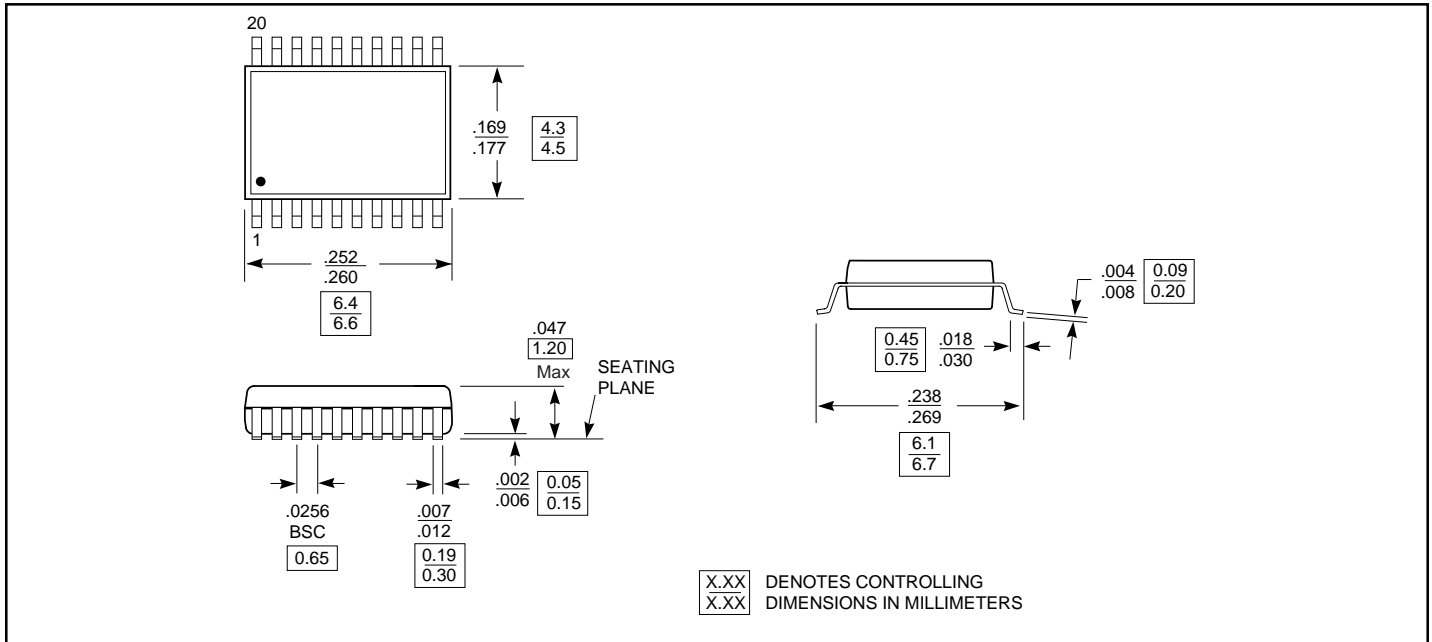
**Notes:**

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50\text{ohm}$ ,  $t_R \leq 2.5\text{ns}$ ,  $t_F \leq 2.5\text{ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

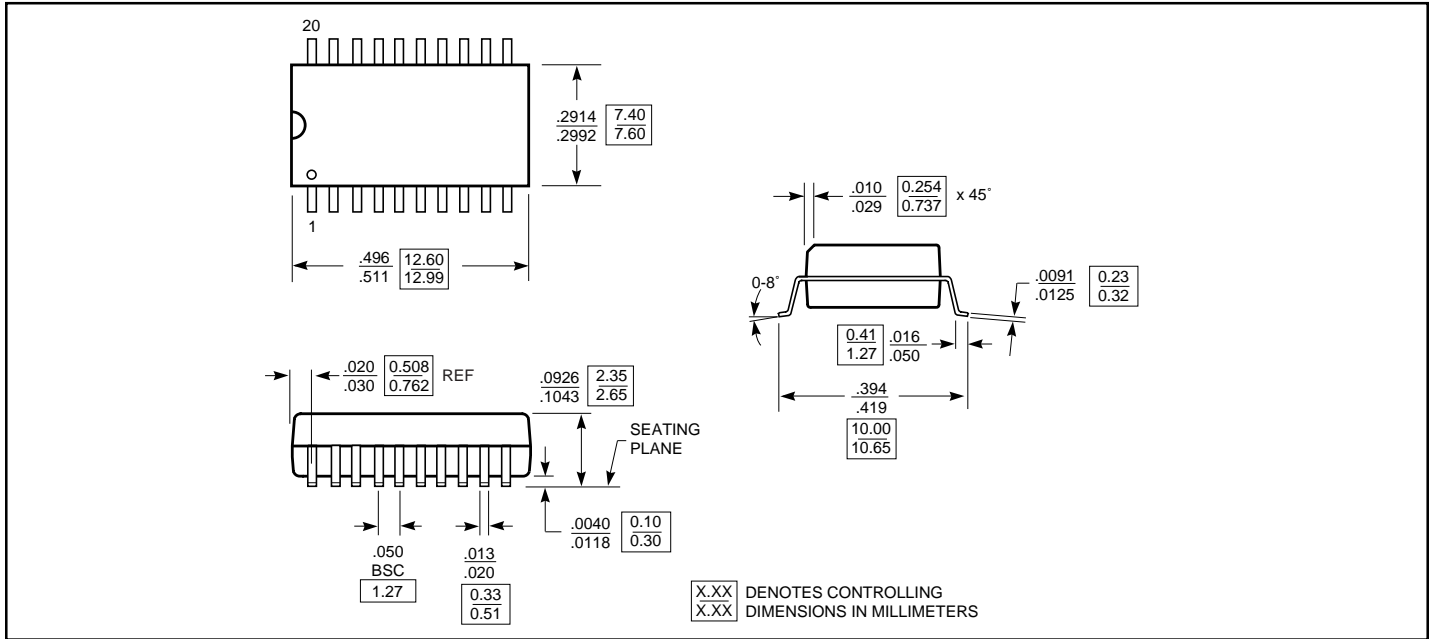
**Packaging Mechanical: 20-pin SSOP (H)**



**Packaging Mechanical: 20-pin TSSOP (L)**



**Packaging Mechanical: 20-pin SOIC (S)**



**Ordering Information**

Ordering Data	Description
PI74LVTC245H	20-pin, 209-mil wide plastic SSOP
PI74LVTC245L	20-pin, 173-mil wide plastic TSSOP
PI74LVTC245S	20-pin, 300-mil wide plastic SOIC

**Notes:**

- Thermal characteristics can be found on the company web site at <http://www.pericom.com/packaging/mechanicals.php>