T-49-19-08

PLESSEY Semiconductors

ADVANCE INFORMATION

PIC1655XT

8 BIT MICROCOMPUTER

FEATURES

- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-Bit RAM Registers
- 512 x 12-Bit Program ROM
- Arithmetic Logic Unit
- Real Time Clock Counter
- Self-contained Crystal Oscillator
- Access to RAM Registers Inherent in Instruction
- Wide Power Supply Operating Range (4.5V to 7.0V)
- Available in Two Temperature Ranges: 0° to 70°C and -40° to 85°C
- 4 Inputs, 8 Outputs, 8 Bidirectional I/O Lines
- 2 Level Stack
- Mask Programmable Prescaler for RTCC
- Mask Programmable Open Drain Option on all I/O Lines

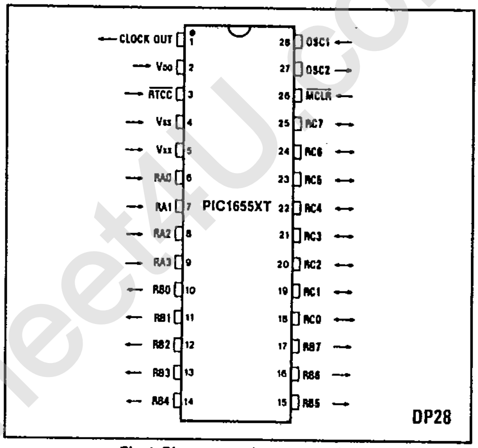

Fig.1 Pin connections - top view

The PIC1655XT microcomputer is a MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial

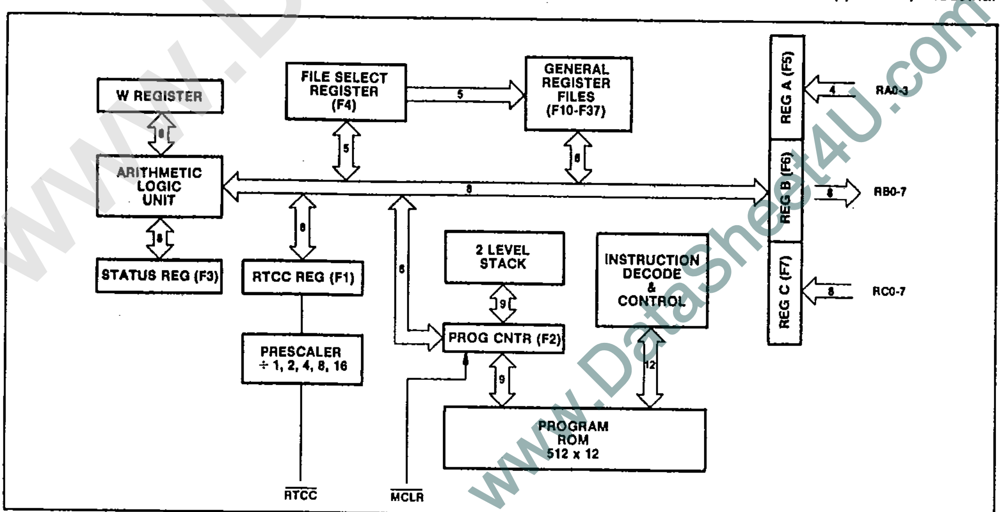

Fig.2 PIC1655XT block diagram

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timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1655XT is fabricated with N-channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for opertion, and an on-chip oscillator provides the operating clock with an external crystal, ceramic resonator or LC network to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC 1664B. The PIC 1664B is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD 1000 Field Demo System is available containing a PIC 1664B with sockets for erasable CMOS PROMs Finally, the PICES (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{\text{MCLR}}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC1 (input), OSC2 (output)	Oscillator pins. The oscillator frequency can be set by a crystal, ceramic resonator, external LC network or driven externally. The oscillator frequency is sixteen times the instruction frequency.
RTCC (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock Counter, Register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input except when a prescaler division ratio of 2,4,8 or 16 is selected in which case the input is TTL compatible.
RA0-3 (input)	4 input lines
RB0-7 (output)	8 output lines
RC0-7 (input/output)	8 user programmable input/output lines All inputs and outputs are under direct control of the program.
MCLR (input)	Master Clear. Used to initialize the internal ROM program to address 777, and latch all I/O registers high. Should be held low at least 1ms past the time when power supply is valid. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power supply. Used to enhance output current sinking capability.
V_{SS}	Ground

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction. (7) 1 · (6) 1 · (5) 1 · (4) 1 · (3) 1 · (2) Z · (1) DC · (0) C C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant. For ROTATE instructions, this bit is loaded with either the high or low order bit of the source. DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant. Z (Zero): Set if the result of an arithmetic operation is zero. Bits: 3-7 These bits are defined as logic ones.
F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3) (A4-A7 defined as zeroes).
F6	Output Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10-F37	General Purpose Registers

The PIC1655XT has the same basic architecture as the PIC1655A with the additional enhancements described below.

Real Time Clock Counter

The Real Time Clock Counter can be read from and written to under software control. In addition, it can be used to count external events via the RTCC input. A prescaler counter between the RTCC input and the Real Time Clock Counter can be mask programmed to enable the RTCC register to increment every 1,2,4,8, or 16 negative edges of the RTCC input pin.

This allows the maximum frequency of the RTCC input to be (assume an instruction cycle time of 4μs):

Prescaler Division Ratio	Maximum Input Frequency
1	0.238MHz
2	0.476MHz
4	0.952MHz
8	1.904MHz
16	3.808MHz

NOTE

The Schmitt trigger input is valid only when a division ratio of 1 is selected. Otherwise, the input is a normal TTL compatible input.

Self-Contained Oscillator

When a crystal, ceramic resonator or LC network is connected between the OSC1 and OSC2 pins, the self-contained oscillator will generate a frequency determined by the external components thus allowing an accurate timing reference, a crystal, to be used for time base control with a minimum of external parts.

The output of this oscillator is divided down by 16 to give the instruction cycle time of the microcomputer, thus with a 4MHz crystal the instruction cycle time is 4μs.

BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇆f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1 The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377₈. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.

2 When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting through a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

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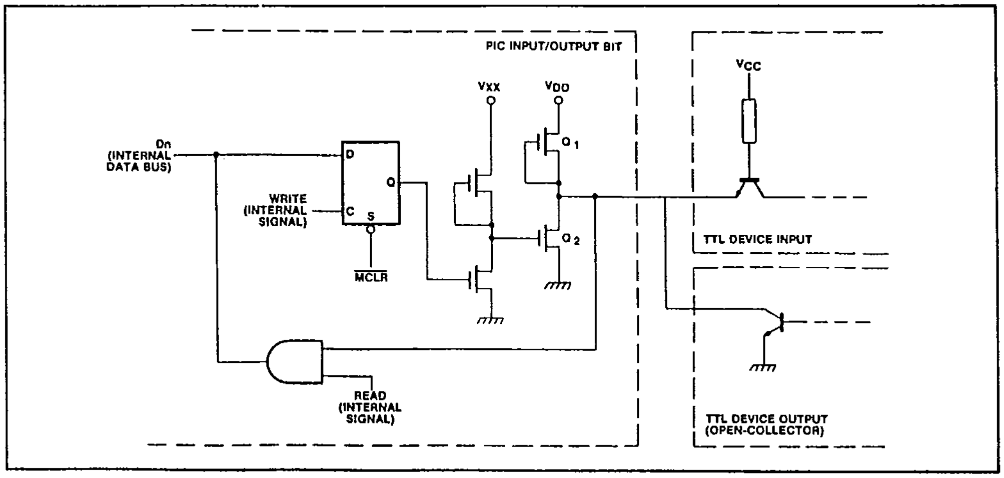


Fig.3 Typical interface - bidirectional I/O line

Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an inut instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Input Only Port: (Port RA)

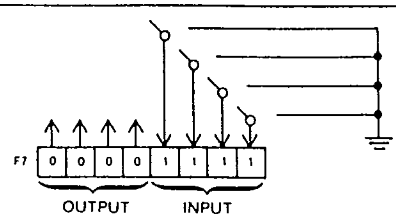
The input only port of the PIC1655XT consists of the four LSB's of F5 (port RA). An internal pull-up device is provided so that external pull-ups on open collector logic are unnecessary. The four MSB's of this port are always read as zeroes. Output operations to F5 are not defined. Note that the BTFSC and BTFSS instructions are input only operations and so can be used with F5.

Output Only Port: (Port RB)

The output only port of the PIC1655XT consists of F6 (port RB). This port contains no input circuitry and is therefore not capable of instructions requiring an input followed by an output operation. The only instructions which can validly use F6 are MOVWF and CLRF.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than t_{cy}(min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

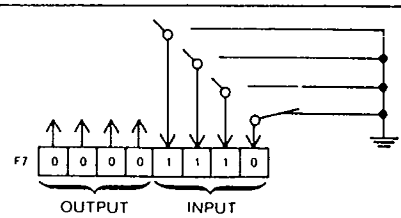


What is thought to be happening
BSF 7.5

Read into CPU	00001111
Set bit 5	00101111
Write to F7	00101111

If no inputs were low during the instruction execution, there would be no problem

Fig.4 Example 1



What could happen if an input were low
BSF 7.5

Read into CPU	00001110
Set bit 5	00101110
Write to F7	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again

Fig.5 Example 2

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias .... 125°C
Storage Temperature .... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} .... −0.3V to +12.0V
Power Dissipation 1000mW
Power Dissipated by any one I/O pin (Note 1) 60mW
Power Dissipated by all I/O pins (Note 1) 300mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	50	mA	All I/O pins high
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins high (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC when driven externally)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH2}	$V_{DD}-1$	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 4)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		—	—	0.40	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		—	—	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		—	—	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−10	—	+10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

NOTES:
1. Power dissipation for I/O pins is calculated by
   $\Sigma (V_{CC} - V_{IL}) (|I_{IL}|) + \Sigma (V_{CC} - V_{OH}) (|I_{OH}|) + \Sigma (V_{OL}) (I_{OL})$.
   The term I/O refers to all interface pins; input, ouput or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 175mA.

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Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.8MHz-4MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	t_{CY}	—	—	—	
High Pulse Width	t_{RTH}	½t_{CY}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{CY}	—	—	—	(Note 2)
I/O Ports						
Data Input Setup Time	t_S	—	—	¼t_{CY}−125	ns	
Data Input Hold Time	t_H	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF

NOTES
1. Instruction cycle period (t_{CY}) equals sixteen times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.
3. If an $\overline{RTCC}$ prescaler division ratio of 2,4,8 or 16 is selected, the maximum rise and fall times of the signal input to the $\overline{RTCC}$ pin is 200nsecs and its duty cycle must be between 40% and 60%.
4. The maximum frequency which may be input to the $\overline{RTCC}$ pin for a division ratio of 1 is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

For example:

$$\text{if } t_{CY} = 4\mu s,\ f_{(max)} = \frac{1}{4.2\mu s} = 238kHz$$

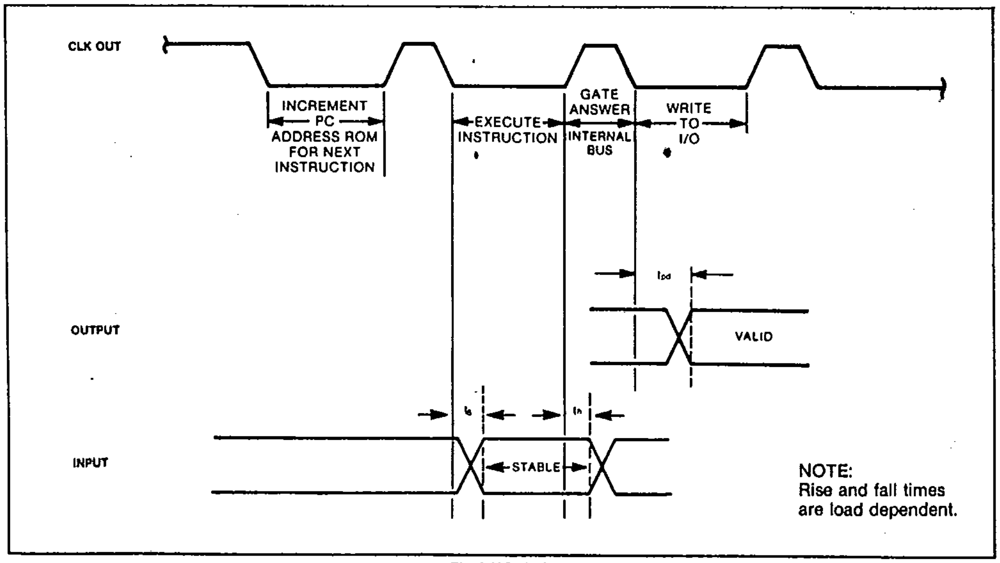


Fig.6 I/O timing

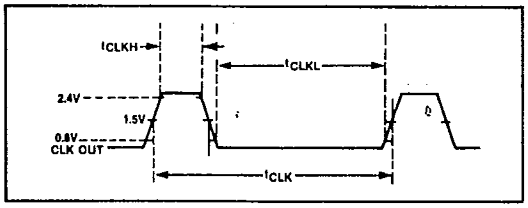


Fig.7 CLK OUT timing

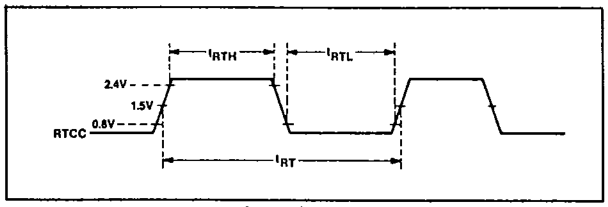


Fig.8 RTCC timing

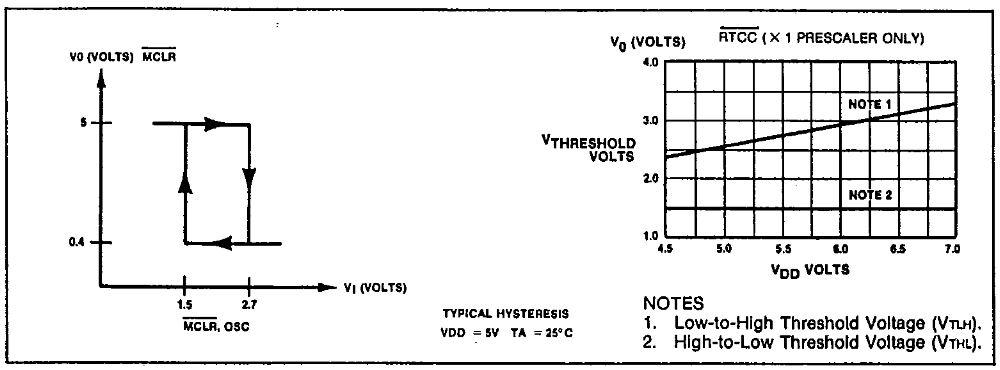


Fig.9 Schmitt trigger characteristics

PIC1655XT

PIC1655XT OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

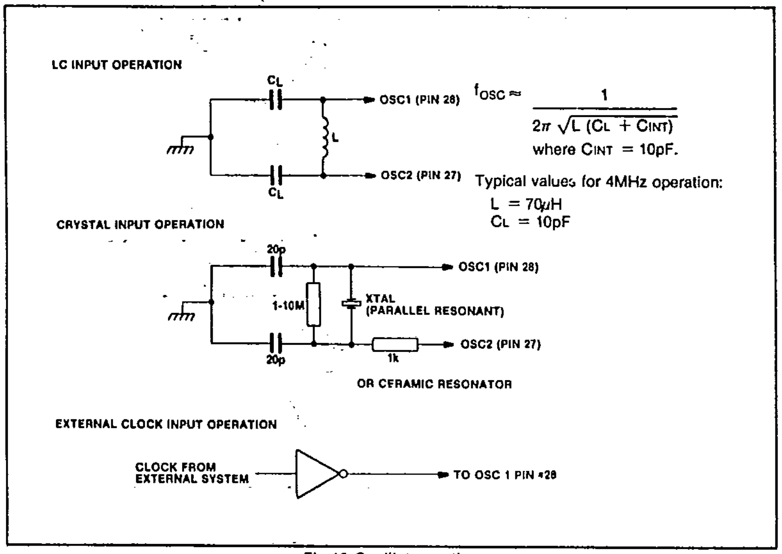


Fig.10 Oscillator options

POWER DISSIPATION DERATING GRAPH

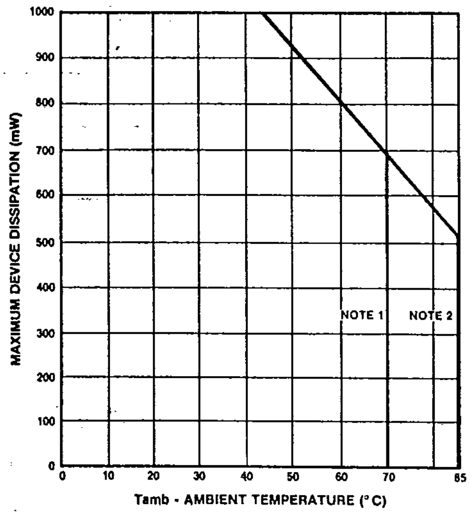
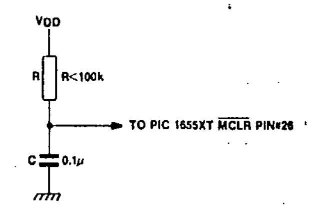


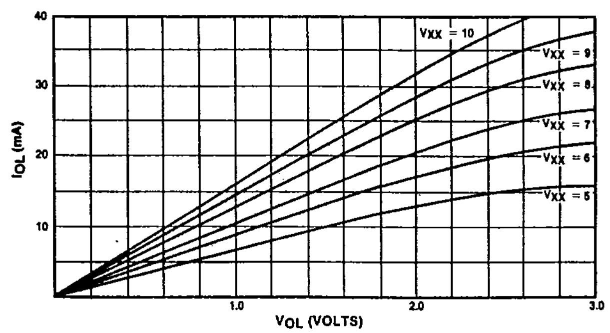
Fig.11 Power dissipation derating graph

NOTES:
1. 70° C is the maximum operating temperature for standard parts.
2. 85° C is the maximum operating temperature for "I" suffix parts.



Master Clear requires > 1.0ms delay before activation after power is applied to the VDD pin. To achieve this, an external RC configuration as shown can be used (assuming VDD is applied as a step function).

Fig.12 Master clear



The Output Sink Current is dependent on the Vxx supply and the output load. This chart shows the typical curves used to express the output drive capability.

Fig.13 Output sink current graph

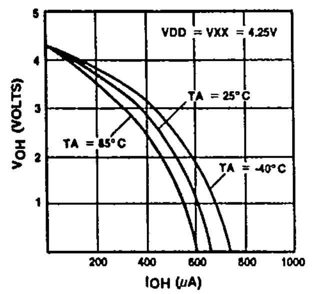


Fig.14 V_{OH} vs. I_{OH} (I/O ports)

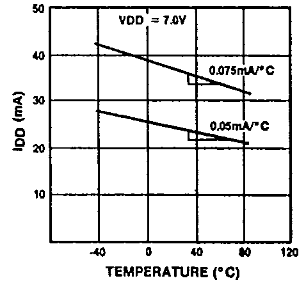


Fig.15 Power supply current vs. temperature

T-49-19-08

PIC1655XT EMULATION CAUTIONS

When emulating a PIC1655XT using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1655XT mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a high state.
1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
3. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module pin.

E. Make sure that during an actual application the $\overline{MCLR}$ input swings from a low to high level a minimum of 10msec after the supply voltage is applied to allow for the crystal to start up.

F. The cable length and internal variations may cause some parameter values to differ between PICES II Module and a production PIC1655XT.

G. The emulator PFD board or PICES II Module offers only 'internal' oscillator operation (i.e. the crystal is on the PFD or Module Board) as the long cable might cause unreliable crystal operation.