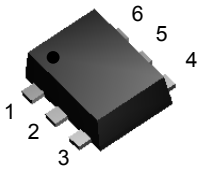
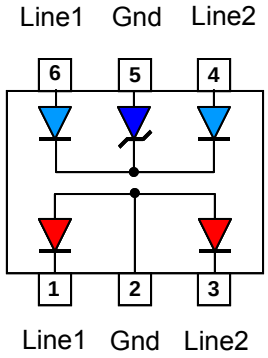
Low Capacitance TVS Diode Array

This diode array is configured to protect up to two high speed data transmission lines, used in Low Voltage Differential Signal (LVDS) ports. Acting as a line terminator, minimizes overshoot and undershoot conditions due to bus impedance, as well as protect against over-voltage events as electrostatic discharges. The line-line concept minimizes the problems to customers to re-route PCB lines, simplifying the design.

SOT563 Package





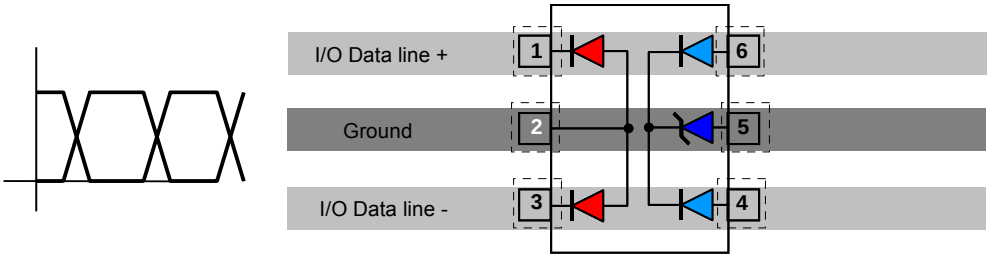
Note: pins 1and 6 (Line1), pins 3 and 4 (Line2) and pins 2 and 5 (Gnd) must be connected externally, as the drawing attached below.

SPECIFICATION FEATURES

- **Maximum Capacitance of 1.2pF at 0Vdc 1MHz Line-to-Ground**
- **Maximum Leakage Current of 1.0μA @ VRWM**
- **Industry Standard SMT Package SOT563**
- **IEC61000-4-2 Full Compliance; 15kV Air, 8kV Contact***
- **100% Tin Matte finish (LEAD-FREE PRODUCT)**

APPLICATIONS

- **USB 2.0 and Firewire Port Protection**
- **HDMI Version 1.3**
- **DVI**
- MARKING : 05



Line-line concept ease the PCB design, directly placing the device over the data lines, opening only the contact points. VREF is fixed by the operating voltage, referenced to the ground.

MAXIMUM RATINGS Tj = 25°C Unless otherwise noted

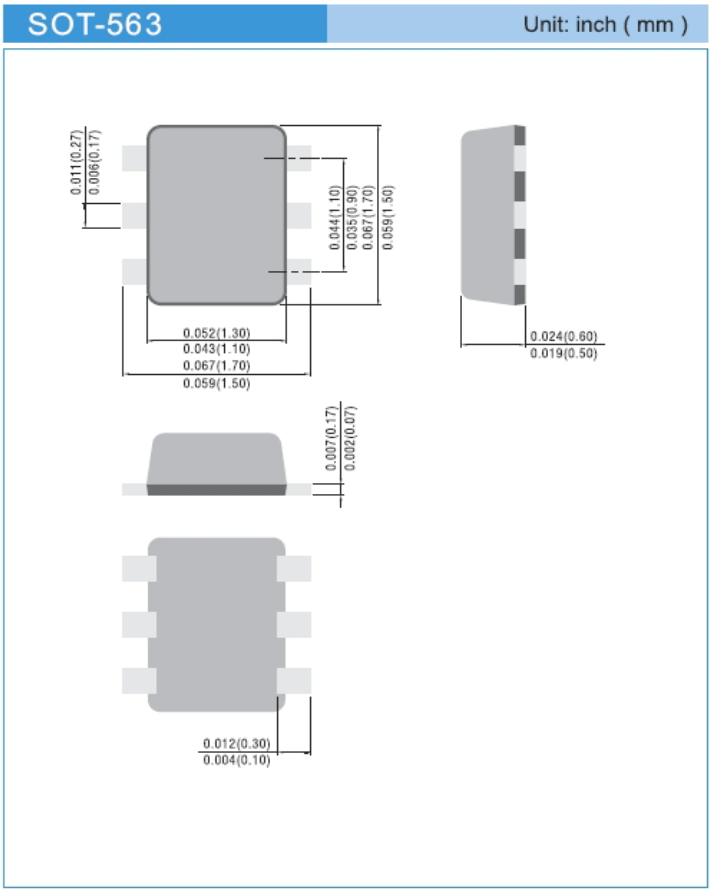
Rating	Symbol	Value	Units
Peak Pulse Power (8/20μs Waveform)	P_{PPM}	50	W
Peak Pulse Current (8/20μs Waveform)	I_{PP}	6	A
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature, t max = 10s	T_L	260	°C

ELECTRICAL CHARACTERISTICS

Tj = 25°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 1mA	6.2			V
Reverse Leakage Current	I_R	V_R = 5V			1.0	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 1 A			10	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 2 A			12	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5 A			15	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and GND			1.0	pF
		0 Vdc Bias f = 1MHz Between I/O pins			1.0	pF

PACKAGE DIMENSIONS - SOT563



APPLICATION EXAMPLE (USB2.0 port)