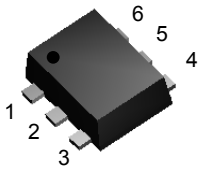
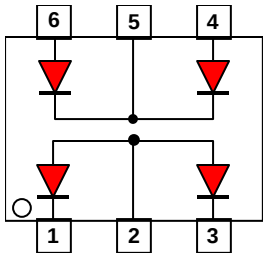
Very Low Capacitance Diode Array

This diode array is configured to protect up to two high speed data transmission lines, used in Low Voltage Differential Signal (LVDS) ports. Acting as a line terminator, minimizes overshoot and undershoot conditions due to bus impedance as well as protect against over-voltage events as electrostatic discharges. The line-line concept minimizes the problems to customers to re-route PCB lines, simplifying the design.

SOT563 Package



Line1 +VREF Line2



Line1 Gnd Line2

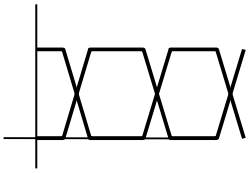
Note: pins 1and 6 (Line1) as well as pins 3 and 4 (Line2) must be connected externally, as the drawing attached below.

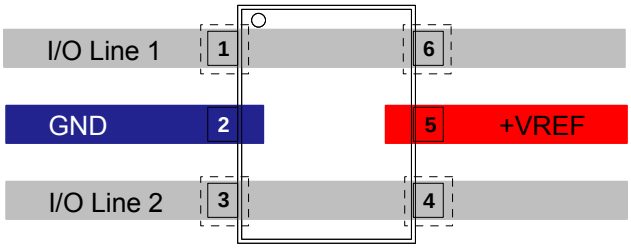
SPECIFICATION FEATURES

- **Maximum Capacitance of 1.2pF at 0Vdc 1MHz Line-to-Ground**
- **Maximum Leakage Current of 1µA @ VRWM**
- **Industry Standard SMT Package SOT563**
- **IEC61000-4-2 Full Compliance; 15kV Air, 8kV Contact***
- **100% Tin Matte finish (LEAD-FREE PRODUCT)**

APPLICATIONS

- **USB 2.0 and Firewire Port Protection**
- **HDMI Version 1.3**
- **DVI**
- MARKING : 70





Line-line concept ease the PCB design, directly placing the device over the data lines, opening only the contact points. VREF is fixed by the operating voltage, referenced to the ground.

MAXIMUM RATINGS Tj = 25°C Unless otherwise noted

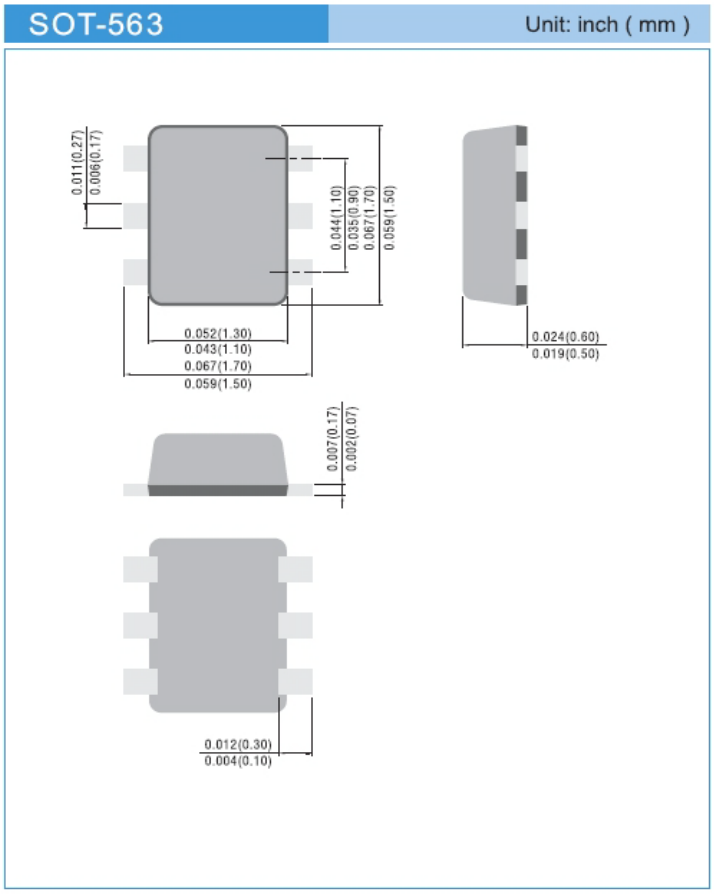
Rating	Symbol	Value	Units
Peak Pulse Current (8/20µs Waveform)	I_{PPM}	12	A
Rectifier Repetitive Peak Reverse Voltage	V_{RRM}	70	V
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature, t max = 10s	T_L	260	°C

Note: ESD Testing requires to connect a TVS between +VREF and GND, if there is no +VREF Bias connected.

ELECTRICAL CHARACTERISTICS Tj = 25°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{RWM}				70	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 50μA	85			V
Reverse Leakage Current	I_R	V_R = 70V			1	μA
Diode Surge Forward Voltage (8/20μs)	V_{FC}	I_{pp} = 1 A			2	V
Diode Surge Forward Voltage (8/20μs)	V_{FC}	I_{pp} = 5 A			7	V
Diode Surge Forward Voltage (8/20μs)	V_{FC}	I_{pp} = 12 A			13	V
Off State Capacitance	C_T	0 Vdc Bias f = 1MHz Between I/O Line and GND			1.0	pF
		0 Vdc Bias f = 1MHz Between I/O lines			1.0	pF

PACKAGE DIMENSIONS - SOT563



APPLICATION EXAMPLE (USB2.0 port)