



PJE8438

50V N-Channel Enhancement Mode MOSFET – ESD Protected

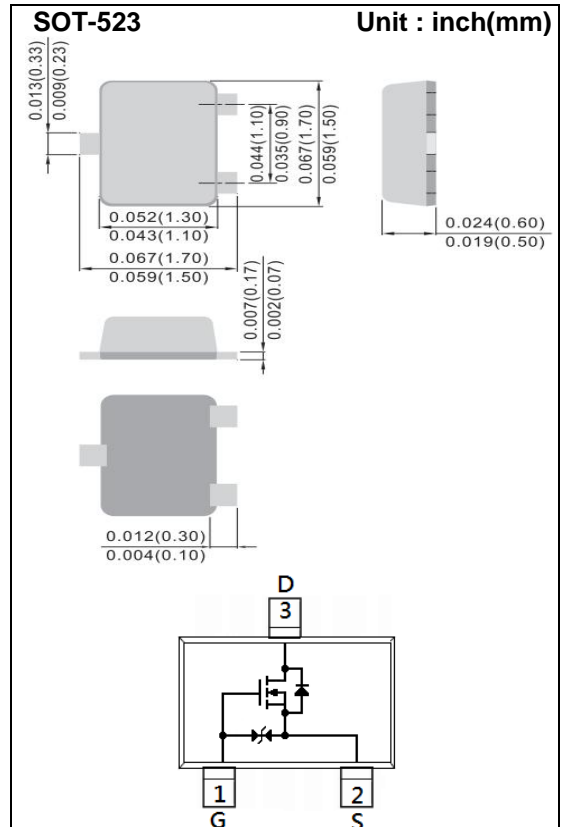
Voltage 50 V **Current** 360mA

Features

- RDS(ON) , VGS@10V, ID@500mA<1.45Ω
- RDS(ON) , VGS@4.5V, ID@200mA<1.95Ω
- RDS(ON) , VGS@2.5V, ID@100mA<4.0Ω
- RDS(ON) , VGS@1.8V, ID@10mA<4.0Ω(typ.)
- Advanced Trench Process Technology
- ESD Protected 2KV HBM
- Specially Designed for Relay driver, Speed line drive, etc.
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOT-523 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.00007 ounces, 0.002 grams
- Marking: E38



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	V _{DS}	50	V	
Gate-Source Voltage	V _{GS}	+20	V	
Continuous Drain Current	I _D	360	mA	
Pulsed Drain Current	I _{DM}	1200	mA	
Power Dissipation	P _D	T _A =25°C	300	mW
		Derate above 25°C	2.4	mW/°C
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C	
Typical Thermal resistance	R _{θJA}	417	°C/W	
- Junction to Ambient (Note 3)				



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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.86	1.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=500mA$	-	1.2	1.45	Ω
		$V_{GS}=4.5V, I_D=200mA$	-	1.3	1.95	
		$V_{GS}=2.5V, I_D=100mA$	-	1.7	4.0	
		$V_{GS}=1.8V, I_D=10mA$	-	4.0	-	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=50V, V_{GS}=0V$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 10	μA
Dynamic (Note 4)						
Total Gate Charge	Q_g	$V_{DS}=25V, I_D=500mA,$ $V_{GS}=4.5V$	-	0.95	-	nC
Gate-Source Charge	Q_{gs}		-	0.34	-	
Gate-Drain Charge	Q_{gd}		-	0.32	-	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$	-	36	-	pF
Output Capacitance	C_{oss}		-	11	-	
Reverse Transfer Capacitance	C_{rss}		-	6.6	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=25V, I_D=500mA,$ $V_{GS}=10V,$ $R_G=6\Omega$ (Note 1,2)	-	2.3	-	ns
Turn-On Rise Time	t_r		-	20	-	
Turn-Off Delay Time	$t_{d(off)}$		-	7	-	
Turn-Off Fall Time	t_f		-	20	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	500	mA
Diode Forward Voltage	V_{SD}	$I_S=500mA, V_{GS}=0V$	-	0.9	1.5	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. mounted on a 1 inch square pad of copper
4. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

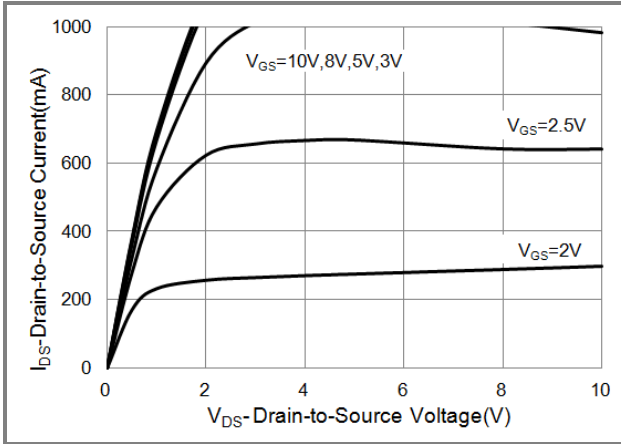


Fig.1 On-Region Characteristics

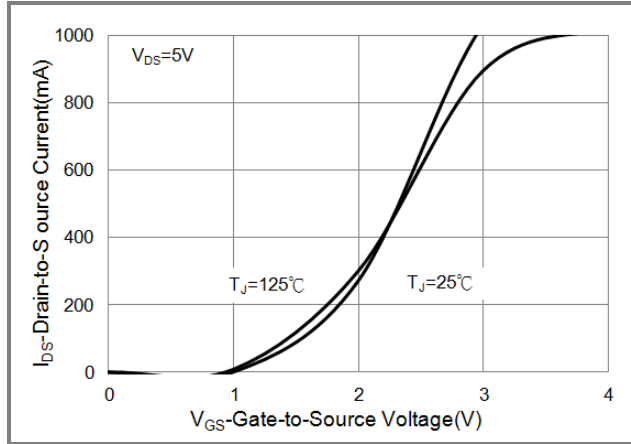


Fig.2 Transfer Characteristics

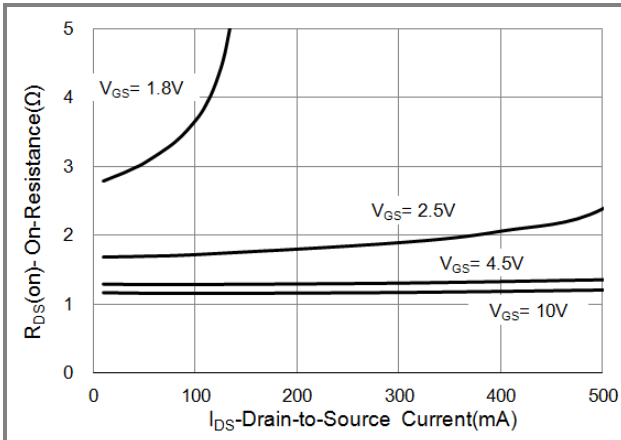


Fig.3 On-Resistance vs. Drain Current

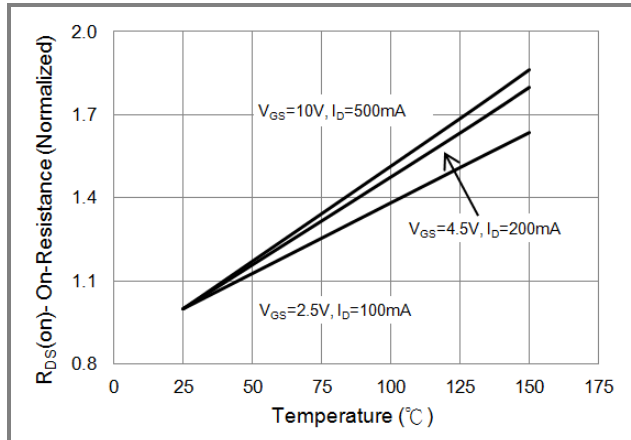


Fig.4 On-Resistance vs. Junction temperature

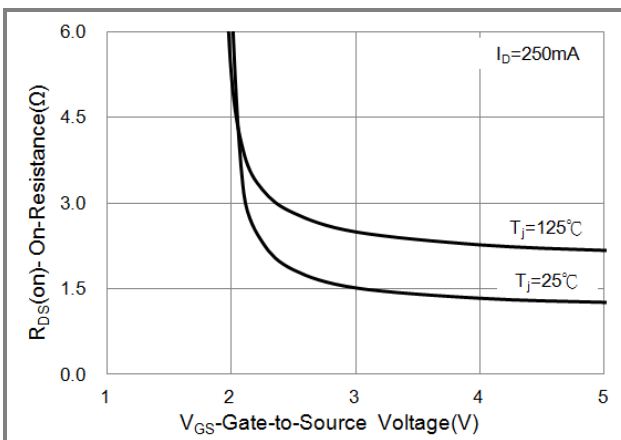


Fig.5 On-Resistance Variation with VGS.

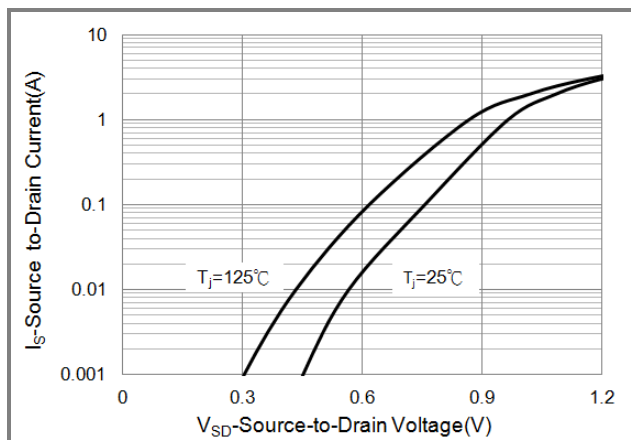


Fig.6 Body Diode Characteristics



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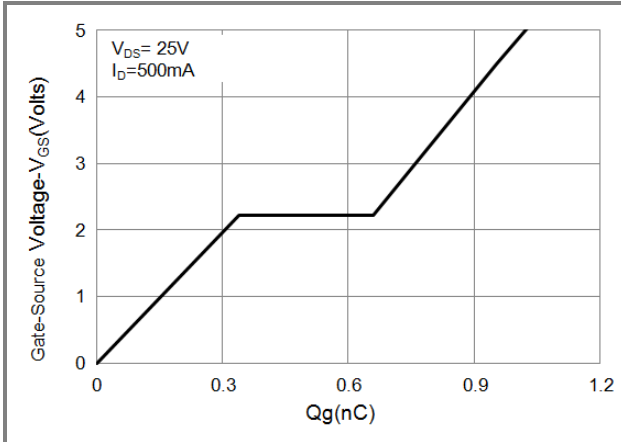


Fig.7 Gate-Charge Characteristics

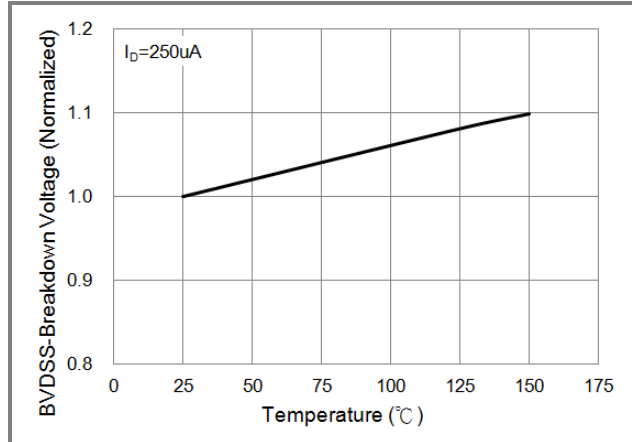


Fig.8 Breakdown Voltage Variation vs. Temperature

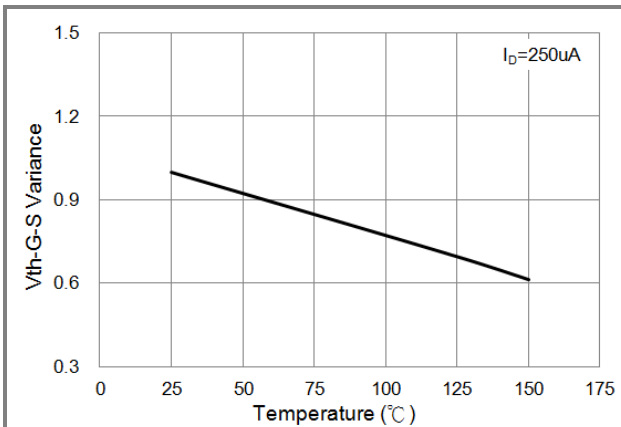


Fig.9 Threshold Voltage Variation with Temperature.

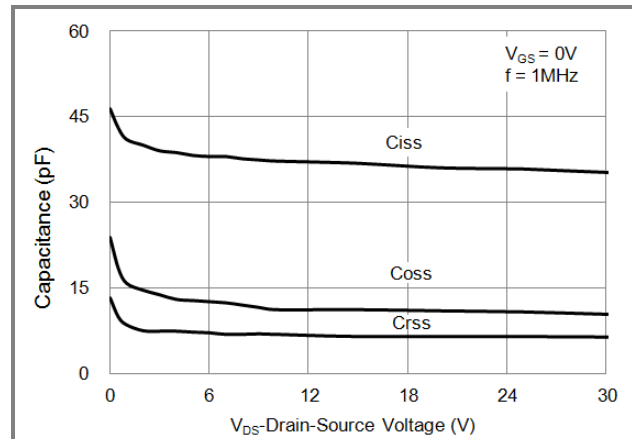


Fig.10 Capacitance vs. Drain-Source Voltage.

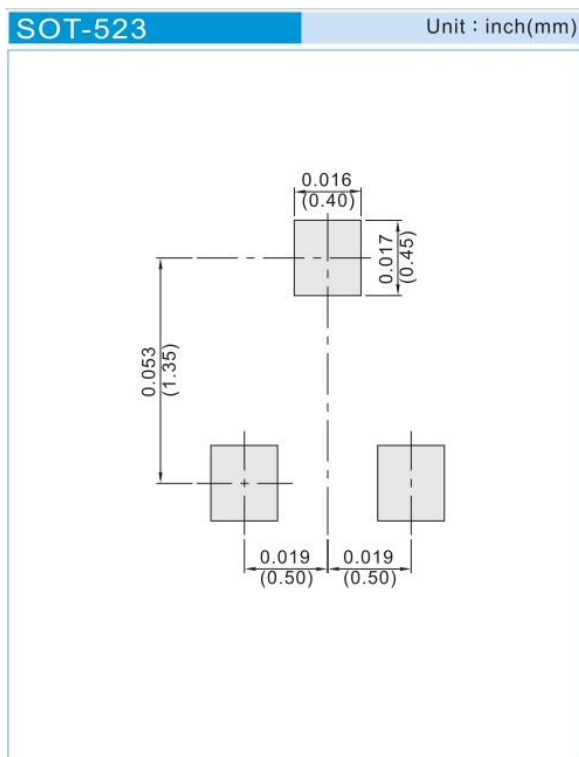


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PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJE8438_R1_00001	SOT-523	4K pcs / 7" reel	E38	Halogen free

MOUNTING PAD LAYOUT





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