



# PJF10N65M

## 650V N-Channel Enhancement Mode MOSFET

<b>Voltage</b>	<b>650V</b>	<b>Current</b>	<b>10 A</b>
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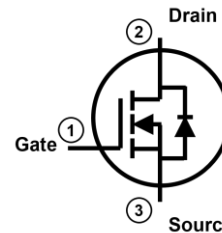
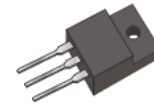
### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@5A < 0.85\Omega$
- High switching speed
- Improved  $dv/dt$  capability
- Low Gate Charge
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case: ITO-220AB-F Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- ITO-220AB-F Approx. Weight : 0.068 ounces, 2 grams

ITO-220AB-F



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		$V_{DS}$	650	V
Gate-Source Voltage		$V_{GS}$	$\pm 30$	
Continuous Drain Current (Note 3,4)	$T_C=25^\circ\text{C}$	$I_D$	10	A
Pulsed Drain Current (Note 1,3)	$T_C=25^\circ\text{C}$	$I_{DM}$	40	
Single Pulse Avalanche Energy (Note 6)		$E_{AS}$	22	mJ
Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	39	W
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
Typical Thermal Resistance (Note 5)	Junction to Case	$R_{\theta JC}$	3.2	$^\circ\text{C/W}$
	Junction to Ambient	$R_{\theta JA}$	120	



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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	650	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	3	4	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =5A	-	0.66	0.85	Ω
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V	-	-	1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>Dynamic (Note 7)</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =520V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V (Note 2,3)	-	37	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	8	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	11	-	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=1.0MHZ	-	1790	-	pF
Output Capacitance	C <sub>oss</sub>		-	100	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	31	-	
Gate resistance	R <sub>g</sub>	f=1.0MHZ	-	1.1	-	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =520V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω (Note 2,3)	-	23	-	ns
Turn-On Rise Time	t <sub>r</sub>		-	27	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	62	-	
Turn-Off Fall Time	t <sub>f</sub>		-	26	-	
<b>Drain-Source Diode</b>						
Diode Forward Current	I <sub>S</sub>	---	-	-	10	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =10A, V <sub>GS</sub> =0V	-	0.84	1.4	V
Reverse Recovery Time	T <sub>rr</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =5A	-	276	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>	dI <sub>S</sub> /dt=100A/us (Note 2,3)	-	2.6	-	uC

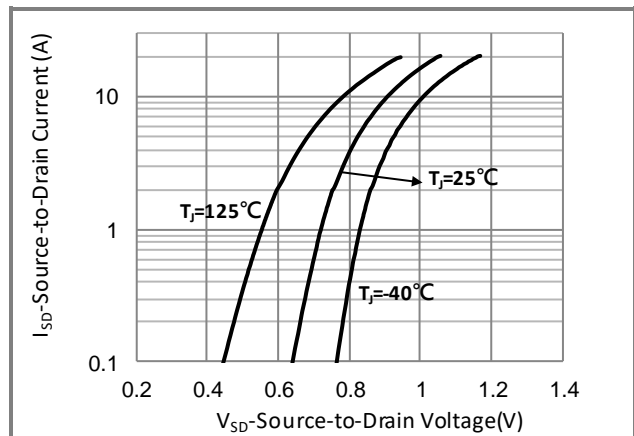
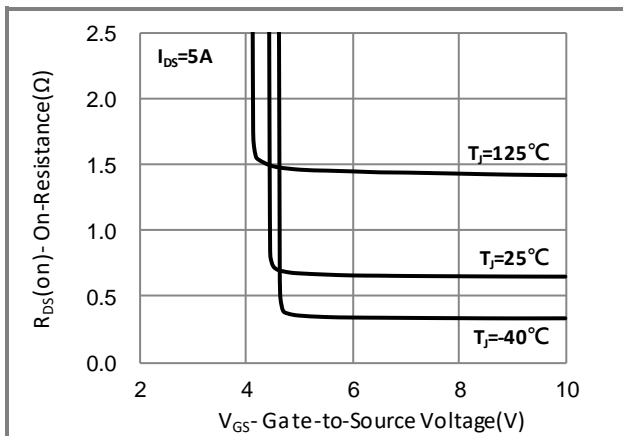
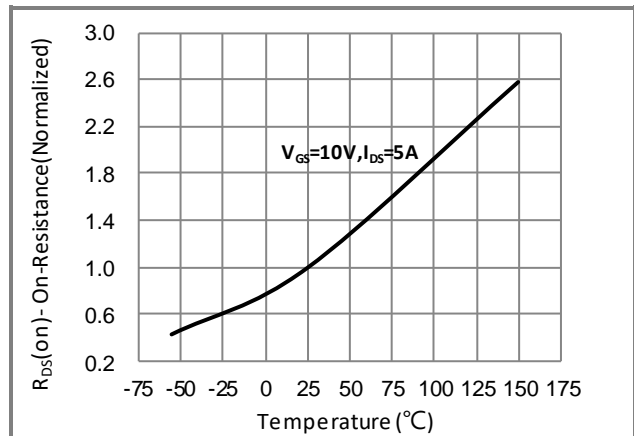
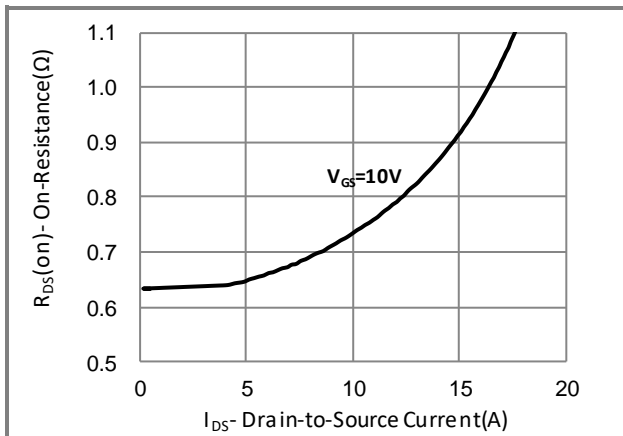
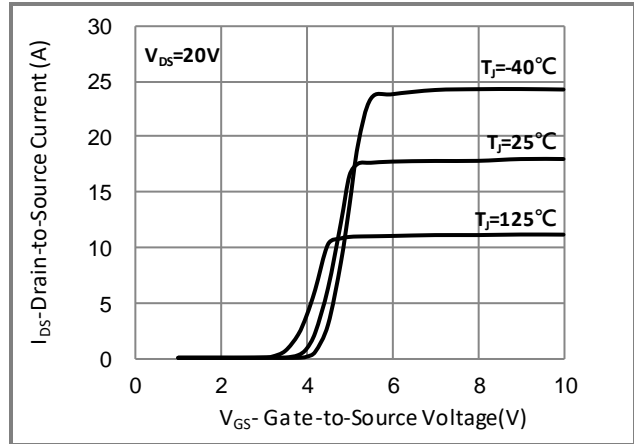
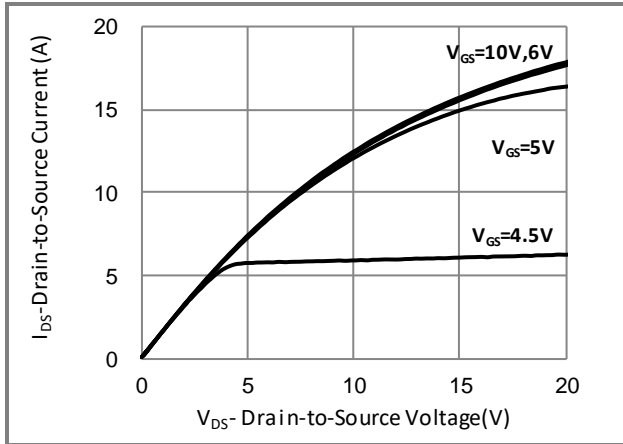
**NOTES :**

1. Pulse width ≤ 300us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.
4. The maximum current rating is package limited.
5. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz. square pad of copper.
6. The test condition is L=1mH, I<sub>AS</sub>=6.6A, R<sub>G</sub>=25 ohm, Starting T<sub>J</sub>=25°C.
7. Guaranteed by design, not subject to production testing.



# PJF10N65M

## TYPICAL CHARACTERISTIC CURVES





# PJF10N65M

## TYPICAL CHARACTERISTIC CURVES

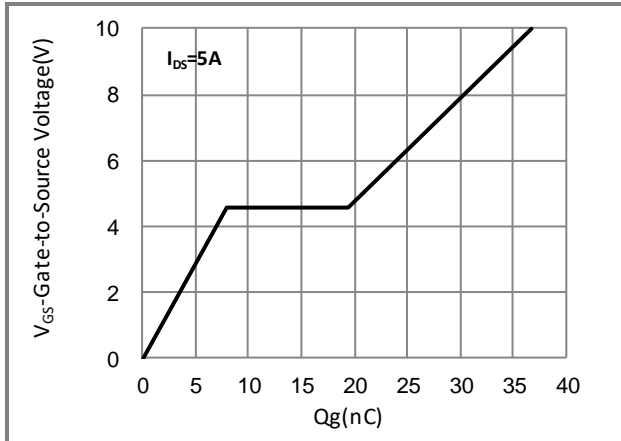


Fig.7 Gate-Charge Characteristics

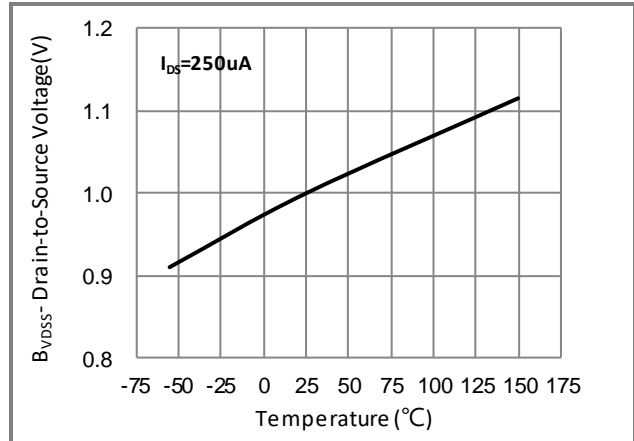


Fig.8 Breakdown Voltage Variation vs. Temperature

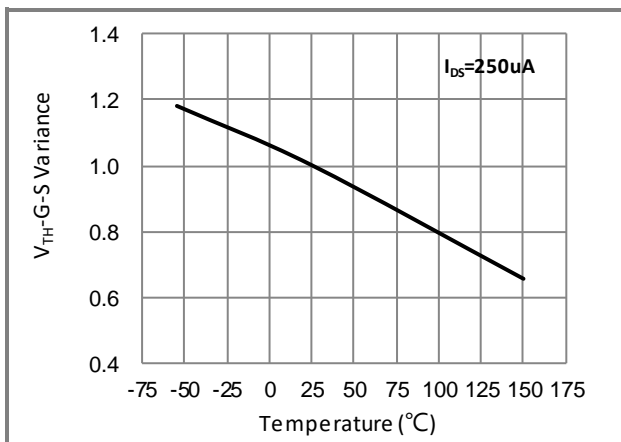


Fig.9 Threshold Voltage Variation with Temperature

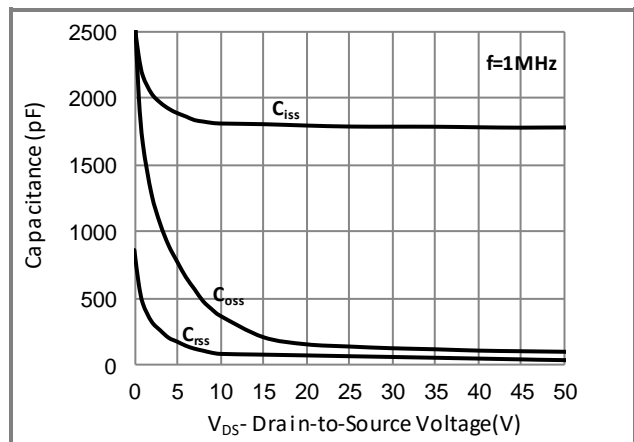


Fig.10 Capacitance vs. Drain-Source Voltage

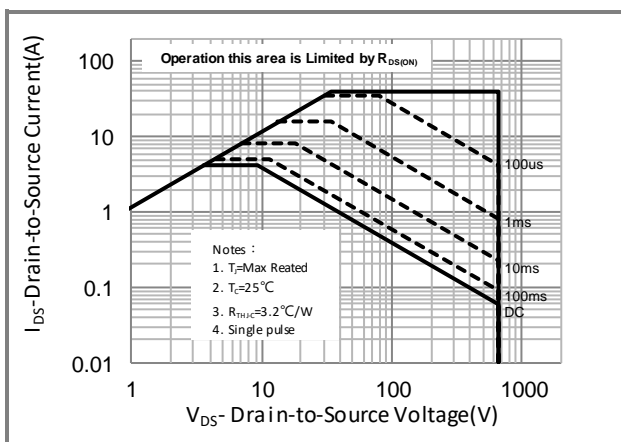


Fig.11 Maximum Safe Operating Area

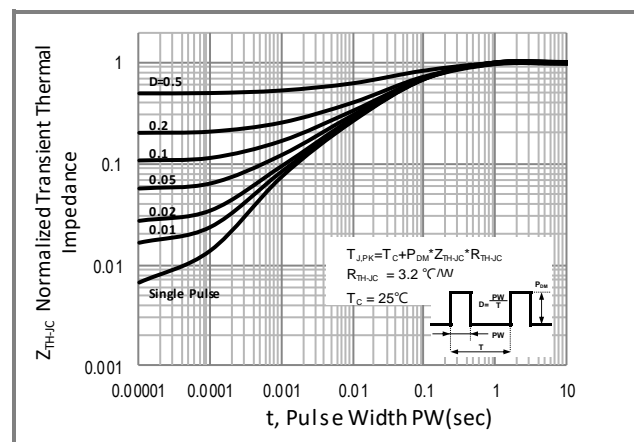


Fig.12 Normalized Transient Thermal Impedance

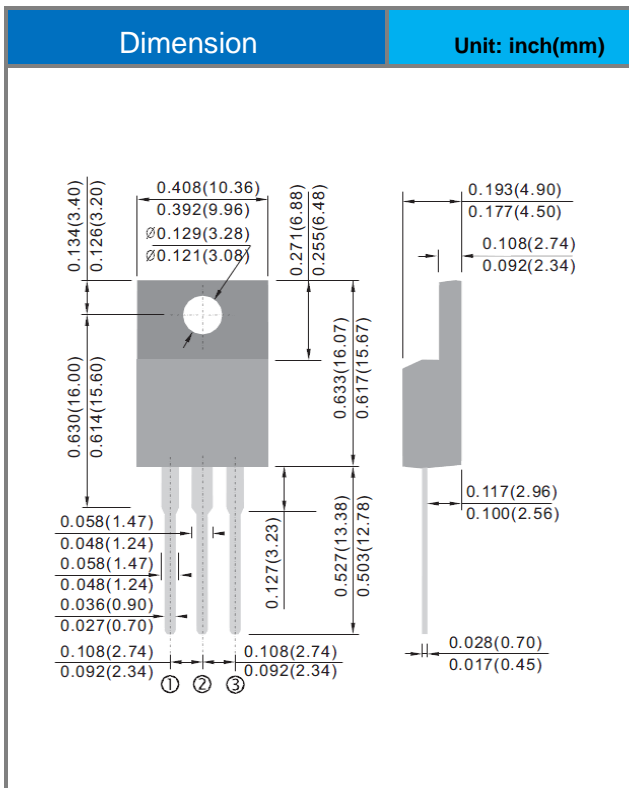


# PJF10N65M

## Part No Packing Code Version

Part No	Package Type	Packing Type	Marking	Version
PJF10N65M	ITO-220AB-F	50pcs / Tube	F10N65M	Halogen free

## Packaging Information





## **PJF10N65M**

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