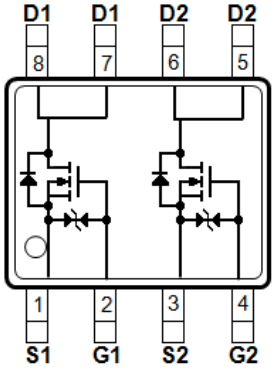
PJL9812

30V Dual N-Channel Enhancement Mode MOSFET

Voltage	30 V	Current	6 A

SOP-8



Features

- RDS(ON) , VGS@10V, ID@6A<35mΩ
- RDS(ON) , VGS@4.5V, ID@4A<40mΩ
- RDS(ON) , VGS@2.5V, ID@2A<54mΩ
- Advanced Trench Process Technology
- ESD Protected 2KV HBM
- High density cell design for ultra low on-resistance
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOP-8 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams
- Marking: L9812

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25°C	I_D	6	A
	T_A=70°C		4.8	
Pulsed Drain Current (Note 1)		I_{DM}	24	A
Power Dissipation	T_A=25°C	P_D	2	W
	T_A=70°C		1.3	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient, t≦10s (Note 5)		$R_{\theta JA}$	62.5	°C/W

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.5	0.8	1.3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=6.0A	-	30	35	mΩ
		V_{GS}=4.5V,I_D=4.0A	-	33	40	
		V_{GS}=2.5V,I_D=2.0A	-	41	54	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±10	uA
Dynamic (Note 6)						
Total Gate Charge	Q_g	V_{DS}=15V, I_D=6.0A, V_{GS}=4.5V (Note 1,2)	-	5.1	-	nC
Gate-Source Charge	Q_{gs}		-	0.8	-	
Gate-Drain Charge	Q_{gd}		-	1.4	-	
Input Capacitance	Ciss	V_{DS}=15V, V_{GS}=0V, f=200KHZ	-	421	-	pF
Output Capacitance	Coss		-	43	-	
Reverse Transfer Capacitance	Crss		-	35	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=15V, I_D=1.0A, V_{GS}=10V, R_G=3Ω (Note 1,2)	-	3.3	-	ns
Turn-On Rise Time	tr		-	24	-	
Turn-Off Delay Time	$td_{(off)}$		-	19	-	
Turn-Off Fall Time	tf		-	16	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	6	A
Diode Forward Voltage	V_{SD}	I_S=6.0A, V_{GS}=0V	-	0.86	1.2	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial TJ =25°C.
5. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

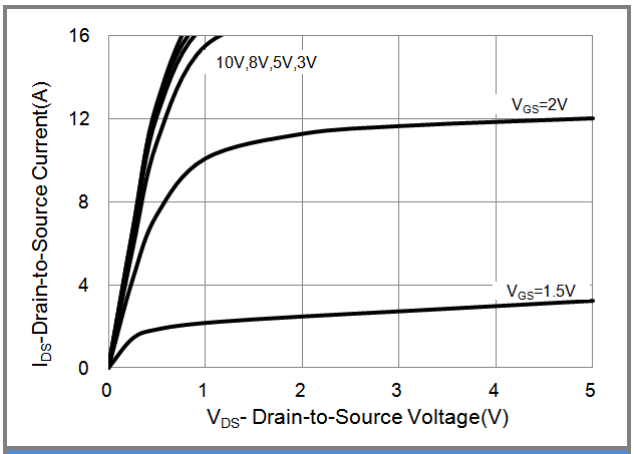

Fig.1 On-Region Characteristics

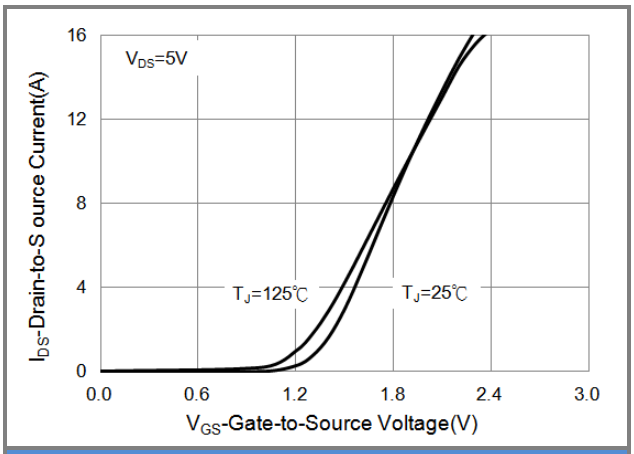

Fig.2 Transfer Characteristics

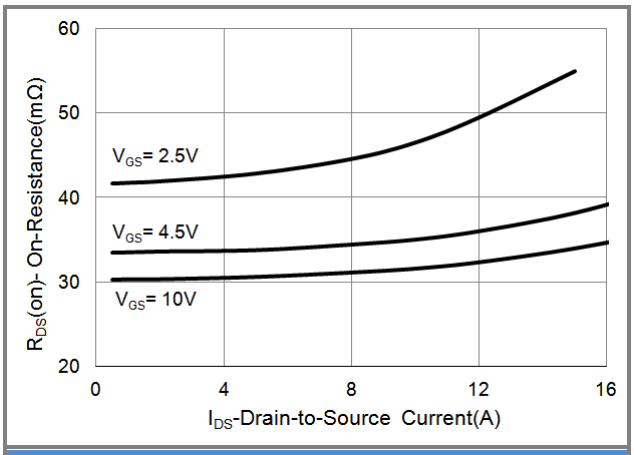

Fig.3 On-Resistance vs. Drain Current

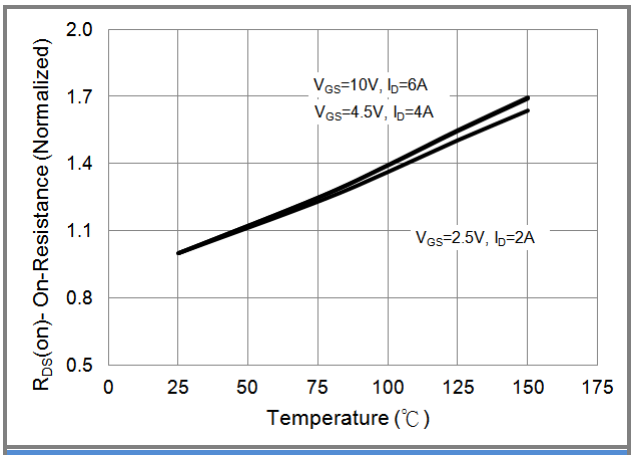

Fig.4 On-Resistance vs. Junction temperature

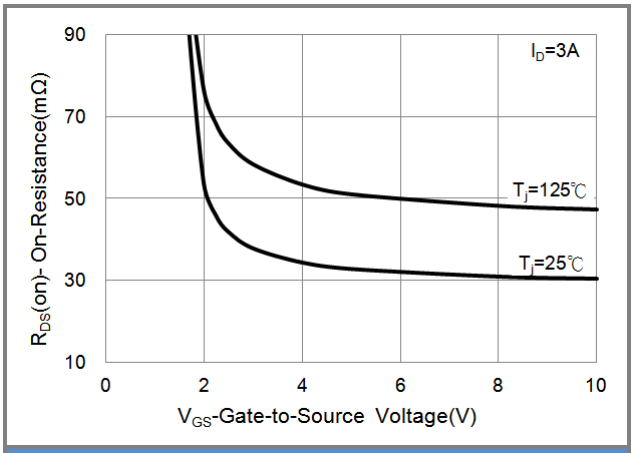

Fig.5 On-Resistance Variation with VGS.

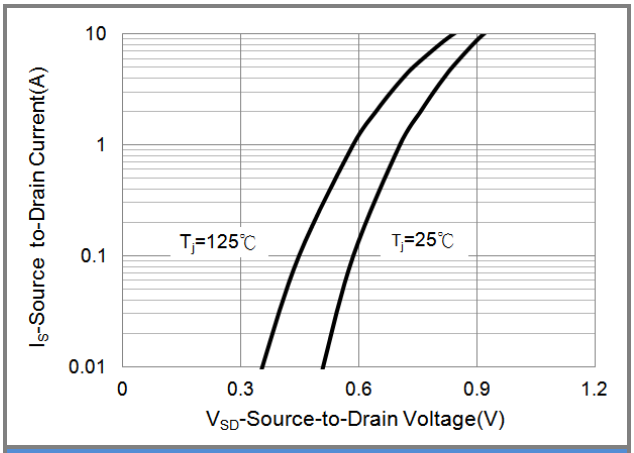

Fig.6 Body Diode Characteristics

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TYPICAL CHARACTERISTIC CURVES

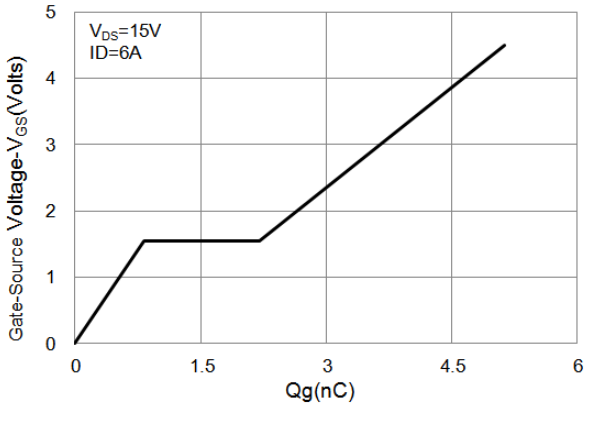


Fig.7 Gate-Charge Characteristics

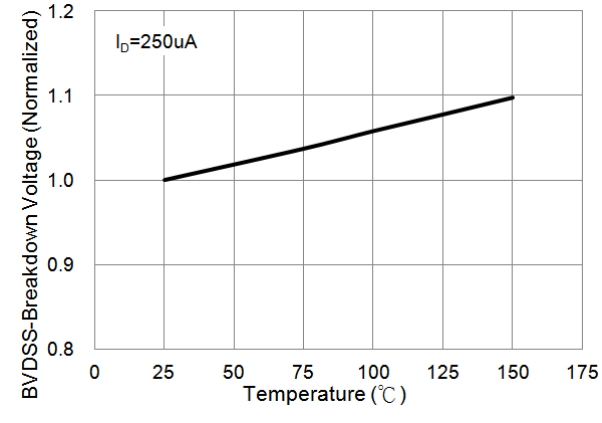


Fig.8 Breakdown Voltage Variation vs. Temperature

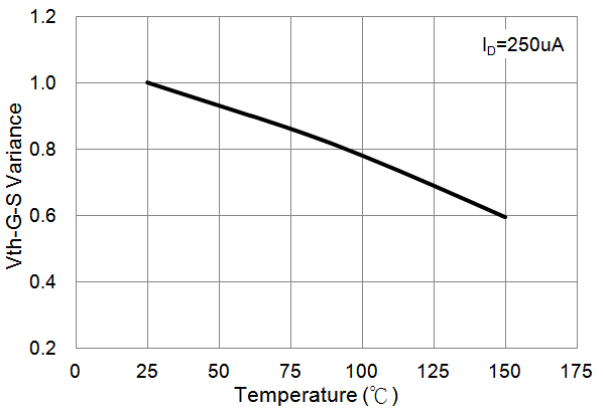


Fig.9 Threshold Voltage Variation with Temperature.

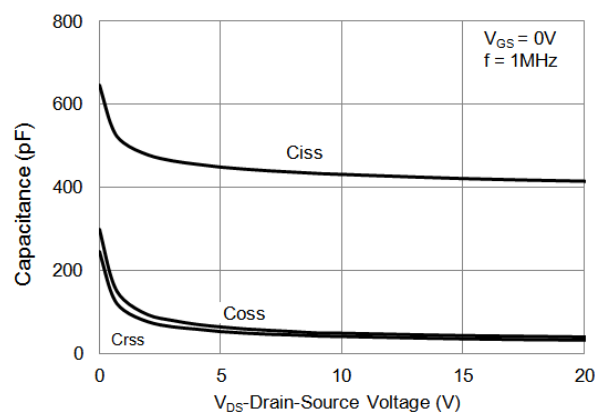


Fig.10 Capacitance vs. Drain-Source Voltage.

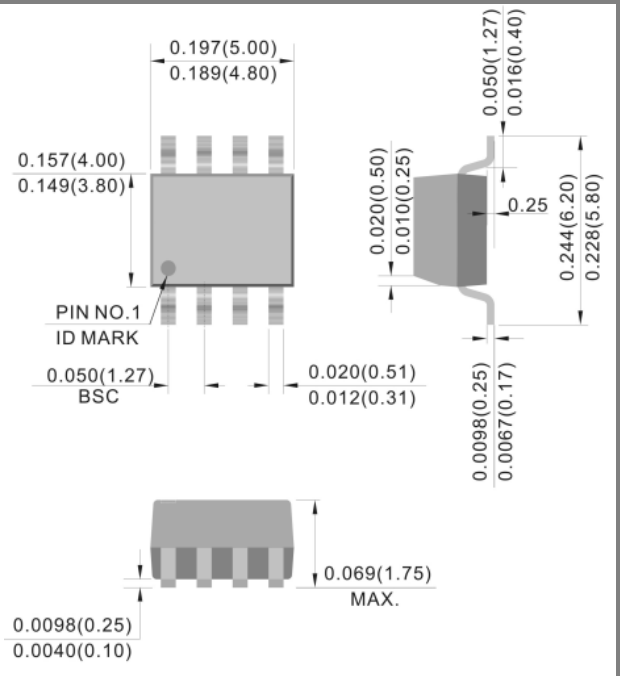
PJL9812

PART NO PACKING CODE VERSION

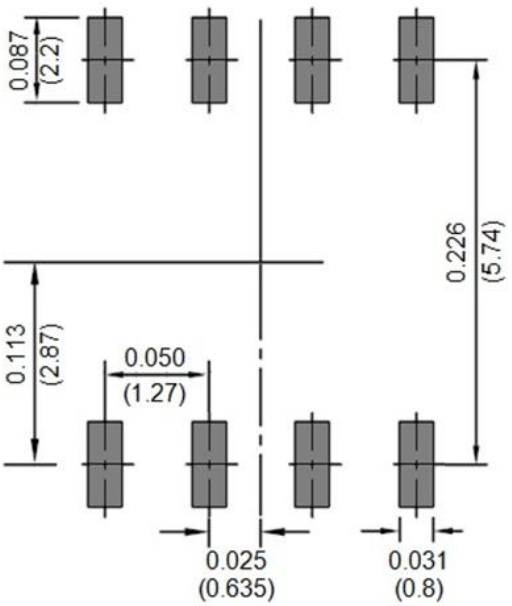
Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9812_R2_00001	SOP-8	2.5K pcs / 13” reel	L9812	Halogen free

Packaging Information & Mounting Pad Layout

SOP-8 Dimension — Unit: mm



SOP-8 PAD LATOUT — Unit: mm



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