

PJL9850

40V Dual N-Channel Enhancement Mode MOSFET

Voltage

40 V

Current

5.4 A

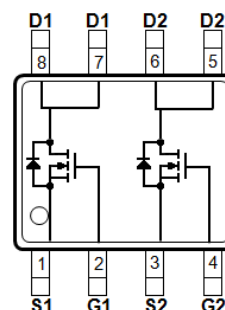
Features

- $R_{DS(ON)}, V_{GS}@10V, I_D@5A < 32m\Omega$
- $R_{DS(ON)}, V_{GS}@4.5V, I_D@3A < 44m\Omega$
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: SOP-8 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams

SOP-8



Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V _{DS}	40	V
Gate-Source Voltage		V _{GS}	±20	
Continuous Drain Current	T _A =25°C	I _D	5.4	A
	T _A =70°C		4.3	
Pulsed Drain Current ^(Note 1)		I _{DM}	20	
Power Dissipation	T _A =25°C	P _D	1.7	W
	T _A =70°C		1.1	
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~150	°C
Typical Thermal Resistance		R _{θJA}	73.5	°C/W
- Junction to Ambient ^(Note 5)				



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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.2	1.8	2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =5A	-	27.5	32	mΩ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =3A	-	35.5	44	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1.0	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q _g	V _{DS} =20V, I _D =5A, V _{GS} =4.5V (Note 3)	-	4.4	-	nC
Gate-Source Charge	Q _{gs}		-	1.3	-	
Gate-Drain Charge	Q _{gd}		-	1.7	-	
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	-	425	-	pF
Output Capacitance	C _{oss}		-	48	-	
Reverse Transfer Capacitance	C _{rss}		-	36	-	
Turn-On Delay Time	td _(on)	V _{DD} =20V, I _D =1A, V _{GS} =4.5V, R _G =25Ω (Note 3)	-	9.4	-	ns
Turn-On Rise Time	tr		-	29	-	
Turn-Off Delay Time	td _(off)		-	21	-	
Turn-Off Fall Time	tf		-	29	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S	---	-	-	5.4	A
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V	-	0.74	1	V

NOTES :

- Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
- Essentially independent of operating temperature typical characteristics.
- The maximum current rating is package limited.
- Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

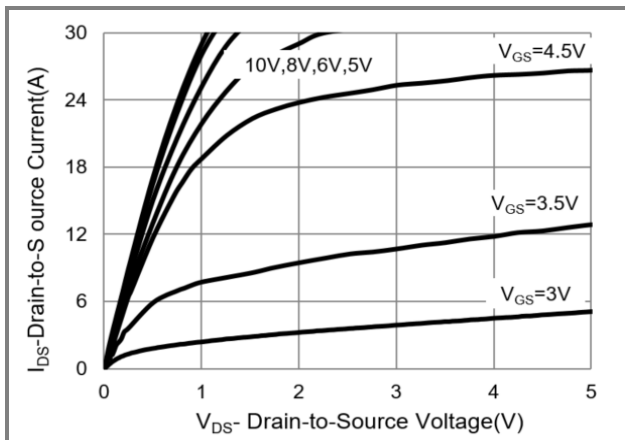


Fig.1 On-Region Characteristics

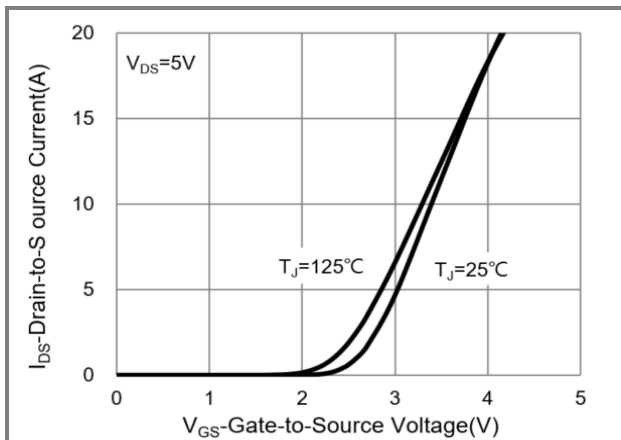


Fig.2 Transfer Characteristics

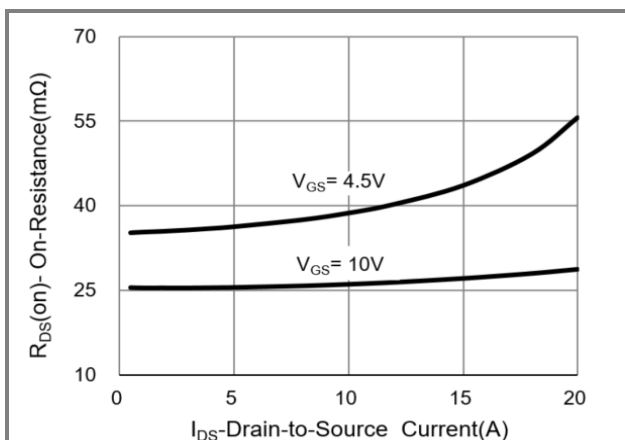


Fig.3 On-Resistance vs. Drain Current

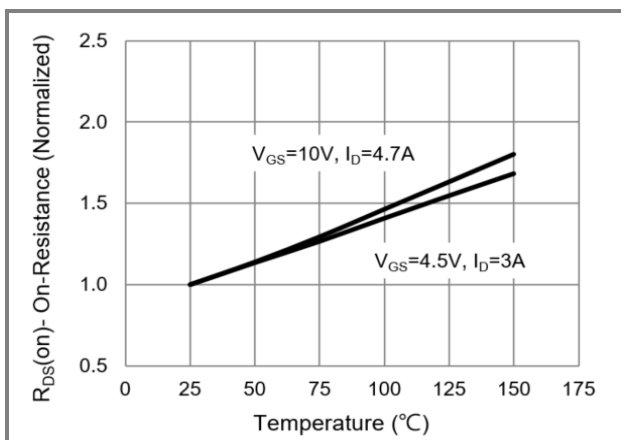


Fig.4 On-Resistance vs. Junction temperature

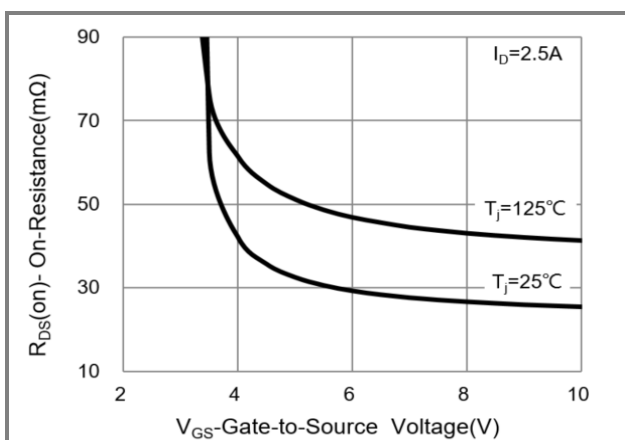


Fig.5 On-Resistance Variation with V_{GS}

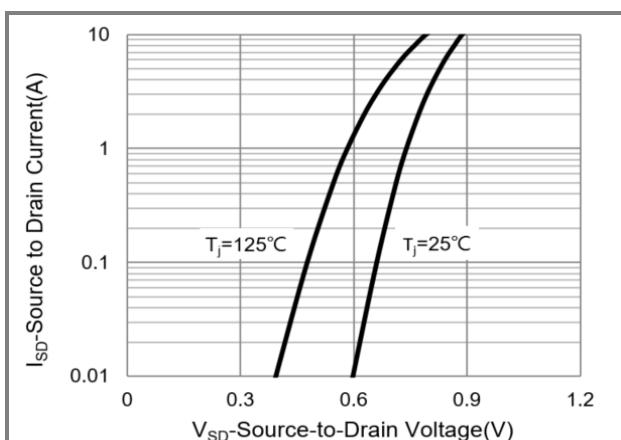


Fig.6 Body Diode Characteristics

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TYPICAL CHARACTERISTIC CURVES

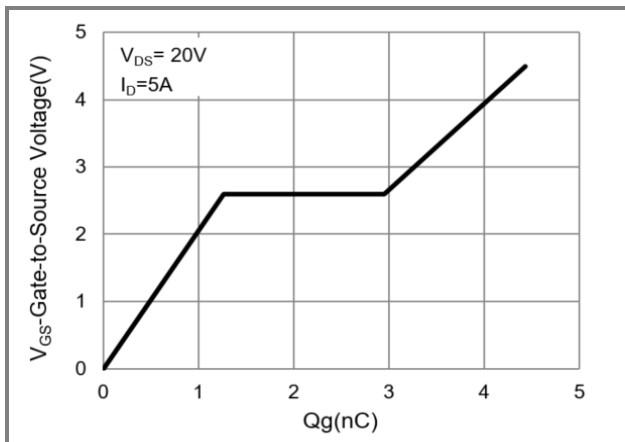


Fig.7 Gate-Charge Characteristics

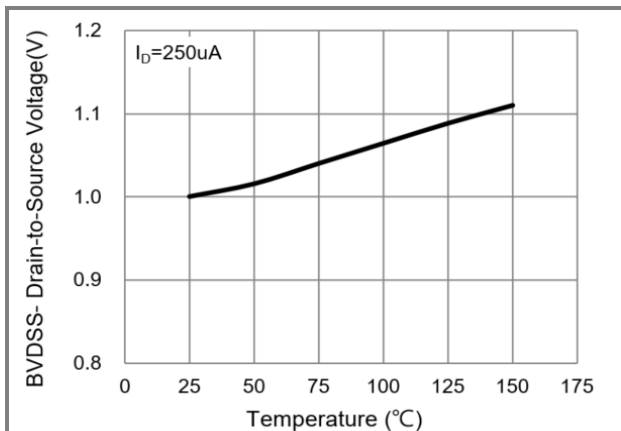


Fig.8 Breakdown Voltage Variation vs. Temperature

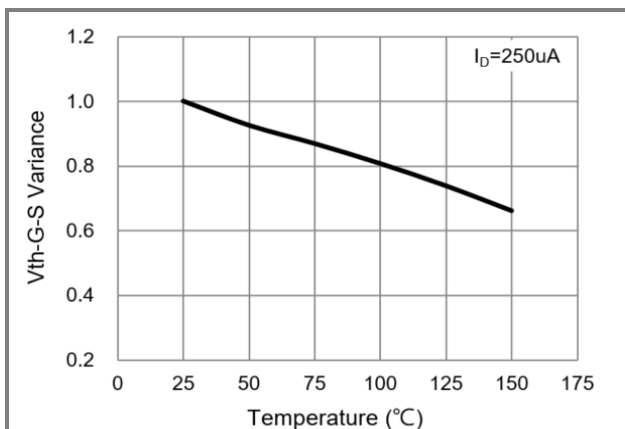


Fig.9 Threshold Voltage Variation with Temperature

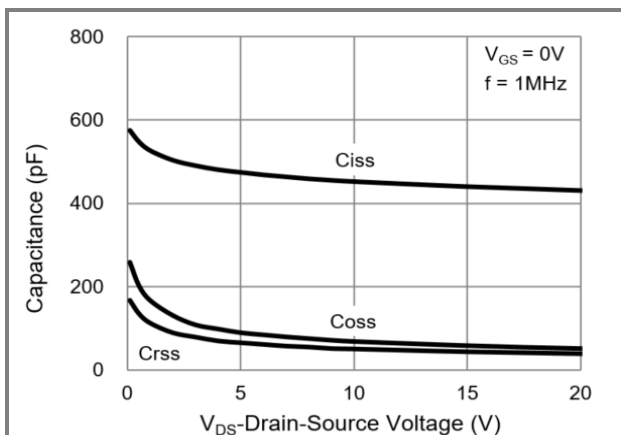


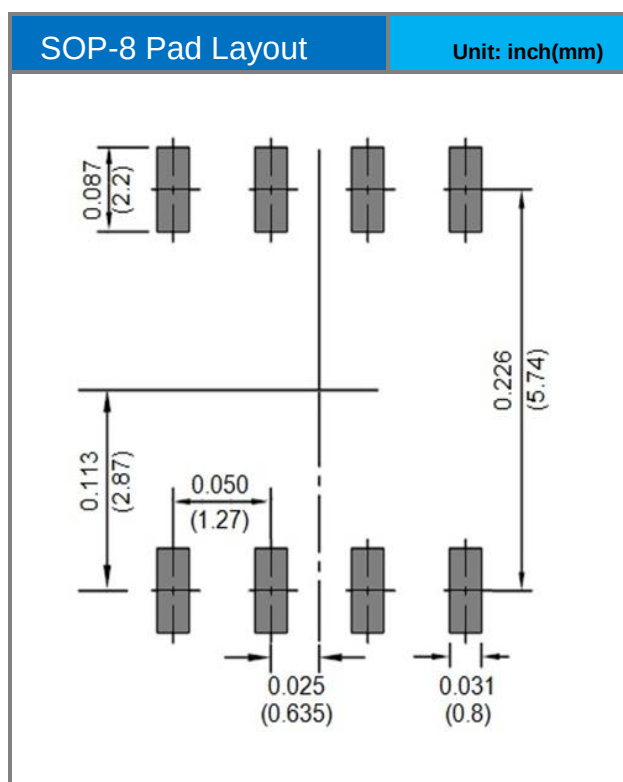
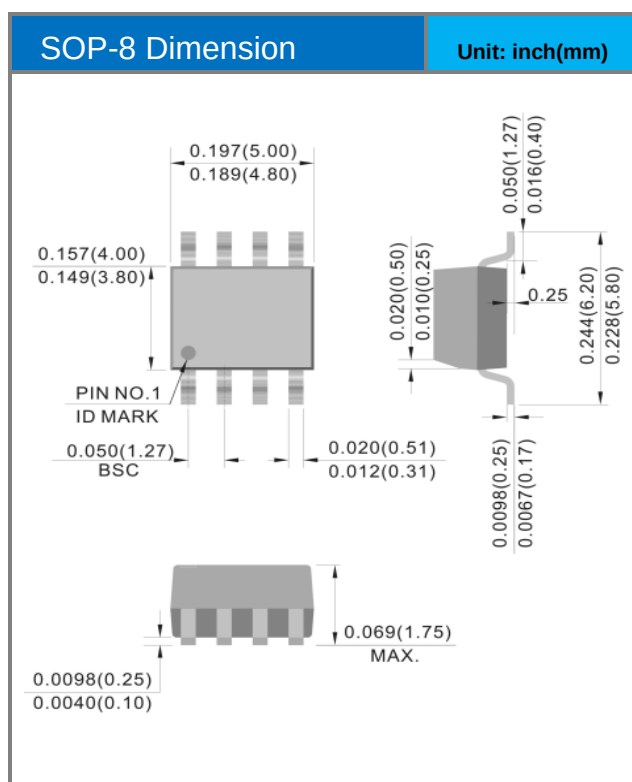
Fig.10 Capacitance vs. Drain-Source Voltage

PJL9850

Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJL9850_R2_00001	SOP-8	2.5K pcs / 13" reel	L9850	Halogen free

Packaging Information & Mounting Pad Layout





PJL9850

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