



PJS6602

20V Complementary Enhancement Mode MOSFET

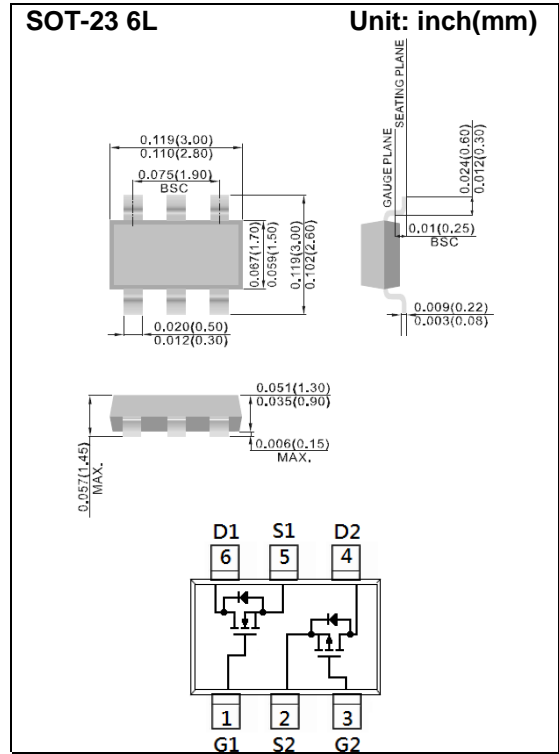
Voltage 20 / -20V **Current** 5.2 / -3.4A

Features

- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOT-23 6L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0005 ounces, 0.014 grams
- Marking: SC2



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	N-Ch LIMIT	P-Ch LIMIT	UNITS
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 12	± 12	V
Continuous Drain Current	I_D	5.2	-3.4	A
Pulsed Drain Current ^(Note 4)	I_{DM}	20.8	-13.6	A
Power Dissipation	$T_a=25^\circ\text{C}$	1.25		W
	Derate above 25°C	10		mW/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150		$^\circ\text{C}$
Typical Thermal Resistance	$R_{\theta JA}$	100		$^\circ\text{C/W}$
- Junction to Ambient ^(Note 3)				



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N-Channel Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.77	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=5.2A$	-	29	36	m Ω
		$V_{GS}=2.5V, I_D=3.2A$	-	39	52	
		$V_{GS}=1.8V, I_D=1.5A$	-	58	92	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 5)						
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=5.2A,$ $V_{GS}=4.5V$ (Note 1,2)	-	4.1	-	nC
Gate-Source Charge	Q_{gs}		-	1.1	-	
Gate-Drain Charge	Q_{gd}		-	0.7	-	
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	396	-	pF
Output Capacitance	C_{oss}		-	54	-	
Reverse Transfer Capacitance	C_{rss}		-	40	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=5.2A,$ $V_{GS}=4.5V,$ $R_G=6\Omega$ (Note 1,2)	-	14	-	ns
Turn-On Rise Time	t_r		-	10	-	
Turn-Off Delay Time	$t_{d(off)}$		-	30	-	
Turn-Off Fall Time	t_f		-	7	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	1.5	A
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$	-	0.75	1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing



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P-Channel Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.65	-1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-3.4A$	-	65	82	m Ω
		$V_{GS}=-2.5V, I_D=-2.2A$	-	82	110	
		$V_{GS}=-1.8V, I_D=-1.2A$	-	103	146	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 5)						
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-3.4A,$ $V_{GS}=-4.5V$ (Note 1,2)	-	7	-	nC
Gate-Source Charge	Q_{gs}		-	1	-	
Gate-Drain Charge	Q_{gd}		-	1.8	-	
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0\text{MHZ}$	-	522	-	pF
Output Capacitance	C_{oss}		-	55	-	
Reverse Transfer Capacitance	C_{rss}		-	40	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-3.4A,$ $V_{GS}=-4.5V,$ $R_G=6\Omega$ (Note 1,2)	-	10	-	ns
Turn-On Rise Time	t_r		-	4	-	
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	
Turn-Off Fall Time	t_f		-	5	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-1.5	A
Diode Forward Voltage	V_{SD}	$I_S=-1.0A, V_{GS}=0V$	-	0.77	-1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
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N-Channel TYPICAL CHARACTERISTIC CURVES

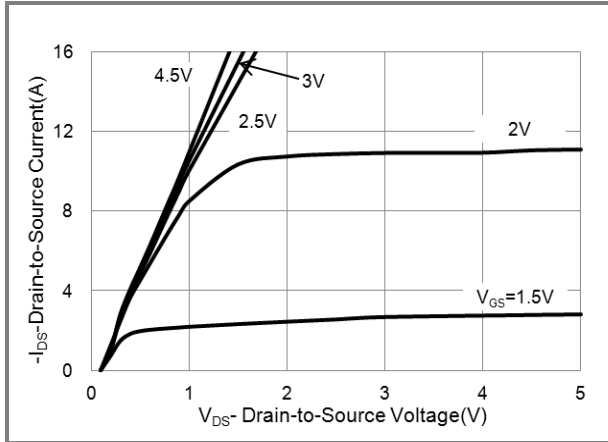


Fig.1 On-Region Characteristics

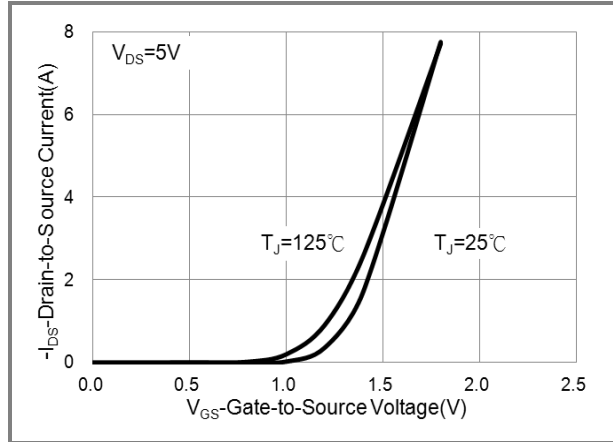


Fig.2 Transfer Characteristics

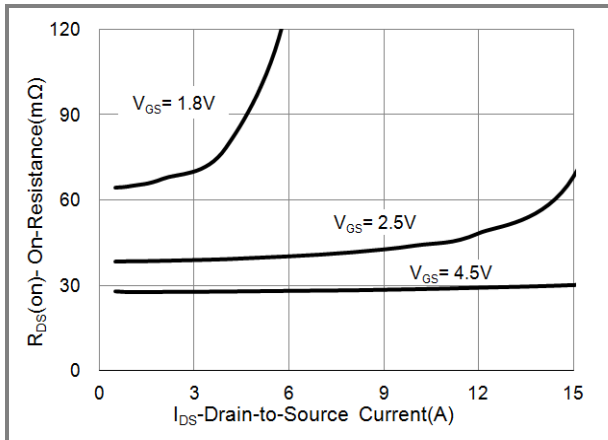


Fig.3 On-Resistance vs. Drain Current

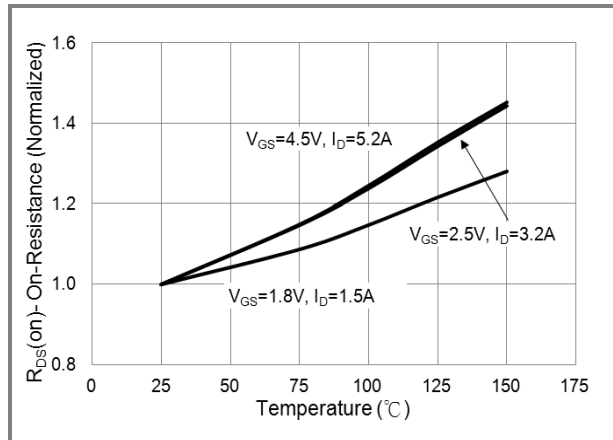


Fig.4 On-Resistance vs. Junction temperature

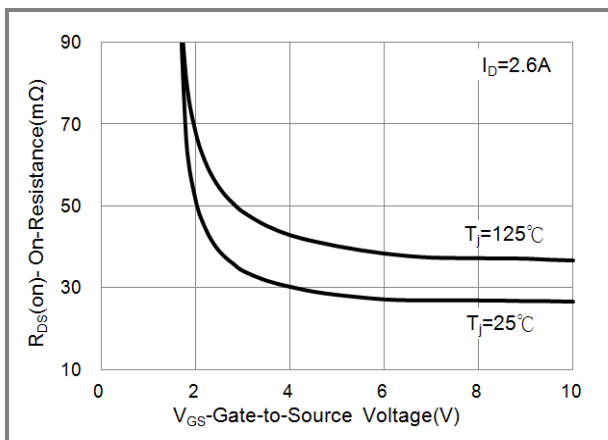


Fig.5 On-Resistance Variation with V_GS.

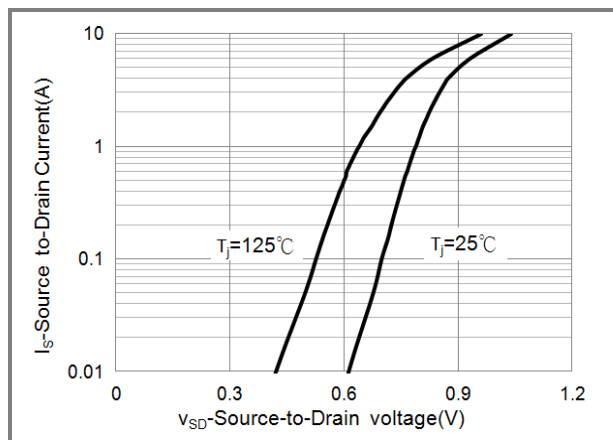


Fig.6 Body Diode Characteristic



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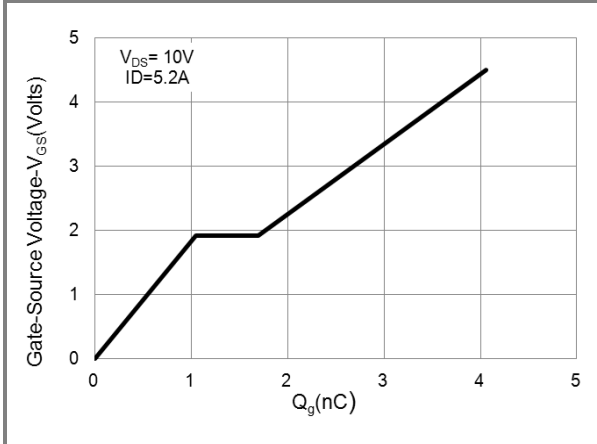


Fig.7 Gate-Charge Characteristics

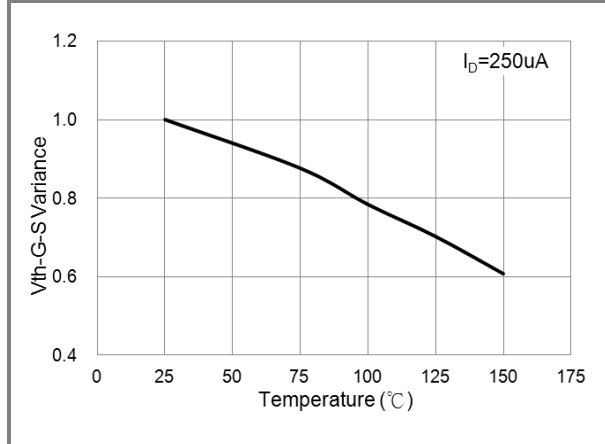


Fig.8 Threshold Voltage Variation with Temperature.

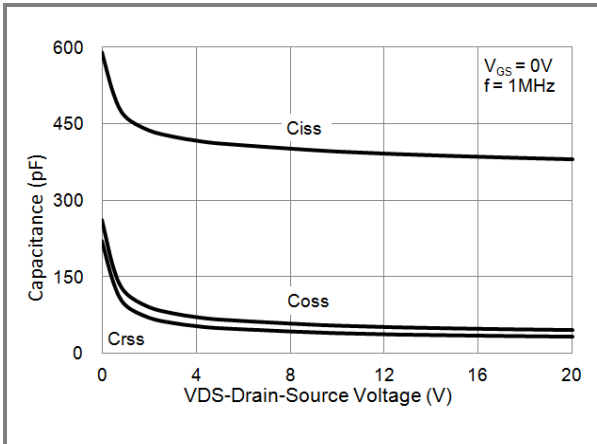


Fig.9 Capacitance vs. Drain-Source Voltage.



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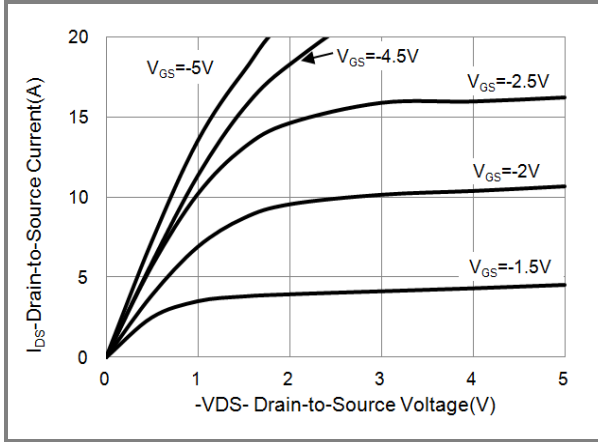


Fig.1 On-Region Characteristics

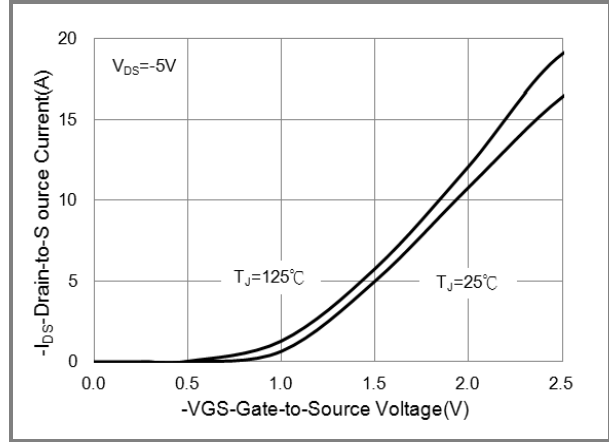


Fig.2 Transfer Characteristics

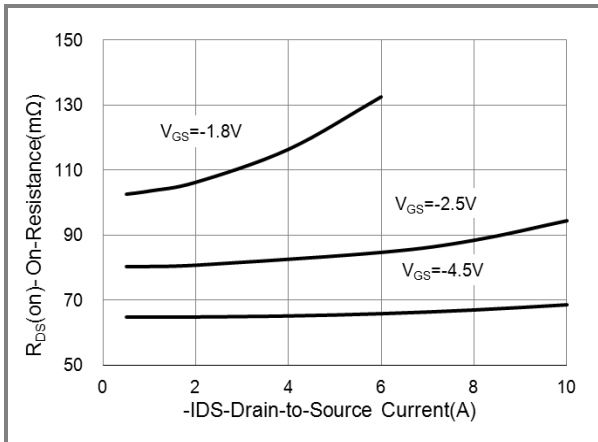


Fig.3 On-Resistance vs. Drain Current

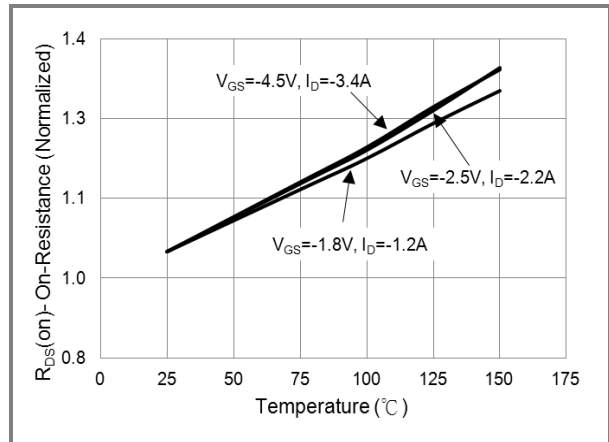


Fig.4 On-Resistance vs. Junction temperature

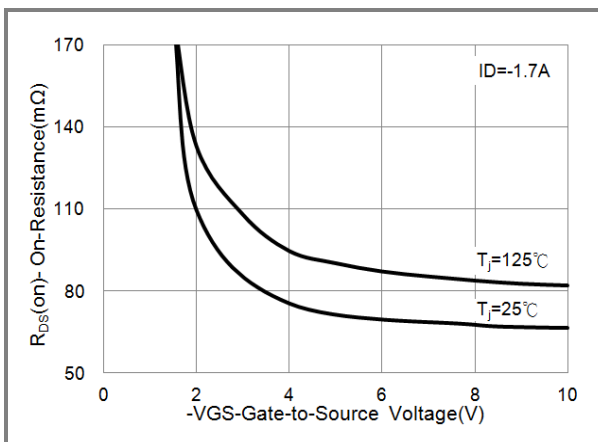


Fig.5 On-Resistance Variation with VGS.

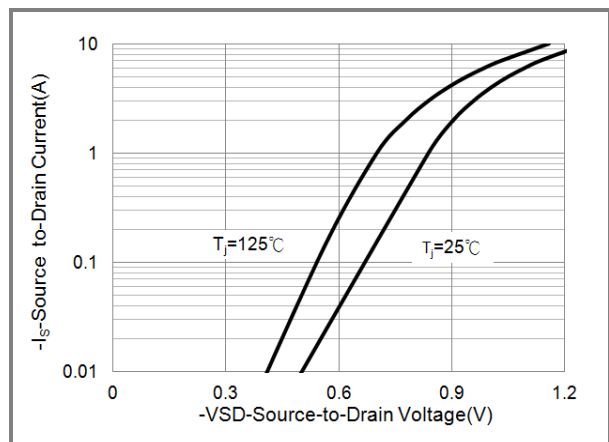


Fig.6 Body Diode Characteristics



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P-Channel TYPICAL CHARACTERISTIC CURVES

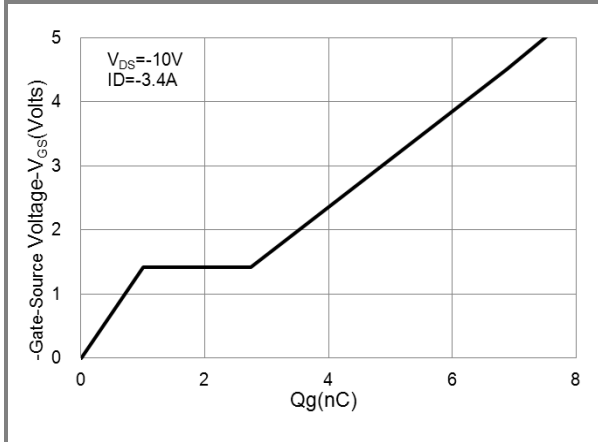


Fig.7 Gate-Charge Characteristics

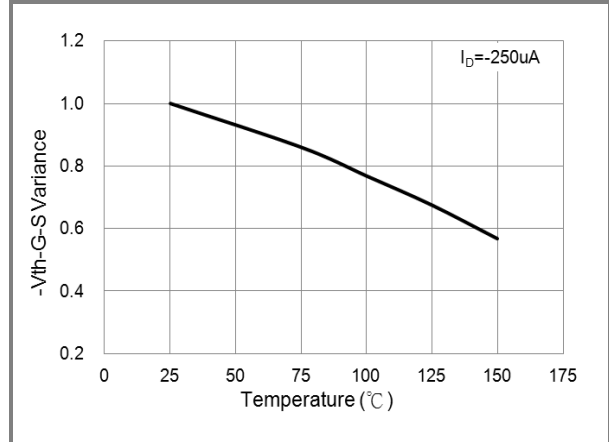


Fig.8 Threshold Voltage Variation with Temperature.

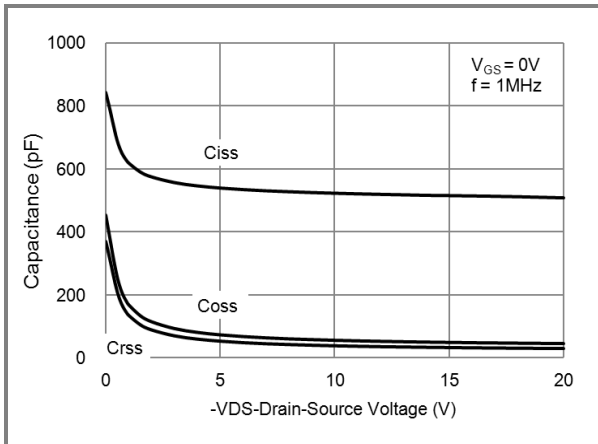


Fig.9 Threshold Voltage Variation with Temperature.

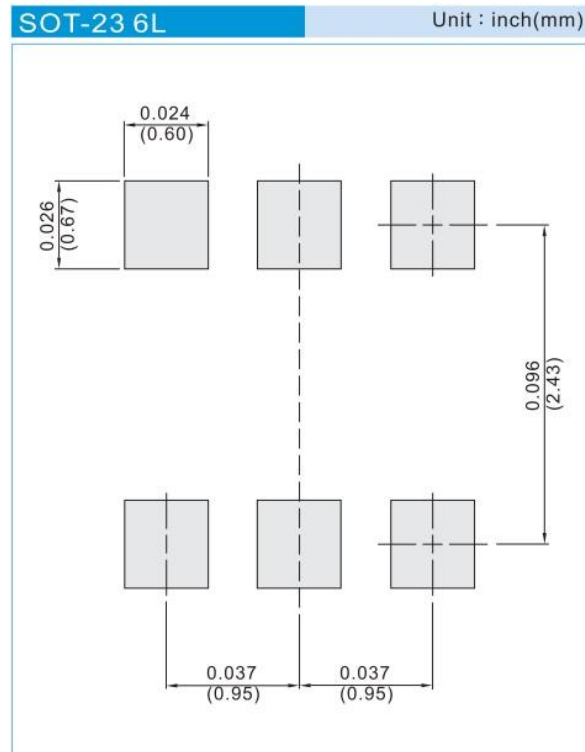


PJS6602

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJS6602_S1_00001	SOT-23 6L	3K pcs / 7" reel	SC2	Halogen free
PJS6602_S2_00001	SOT-23 6L	10K pcs / 13" reel	SC2	Halogen free

MOUNTING PAD LAYOUT





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