



PJSD05CTS

BI-DIRECTIONAL ESD PROTECTION DIODE

This Penta has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5Vdc and below. This offers an integrated solution to protect up to data line where the board space is a premium.

SPECIFICATION FEATURES

- 100W Power Dissipation (8/20 μ s Waveform)
- Low Leakage Current, Maximum of 0.5 μ A@5Vdc
- Very low Clamping voltage
- IEC 61000-4-2 ESD 15kV air, 8kV Contact Compliance
- In compliance with EU RoHS 2002/95/EC directivess

APPLICATIONS

- Video I/O ports protection
- Set Top Boxes
- Portable Instrumentation
- Case : SOD-523 plastic
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx Weight : 0.0014 grams
- Marking : RS

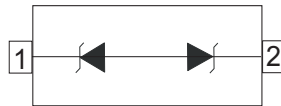
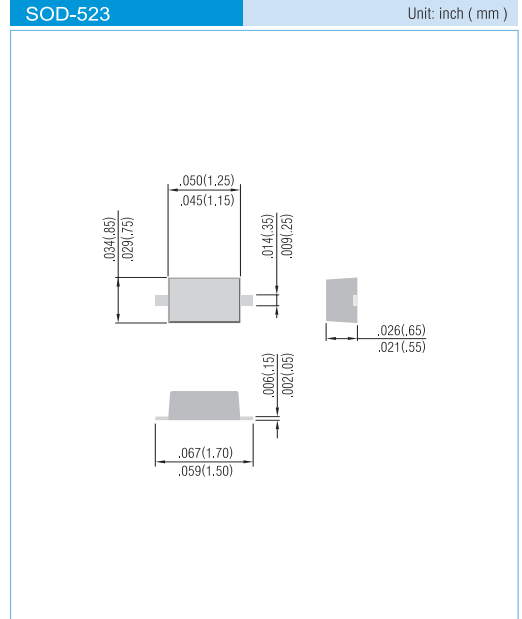


Fig.130



MAXIMUM RATINGS

Rating	Symbol	Value	Units
Peak Pulse Power (8/20 μ s Waveform)	P _{PP}	100	W
Peak Pulse Current (8/20 μ s Waveform)	I _{PP}	5.0	A
ESD Voltage (HBM)	V _{ESD}	>25	kV
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

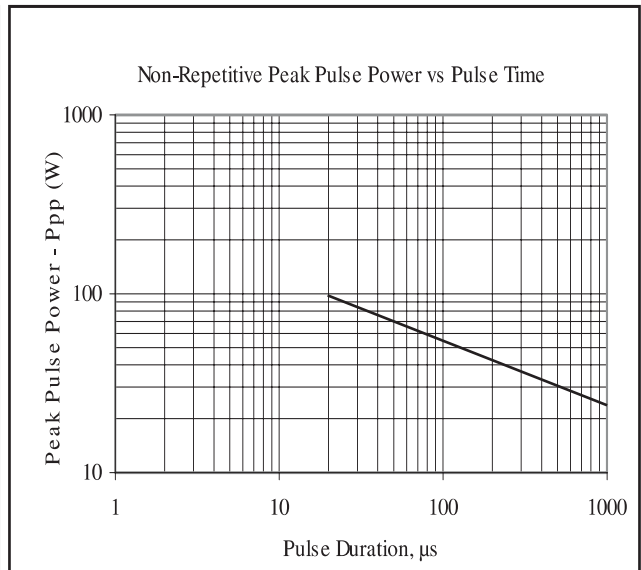
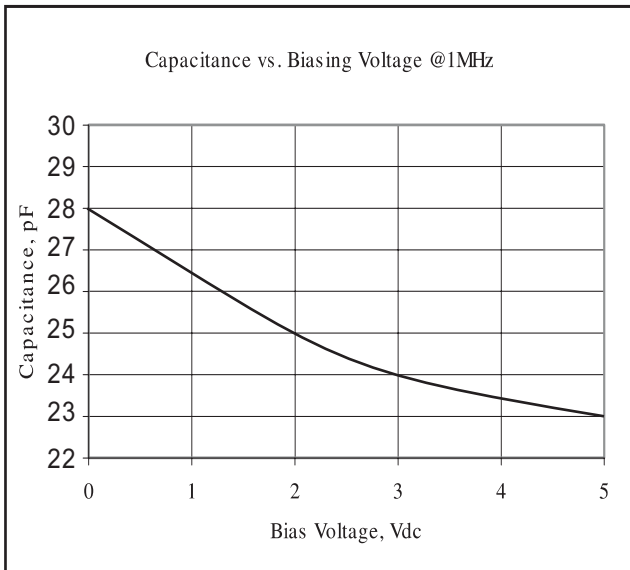
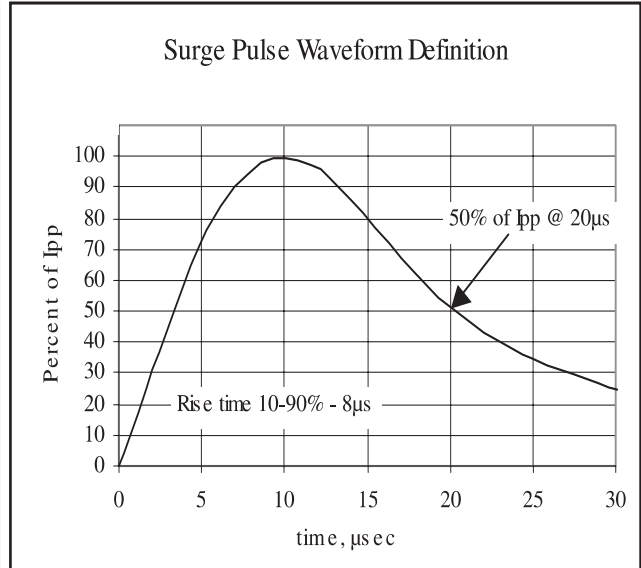
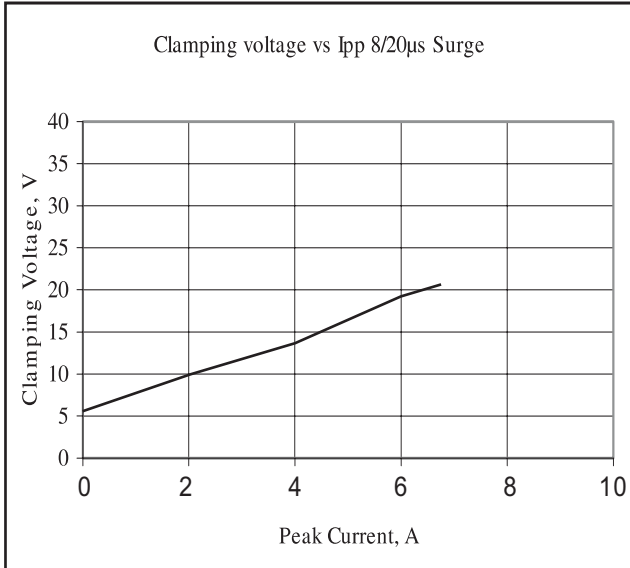
ELECTRICAL CHARACTERISTICS (T_A=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{WRM}		-	-	5.0	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} =1mA	5.78	-	7.82	V
Reverse Leakage Current	I _R	V _R =3.5V	-	-	0.5	μ A
Clamping Voltage (8/20 μ s)	V _C	I _{PP} =1A	-	-	12	V
Clamping Voltage (8/20 μ s)	V _C	I _{PP} =4A	-	-	15	V
Off State Junction Capacitance	C _J	0 Vdc Bias f=1MHz	-	-	30	pF
Off State Junction Capacitance	C _J	5 Vdc Bias f=1MHz	-	-	25	pF



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TYPICAL CHARACTERISTICS



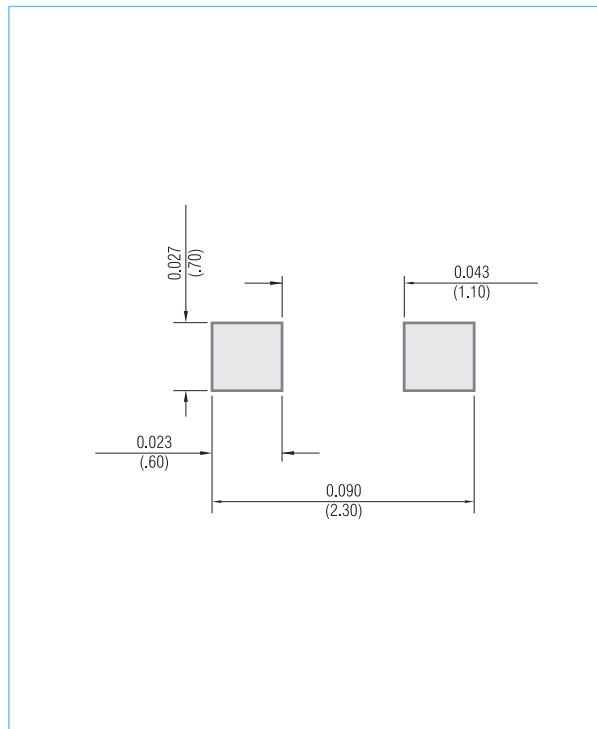


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MOUNTING PAD LAYOUT

SOD-523

Unit: inch (mm)



ORDER INFORMATION

- Packing information
 - T/R - 12K per 13" plastic Reel
 - T/R - 5K per 7" plastic Reel

LEGAL STATEMENT

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