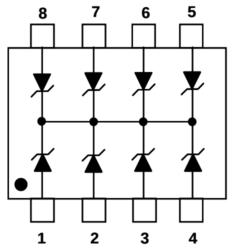
PJSMDA05C-7 SERIES

PANJIT SEMI CONDUCTOR

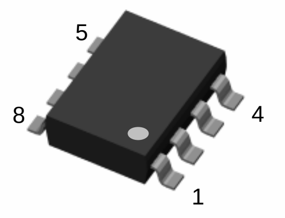
BI-DIRECTIONAL 7-TVS ARRAY

This 7 TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V, 12V, 15V and 24V. This TVS array offers an integrated solution to protect up to 7 data lines where the board space is a premium.



SPECIFICATION FEATURES

- **350W Power Dissipation (8x20µsec Waveform)**
- **Low Leakage Current, Maximum of 5µA at rated voltage**
- **Very Low Clamping Voltage**
- **IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance**
- **Packaged in the Industry Standard SOIC-8**
- **100% Tin Matte Finish (RoHS Compliant)**



SOIC-8

APPLICATIONS

- **RS-232C or RS-422 Communication ports**
- **GPIB/IEEE 485 Ports**
- **Portable Instrumentation**
- **Video Signal Ports**

MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{pp}	350	W
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-50 to +125	°C
Storage Temperature Range	T_{stg}	-50 to +150	°C

ELECTRICAL CHARACTERISTICS Tj = 25°C

PJSMDA05C-7

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 1mA	6			V
Reverse Leakage Current	I_R	V_R = 5V			5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5A			9.5	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 24A			13	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins			100	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins			60	pF

ELECTRICAL CHARACTERISTICS Tj = 25°C

PJSMDA12C-7

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	13.3			V
Reverse Leakage Current	I_R	V_R =12V			5	µA
Clamping Voltage (8x20µs)	V_c	I_{pp} =5A			17	V
Clamping Voltage (8x20µs)	V_c	I_{pp} = 15A			21	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins			50	pF

PJSMDA15C-7

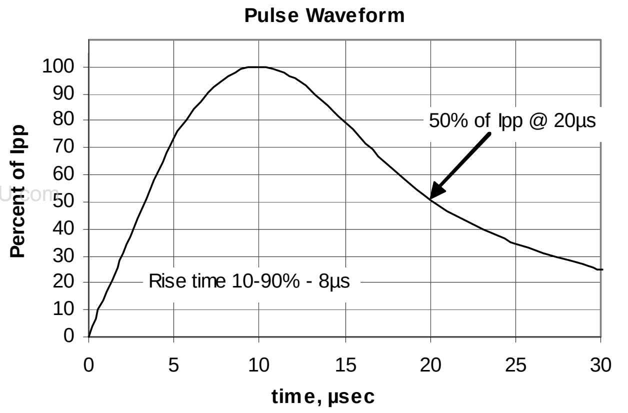
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	16.7			V
Reverse Leakage Current	I_R	V_R =15V			5	µA
Clamping Voltage (8x20µs)	V_c	I_{pp} =5A			22	V
Clamping Voltage (8x20µs)	V_c	I_{pp} = 12A			27	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins			40	pF

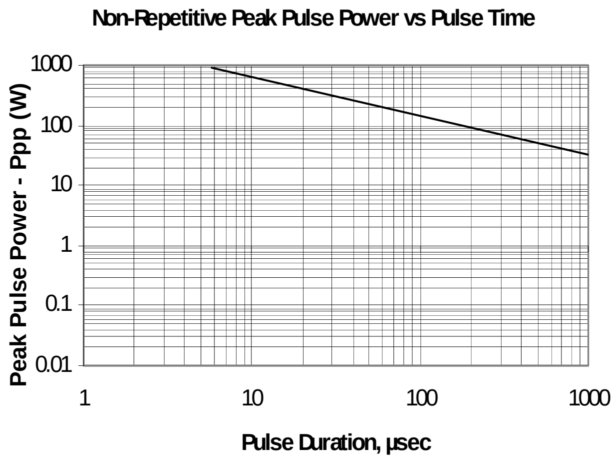
PJSMDA24C-7

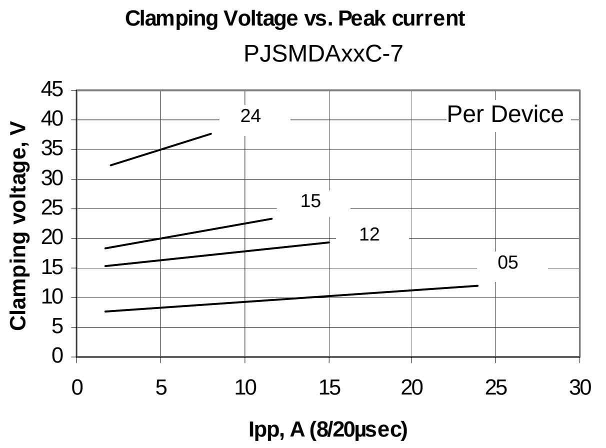
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				24	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	26.7			V
Reverse Leakage Current	I_R	V_R =24V			5	µA
Clamping Voltage (8x20µs)	V_c	I_{pp} =5A			35	V
Clamping Voltage (8x20µs)	V_c	I_{pp} = 8A			40	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins			30	pF

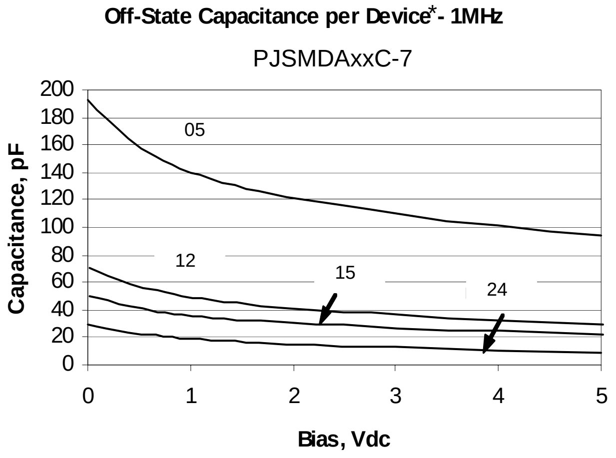
TYPICAL CHARACTERISTICS TJ = 25°C unless otherwise noted

Surge Pulse Waveform Definition



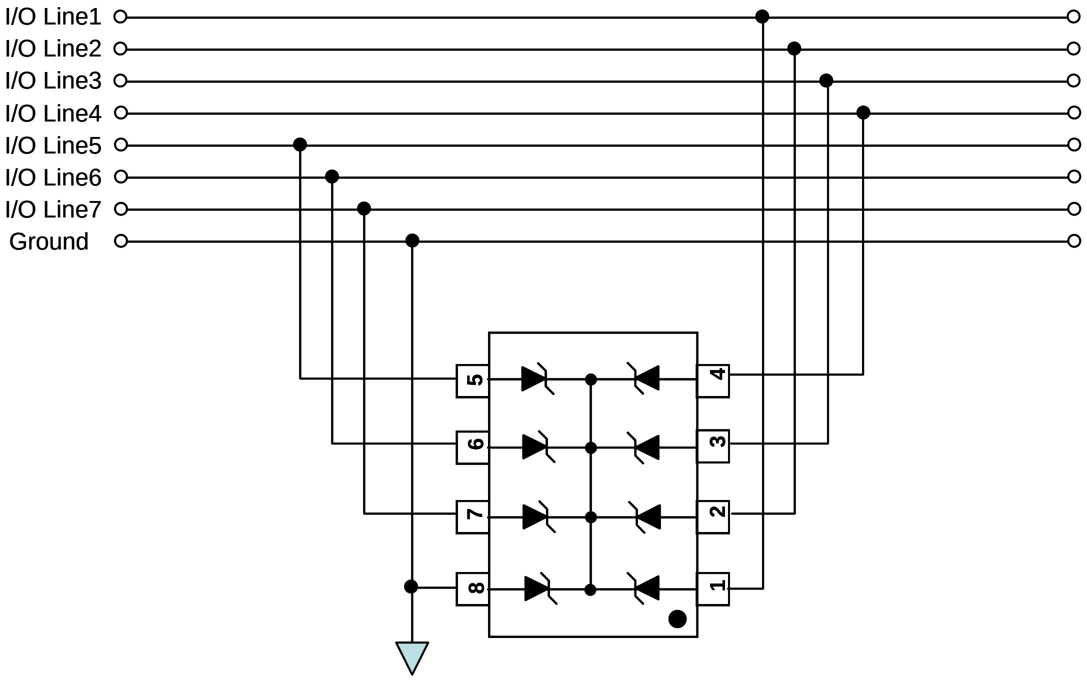




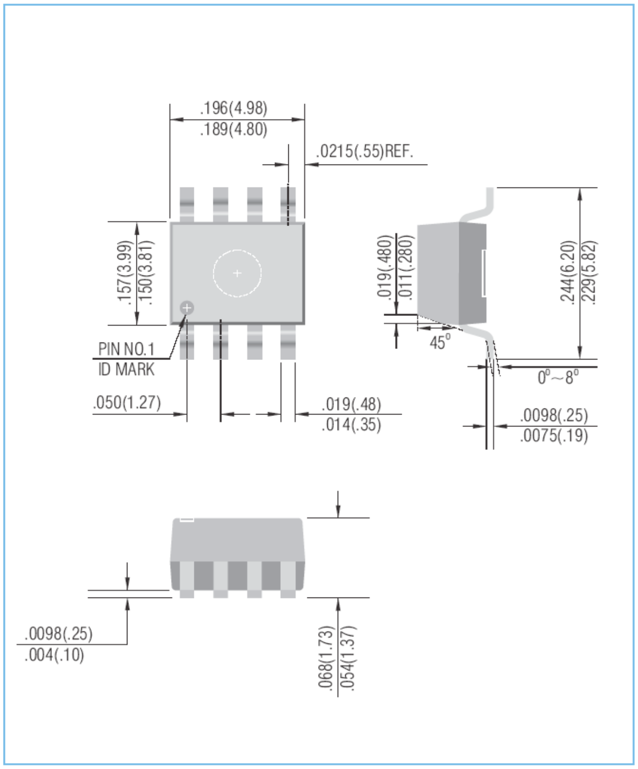


* Note: Capacitance between I/O Lines is half of the value shown here.

TYPICAL APPLICATION EXAMPLE AND PACKAGE DIMENSIONS



SOIC-08 Unit: inch (mm)



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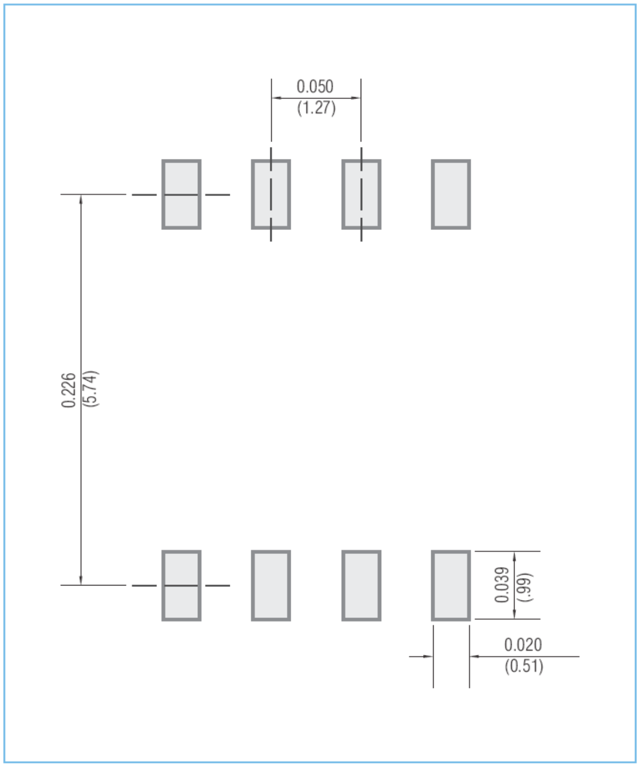

DEVICE MARKING INFORMATION

TVS	Marking Code
PJSMDA05C-7	B05
PJSMDA12C-7	B12
PJSMDA15C-7	B15
PJSMDA24C-7	B24