

## BI-DIRECTIONAL 7-TVS ARRAY

This 7 TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V, 12V, 15V and 24V. This TVS array offers an integrated solution to protect up to 7 data lines where the board space is a premium.

### SPECIFICATION FEATURES

- 350W Power Dissipation (8x20µsec Waveform)
- Low Leakage Current, Maximum of 5µA at rated voltage
- Very Low Clamping Voltage
- IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance
- Packaged in the Industry Standard SOIC-8
- 100% Tin Matte Finish (RoHS Compliant)

### APPLICATIONS

- RS-232C or RS-422 Communication ports
- GPIB/IEEE 485 Ports
- Portable Instrumentation
- Video Signal Ports

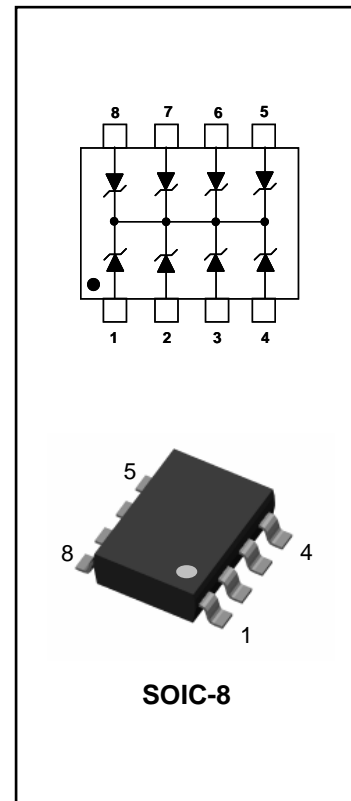
### MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	$P_{pp}$	350	W
ESD Voltage (HBM)	$V_{ESD}$	>25	kV
Operating Temperature Range	$T_J$	-50 to +125	°C
Storage Temperature Range	$T_{stg}$	-50 to +150	°C

### ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$

#### PJSMDA05C-7

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				5	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 1\text{mA}$	6			V
Reverse Leakage Current	$I_R$	$V_R = 5\text{V}$			5	µA
Clamping Voltage (8/20µs)	$V_c$	$I_{pp} = 5\text{A}$			9.5	V
Clamping Voltage (8/20µs)	$V_c$	$I_{pp} = 24\text{A}$			13	V
Off State Junction Capacitance	$C_j$	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins			100	pF
Off State Junction Capacitance	$C_j$	5 Vdc Bias $f = 1\text{MHz}$ Between I/O pins			60	pF





## ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$

### PJSMDA12C-7

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				12	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 1\text{mA}$	13.3			V
Reverse Leakage Current	$I_R$	$V_R = 12\text{V}$			5	$\mu\text{A}$
Clamping Voltage (8x20 $\mu\text{s}$ )	$V_C$	$I_{pp} = 5\text{A}$			17	V
Clamping Voltage (8x20 $\mu\text{s}$ )	$V_C$	$I_{pp} = 15\text{A}$			21	V
Off State Junction Capacitance	$C_j$	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins			50	pF

### PJSMDA15C-7

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				15	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 1\text{mA}$	16.7			V
Reverse Leakage Current	$I_R$	$V_R = 15\text{V}$			5	$\mu\text{A}$
Clamping Voltage (8x20 $\mu\text{s}$ )	$V_C$	$I_{pp} = 5\text{A}$			22	V
Clamping Voltage (8x20 $\mu\text{s}$ )	$V_C$	$I_{pp} = 12\text{A}$			27	V
Off State Junction Capacitance	$C_j$	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins			40	pF

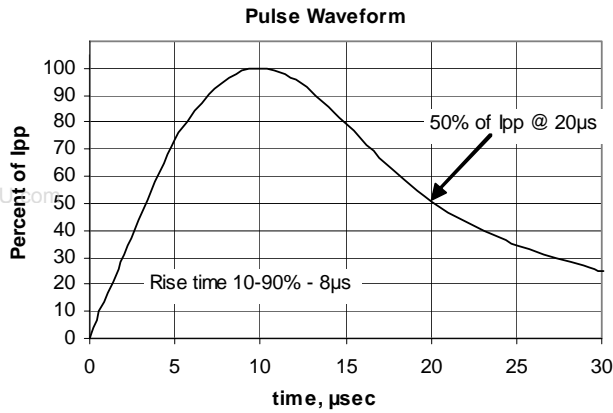
### PJSMDA24C-7

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				24	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 1\text{mA}$	26.7			V
Reverse Leakage Current	$I_R$	$V_R = 24\text{V}$			5	$\mu\text{A}$
Clamping Voltage (8x20 $\mu\text{s}$ )	$V_C$	$I_{pp} = 5\text{A}$			35	V
Clamping Voltage (8x20 $\mu\text{s}$ )	$V_C$	$I_{pp} = 8\text{A}$			40	V
Off State Junction Capacitance	$C_j$	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins			30	pF

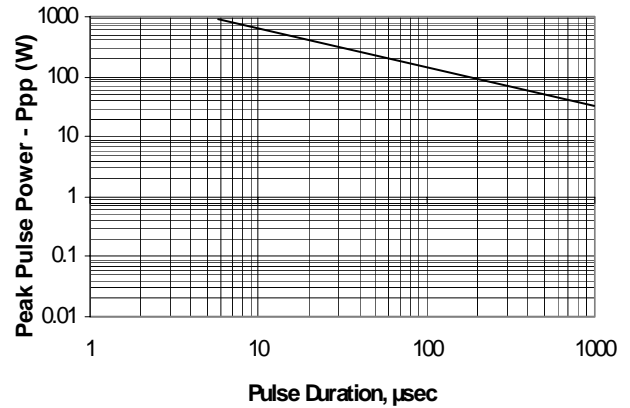


TYPICAL CHARACTERISTICS TJ = 25°C unless otherwise noted

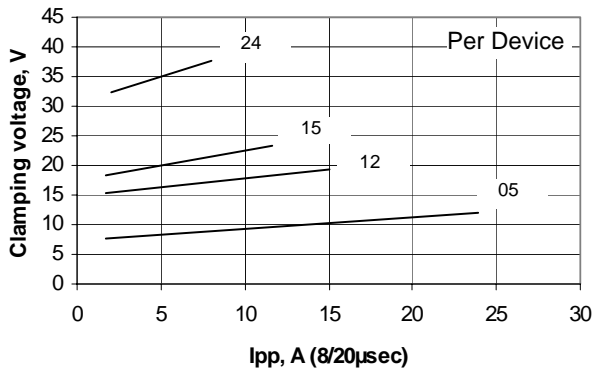
Surge Pulse Waveform Definition



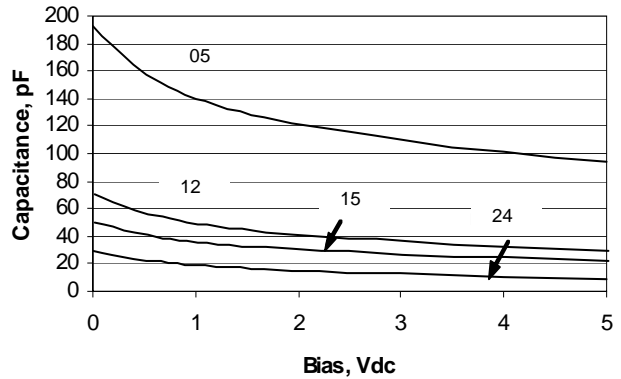
Non-Repetitive Peak Pulse Power vs Pulse Time



Clamping Voltage vs. Peak current PJSMDAxxC-7

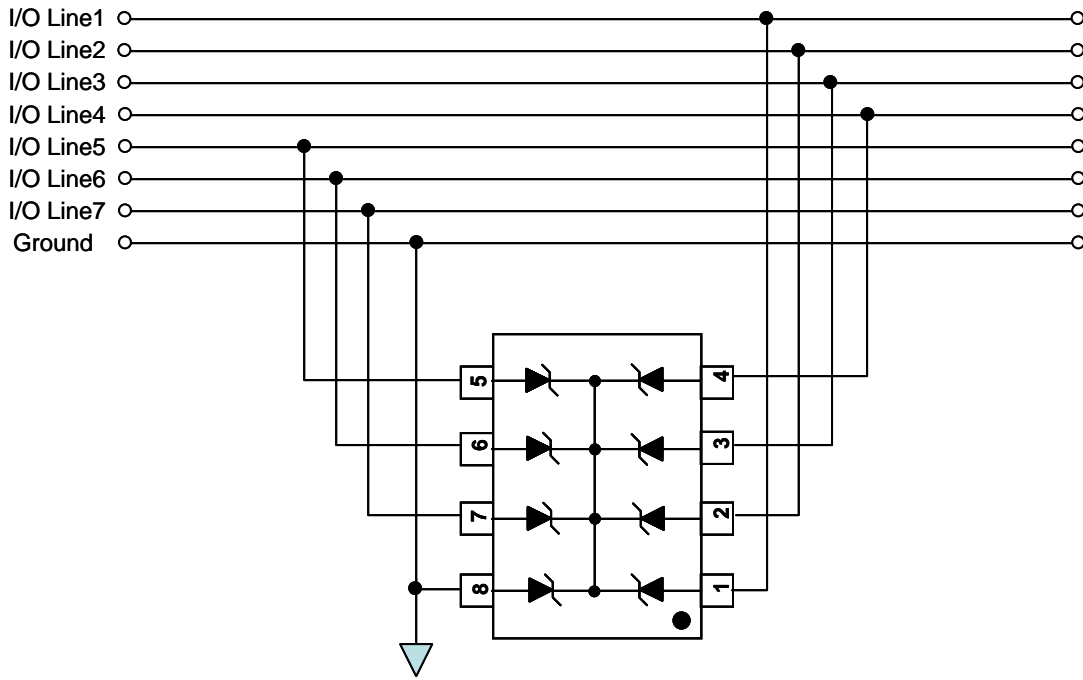


Off-State Capacitance per Device\* - 1MHz PJSMDAxxC-7



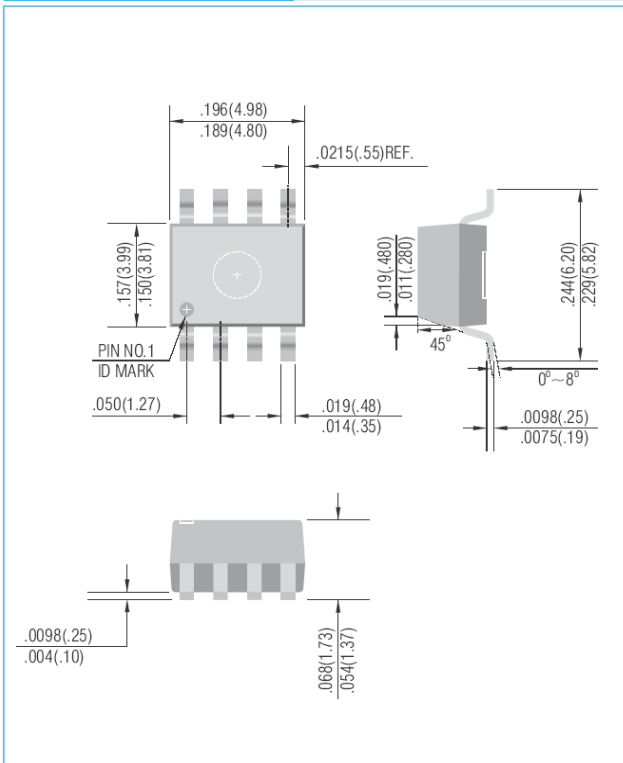
\* Note: Capacitance between I/O Lines is half of the value shown here.

TYPICAL APPLICATION EXAMPLE AND PACKAGE DIMENSIONS

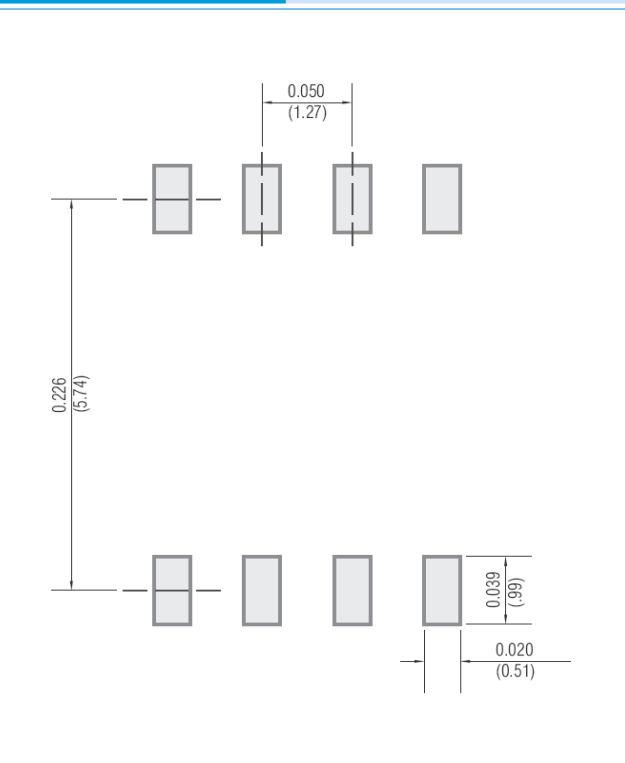


www.DataSheet4U.com

SOIC-08 Unit: inch ( mm )



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**DEVICE MARKING INFORMATION**

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TVS	Marking Code
PJSMDA05C-7	B05
PJSMDA12C-7	B12
PJSMDA15C-7	B15
PJSMDA24C-7	B24

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