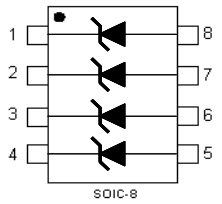
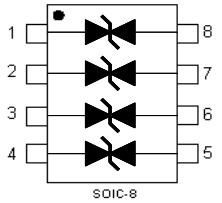
QUAD TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

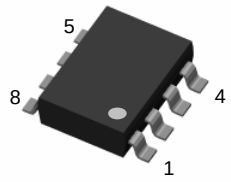
This Quad TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V, 12V, 15V and 24V for Unidirectional and Bi-directional protection options. This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.



PJSMDA05 Series



PJSMDA05C Series



SPECIFICATION FEATURES

- **350W Power Dissipation (8/20µs Waveform)**
- **Low Leakage Current, Maximum of 5µA at rated voltage**
- **Very Low Clamping Voltage**
- **IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance**
- **Packaged in the Industry Standard SOIC-8**
- **Unidirectional and Bi-directional Protection Options**
- **100% Tin Matte Finish (RoHS Compliant)**

APPLICATIONS

- **RS-232C or RS-422 Communication ports**
- **GPIB/IEEE 485 Ports**
- **Portable Instrumentation**

MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{pp}	350	W
ESD Voltage (HBM) Per MIL-STD-883C	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-50 to +125	°C
Storage Temperature Range	T_{stg}	-50 to +150	°C

ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMDA05, 05C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 1mA	6			V
Reverse Leakage Current	I_R	V_R = 5V			5	µA
Clamping Voltage (8/20µs)	V_C	I_{pp} = 5A			9.5	V
Clamping Voltage (8/20µs)	V_C	I_{pp} = 24A			13	V
Off State Junction Capacitance*	Cj	0 Vdc Bias f = 1MHz			200	pF
Off State Junction Capacitance*	Cj	5 Vdc Bias f = 1MHz			110	pF

*Note: Off-state capacitance in the bi-directional version is half of the value shown for the unidirectional.

ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMDA12, 12C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	13.3			V
Reverse Leakage Current	I_R	V_R = 12V			5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5A			17	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 15A			21	V
Off State Junction Capacitance*	Cj	0 Vdc Bias f = 1MHz			90	pF

PJSMDA15, 15C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	16.7			V
Reverse Leakage Current	I_R	V_R = 15V			5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5A			22	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 12A			27	V
Off State Junction Capacitance*	Cj	0 Vdc Bias f = 1MHz			70	pF

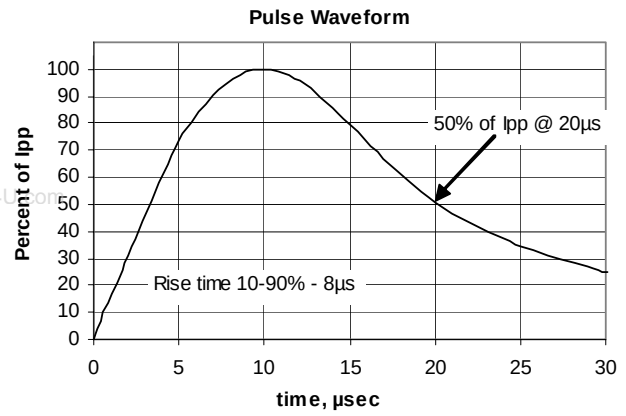
PJSMDA24, 24C

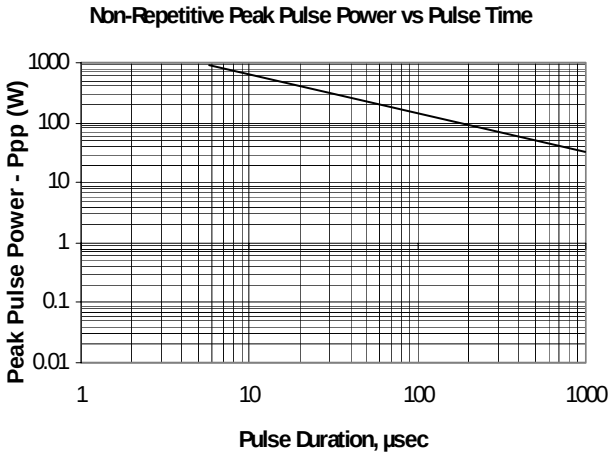
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				24	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	26.7			V
Reverse Leakage Current	I_R	V_R = 24V			5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5A			35	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 8A			40	V
Off State Junction Capacitance*	Cj	0 Vdc Bias f = 1MHz			50	pF

*Note: Off-state capacitance in the bi-directional version is half of the value shown for the unidirectional.

TYPICAL CHARACTERISTICS TJ = 25°C unless otherwise noted

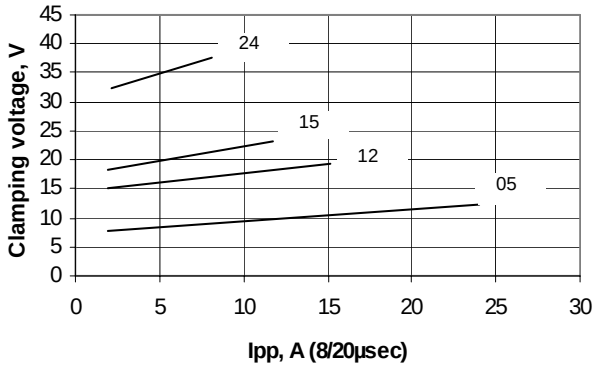
Surge Pulse Waveform Definition





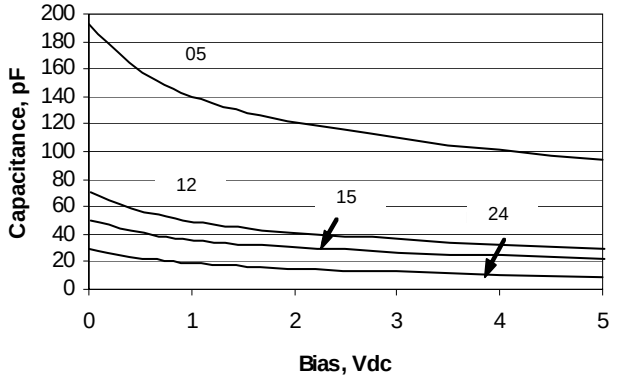
Clamping Voltage vs. Peak current

PJSMDAxx, xxC



Off-State Capacitance per Device - 1MHz

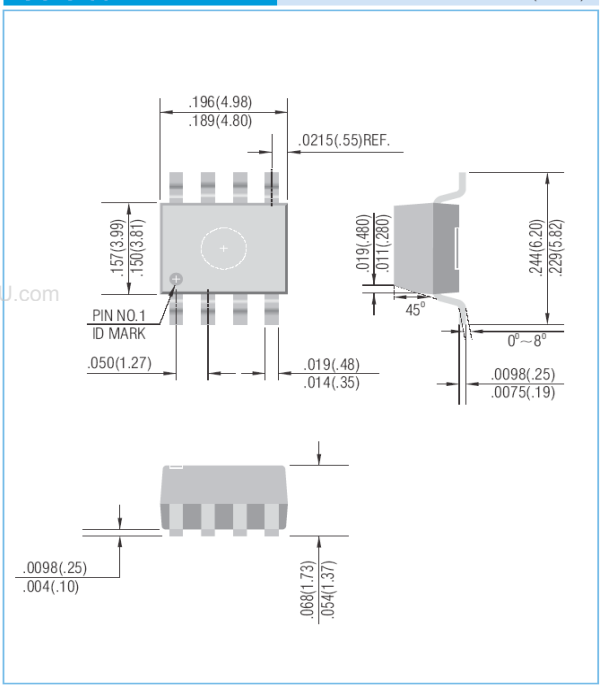
PJSMDAxx, xxC*



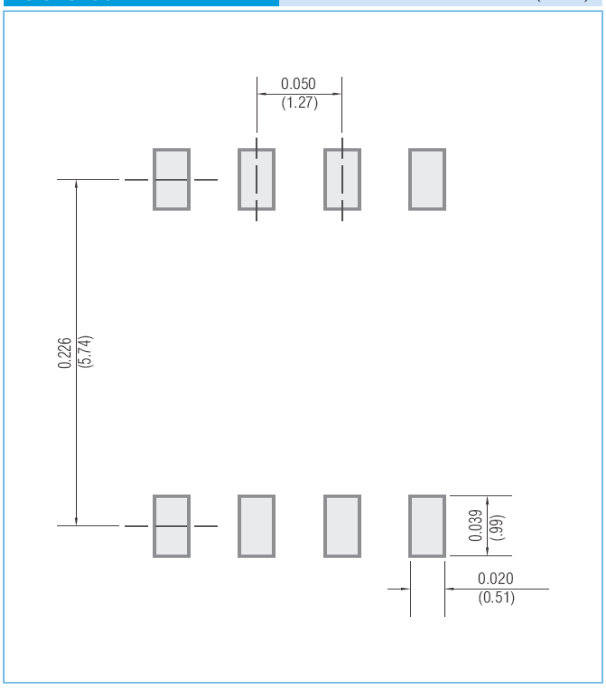
*Note: Off-state capacitance in the bi-directional version is half of the value shown for the unidirectional.

PACKAGE AND LAYOUT DIMENSIONS

SOIC-08 Unit: inch (mm)



SOIC-08 Unit: inch (mm)



DEVICE MARKING INFORMATION

TVS	Marking Code
PJSMDA05	DA5
PJSMDA12	DA2
PJSMDA15	DAA
PJSMDA24	DA4
PJSMDA05C	DC5
PJSMDA12C	DC2
PJSMDA15C	DCC
PJSMDA24C	DC4