Crystal Image through Imaging Innovation
PIXELPLUS

Datasheet

1/2.7 inch FHD Bayer Chip
CMOS Image Sensor with 1960x1120 Pixel Array

PK5210N

Rev 0.4

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- Output Format
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  - Tone-mapped RGB bayer
  - Separate RGB bayer
- Output Interface
  - DVP(Digital Video Parallel) 12-bit
  - 2-lane MIPI
- High dynamic range
- Auto black level compensation
- Programmable frame size, frame rate, window size, exposure and white balance gain
- Horizontal/Vertical mirroring
- Image processing : DPC, Combine, Compress, ADG(Adaptive Digital Gain), Tone-mapping
- External synchronization support (Genlock)
- Chip address selection PAD (2ea)
- Software reset
- On-chip phase locked loop (PLL)
- I2C Interface support
- SKIP, Cropping (Row)

General Description

The PK5210N is a 1/2.7-inch CMOS image sensor. It is a bayer sensor with an effective pixel array of 1960 (width) x 1120 (height). The PK5210N can generate a 12-bit combine & compressed RGB bayer data or a 12-bit tone-mapped RGB bayer data at maximum frame rate of 30 fps through MIPI serial interface or DVP(Digital Video Parallel) 12-bit interface. On-chip sensor functions can be controlled through I2C interface.

Table 1 Key Performance Parameter

Parameter	Typical value
Pixel size	3.0 [um] x 3.0 [um]
Effective pixel array	1960(H) x 1120(V)
Effective image area	5.880 [mm] x 3.360 [mm]
Optical format	1/2.7 [inch]
Input clock frequency	27 [MHz]
Output interface	DVP(Digital Video Parallel) 12-bit
	MIPI serial interface with 2 lane
Max. frame rate	30 [FPS]
Dark signal	41.9 [e/sec]
Sensitivity	35.6K [e/lux*sec]
Power supply	HVDD : 1.8 ~ 3.3 [V] @ DVP HVDD : 3.3 [V] @ MIPI
	AVDD : 3.3 [V]
	DVDD : 1.3 [V]
	DVDDM : 1.3 [V]
Power consumption	341 [mW] @ DVP (HVDD = 3.3[V]) 277 [mW] @ DVP (HVDD = 1.8[V]) 258 [mW] @ MIPI 0.87 [mW] @ Standby
Operating temp. (Fully functional temp.)	-40~105 [°C] (Ambient)
Dynamic range	120 [dB]
SNR	44.9 [dB]
Package type	64 CLCC

Chip Architecture

The PK5210N has a 1960 x 1128 total pixel array and includes column/row driver circuits for reading out pixel data progressively. CDS circuit reduces noises generated from various sources, which mainly are resulted from process variations. The fixed error signal level caused by pixel process variation can be reduced by sampling the difference between the output and the reset level of the pixel. Each of R, G, and B pixel output can be multiplied by different gain factors to balance the color of images under various light conditions. The analog signals are converted into digital data one line at a time and each line data is streamed out column by column. The bayer RGB data passes through a sequence of image signal processing to produce bayer output data. Image signal processing includes operations such as DPC, combine, compress, tone-mapping and adaptive digitalgain(ADG). The PK5210N supports output interfaces such as a 12-bit parallel and the MIPI. The control of internal functions and output signal timings can be enabled by modifying registers directly through a 2-wire serial interface called I2C.

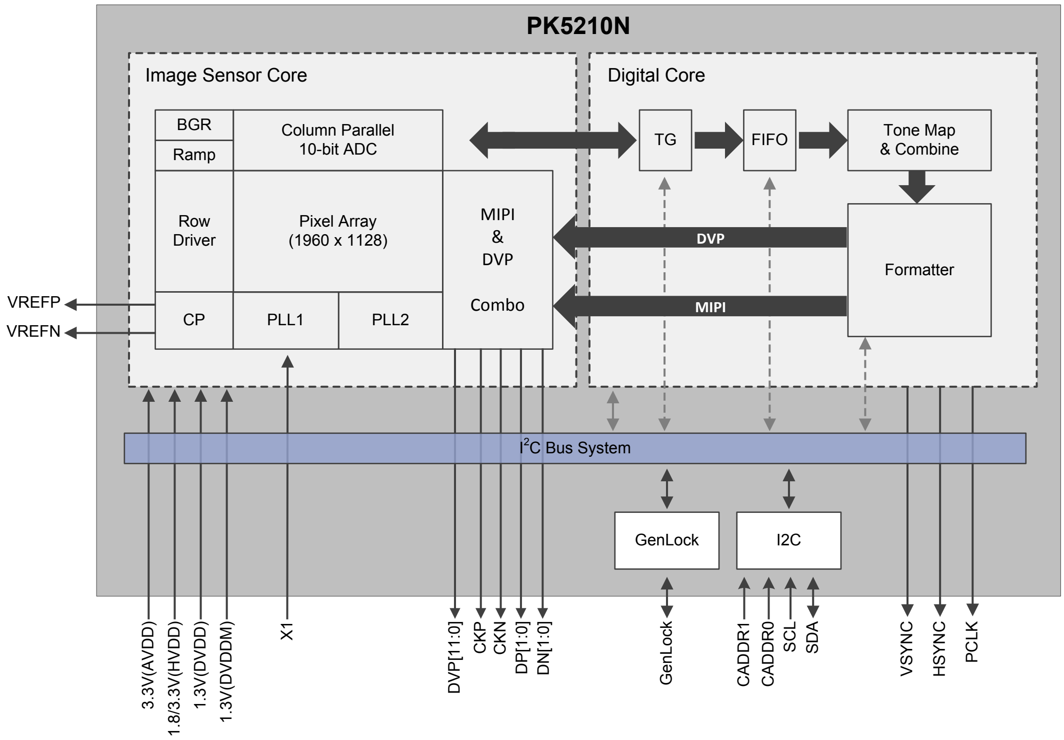


Figure 1 Chip architecture

Frame Structure

The size of a frame is determined by framewidth and frameheight registers. One frame consists of (framewidth + 1) columns and (frameheight + 1) rows, where the size of one frame is allowed to be larger than the total pixel array size. Window determines the output image size, and its default size is 1920 x 1080 pixels. It is possible to define a specific region of the frame by a determined window. Pixel scanning is performed row by row on entire frame. Frame row counter and frame column counter, which are limited by framewidth and frameheight values respectively, are used to indicate the current coordinate of pixel being scanning. The column counter value increases by every pixel clock (pclk). every time the column counter reaches maximum value, the row counter value increase. Figure 2 shows the default frame structure and the window position of the PK5210N with origin point (0,0) in the top right corner .

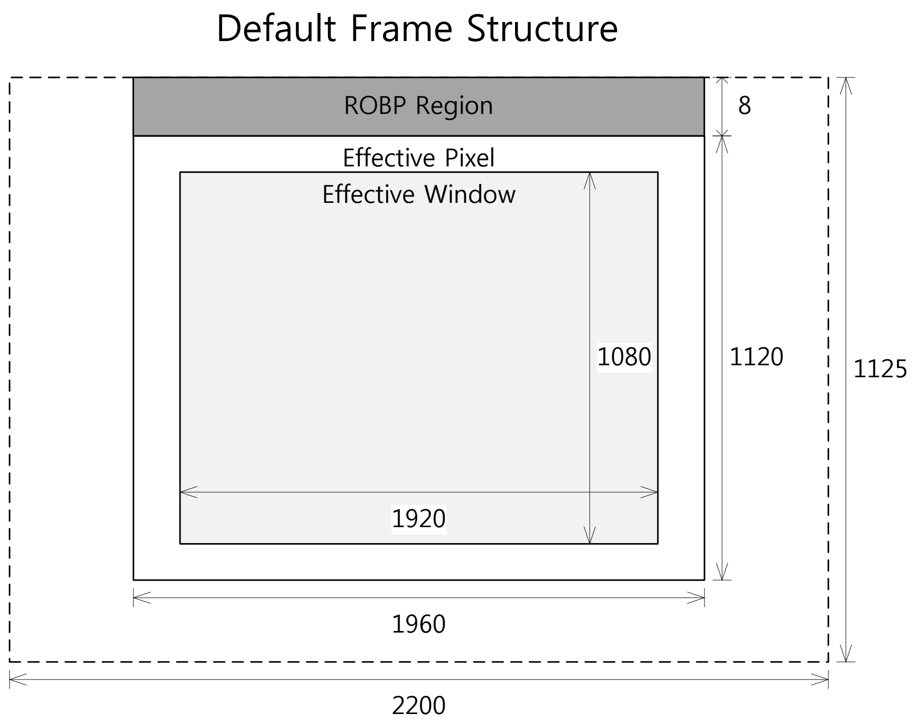


Figure 2 Default frame structure(top view)

Table 2 Register Table - Frame structure

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
framewidth_h	A	06	[4:0]	0x08	RW	aev	Framewidth High Byte (must be larger than window width)
framewidth_l	A	07	[7:0]	0x97	RW	aev	Framewidth Low Byte (must be larger than window width)
fheight_a_h	A	08	[4:0]	0x04	RW	aev	Frameheight High Byte (must be larger than window height)
fheight_a_l	A	09	[7:0]	0x7C	RW	aev	Frameheight Low Byte (must be larger than window height)

Pixel Data Format

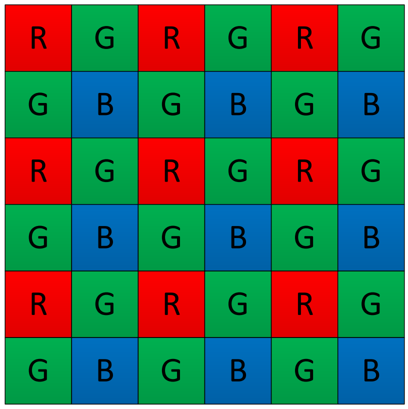


Figure 3 Bayer color filter pattern

The pixel array is covered by bayer color filters as shown in the Figure 3. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PK5210N provides RGB bayer pattern data through a 10-bit channel which passes one pixel data to the output bus at every pclk.

The PK5210N provides horizontal, vertical mirror which respectively reverse the sensor data readout order horizontally and vertically. Figure 4 shows a normal image and a mirrored image.

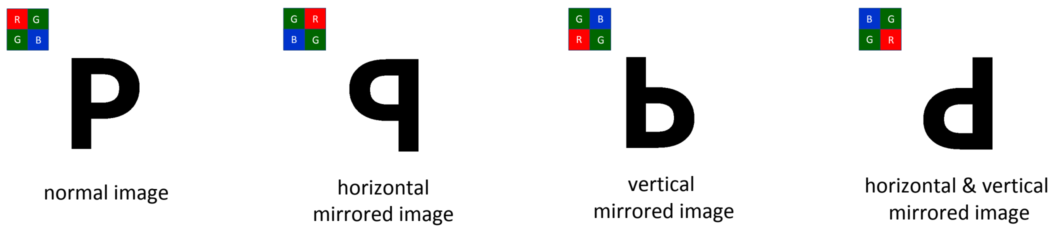


Figure 4 Mirror

Table 3 shows registers relevant to mirror.

Table 3 Register Table - Mirror

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
mirror	A	05	[1:0]	0x00	RW	aev	Image Inversion mirror[1] : vertical inversion mirror[0] : horizontal inversion

Parallel Formatter

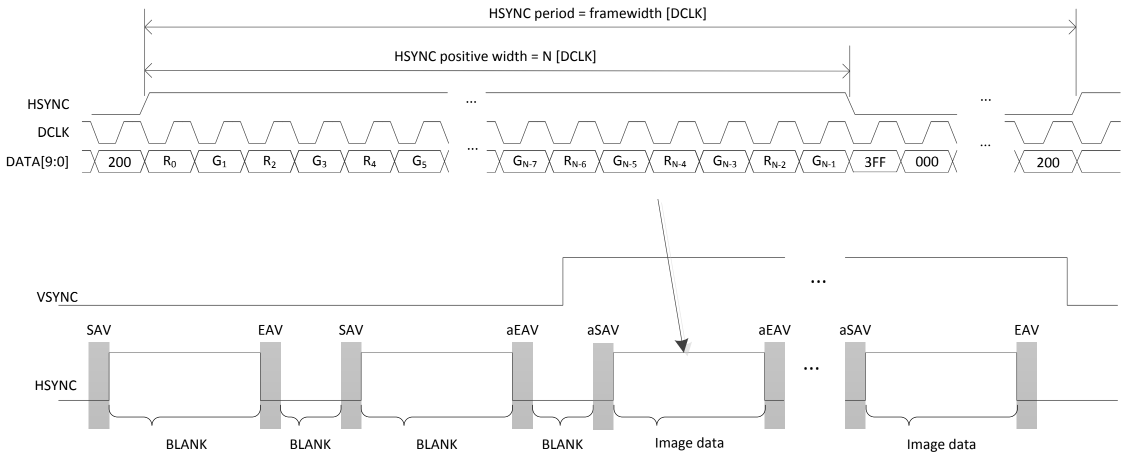


Figure 5 Parallel format timing

The parallel data is controlled by format header, also called timing reference sequence (TRS). The TRS indicates start or end of video and is included with pixel data during serial transfer. Figure 6 shows TRS and vertical timing.

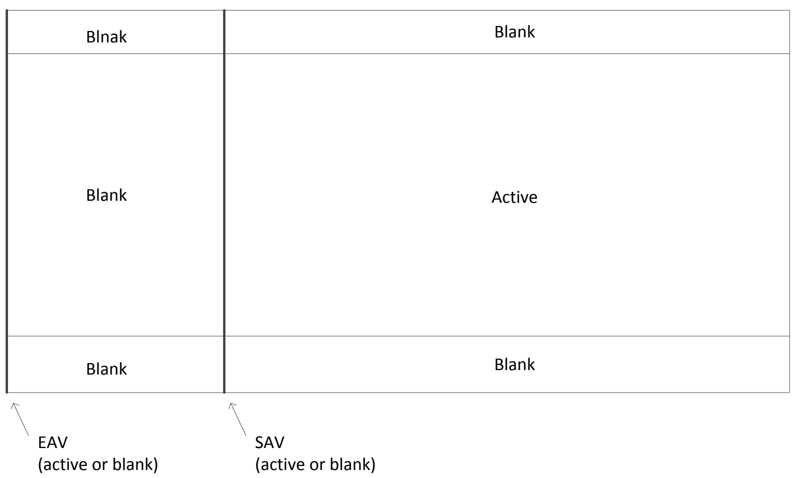


Figure 6 Parallel format

SAV, EAV, aEAV, aSAV and blank data shown in Figure 6 are generated as follows.

```
SAV   = {sync_CCIR_FF, sync_CCIR_00, sync_CCIR_00, sync_blankSAV}
EAV   = {sync_CCIR_FF, sync_CCIR_00, sync_CCIR_00, sync_blankEAV}
aSAV  = {sync_CCIR_FF, sync_CCIR_00, sync_CCIR_00, sync_activeSAV}
aEAV  = {sync_CCIR_FF, sync_CCIR_00, sync_CCIR_00, sync_activeEAV}
BLANK = {sync_CCIR_80, sync_CCIR_10} - - - {sync_CCIR_80, sync_CCIR_10}
```

Table 4 Register Table - Parallel format

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_blankEAV_h	A	63	[3:0]	0x0B	RW		Blanking EAV control High Byte
sync_blankEAV_l	A	64	[7:0]	0x60	RW		Blanking EAV control Low Byte
sync_blankSAV_h	A	65	[3:0]	0x0A	RW		Blanking SAV control High Byte
sync_blankSAV_l	A	66	[7:0]	0xB0	RW		Blanking SAV control Low Byte
sync_activeEAV_h	A	67	[3:0]	0x09	RW		Active EAV control High Byte
sync_activeEAV_l	A	68	[7:0]	0xD0	RW		Active EAV control Low Byte
sync_activeSAV_h	A	69	[3:0]	0x08	RW		Active SAV control High Byte
sync_activeSAV_l	A	6A	[7:0]	0x00	RW		Active SAV control Low Byte
sync_CCIR_FF_h	A	6B	[3:0]	0x0F	RW		Format header control 0 (FF) High Byte
sync_CCIR_FF_l	A	6C	[7:0]	0xFF	RW		Format header control 0 (FF) Low Byte
sync_CCIR_00_h	A	6D	[3:0]	0x00	RW		Format header control 1 (00) High Byte
sync_CCIR_00_l	A	6E	[7:0]	0x00	RW		Format header control 1 (00) Low Byte
sync_CCIR_80_h	A	6F	[3:0]	0x08	RW		Blank data control 0 (80) High Byte
sync_CCIR_80_l	A	70	[7:0]	0x00	RW		Blank data control 0 (80) Low Byte
sync_CCIR_10_h	A	71	[3:0]	0x01	RW		Blank data control 1 (10) High Byte
sync_CCIR_10_l	A	72	[7:0]	0x00	RW		Blank data control 1 (10) Low Byte

When data_clamp is enabled, active data is clamped by data_min and data_max as shown in Table 5. data_min determines minimum value of active data, and data_max determines maximum value of active data. Table 6 shows registers relevant to data clamp.

Table 5 Register Table - Active data(data_cmlamp = enable)

output bit	data_min	data_max
MSB 8bit	010h	FE0h
MSB 9bit	008h	FF0h
MSB 10bit	004h	FF8h
MSB 11bit	002h	FFCh
MSB 12bit	001h	FFEh

Table 6 Register Table - Data clamp

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
data_clamp	A	AE	[1]	1'b0	RW	aev	Effective data clamping enable 1'b0 : disable 1'b1 : enable
data_min_h	A	B0	[3:0]	0x00	RW		Minimum active data High Byte
data_min_l	A	B1	[7:0]	0x00	RW		Minimum active data Low Byte
data_max_h	A	B2	[3:0]	0x0F	RW		Maximum active data High Byte
data_max_l	A	B3	[7:0]	0xFF	RW		Maximum active data Low Byte

Vsync and Hsync

By manipulating vsyncstartrow0, vsyncstoprow0, and vsynccolumn0 register value, start and stop positions of vsync are controlled. sync_drop register allows user to drop vsync or hsync. Figure 7 shows 4 different cases of sync_drop. In addition, sync_hsyncAllLines enables hsync during vsync blank region. Figure 8 shows operation of sync_hsyncAlllines.

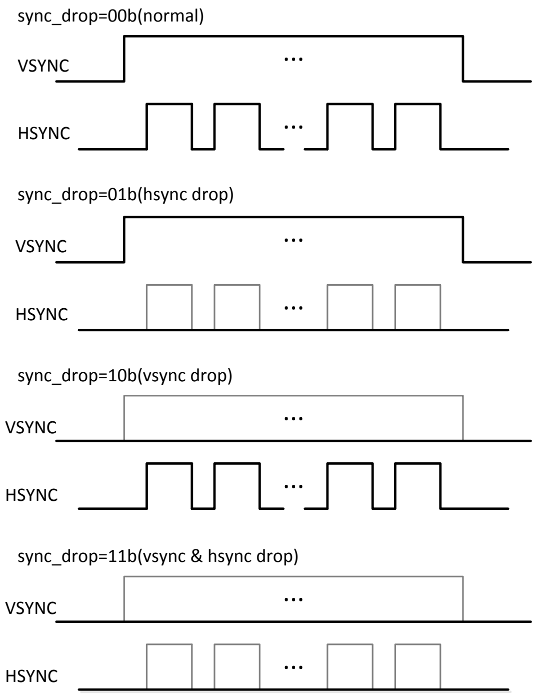


Figure 7 Sync drop

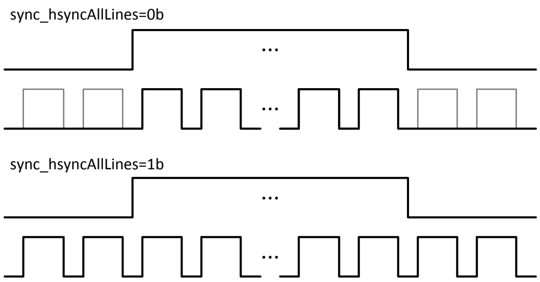


Figure 8 Hsync all lines

sync_vsyncPolarity, sync_hsyncPolarity registers invert vsync, hsync signal respectively. The inversion functions are shown in Figure 9, Figure 10.

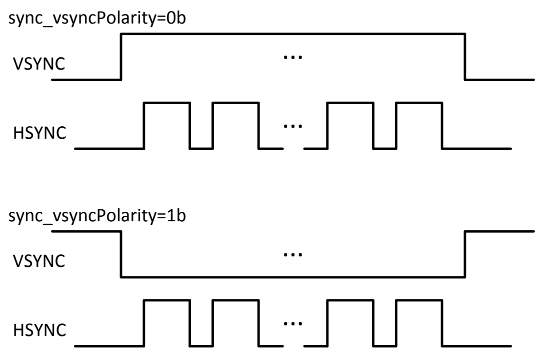


Figure 9 Vsync polarity

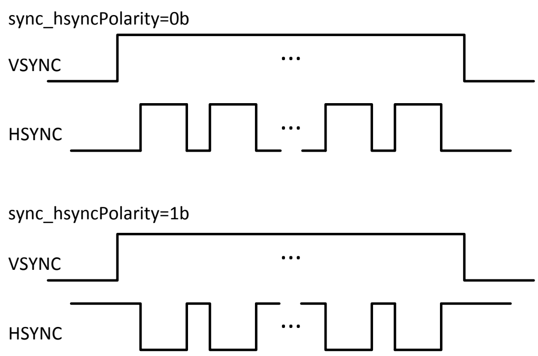


Figure 10 Hsync polarity

Table 7 Register Table - Sync control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
vsyncstartrow0_h	A	74	[4:0]	0x00	RW	aev	Parallel interface - Vertical sync start control High Byte MIPI interface @ Virtual channel 0 - Frame start control High Byte
vsyncstartrow0_l	A	75	[7:0]	0x17	RW	aev	Parallel interface - Vertical sync start control Low Byte MIPI interface @ Virtual channel 0 - Frame start control Low Byte
vsyncstoprow0_h	A	76	[4:0]	0x04	RW	aev	Parallel interface - Vertical sync end control High Byte MIPI interface @ Virtual channel 0 - Frame end control High Byte
vsyncstoprow0_l	A	77	[7:0]	0x5F	RW	aev	Parallel interface - Vertical sync end control Low Byte MIPI interface @ Virtual channel 0 - Frame end control Low Byte
vsynccolumn0_h	A	78	[4:0]	0x00	RW	aev	Internal vsync 0 start point High Byte @ column counter
vsynccolumn0_l	A	79	[7:0]	0x02	RW	aev	Internal vsync 0 start point Low Byte @ column counter

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_drop	A	AD	[6:5]	2'b00	RW	aev	Vsync, hsync drop control 2'b00 : No drop 2'b01 : vsync drop 2'b10 : hsync drop 2'b11 : hsync and vsync drop
sync_vsyncPolarity	A	AE	[6]	1'b0	RW	aev	Vsync polarity change 1'b0 : disable 1'b1 : enable
sync_hsyncPolarity	A	AE	[4]	1'b0	RW	aev	Hsync polarity change 1'b0 : disable 1'b1 : enable
sync_hsyncAllLines	A	AE	[5]	1'b0	RW	aev	Hsync output all lines enable(black and active) 1'b0 : No hsync during vertical blank 1'b1 : hsync during vertical blank

PCLK

PCLK inversion can be enabled via pclk_pol register as shown in Figure 11.

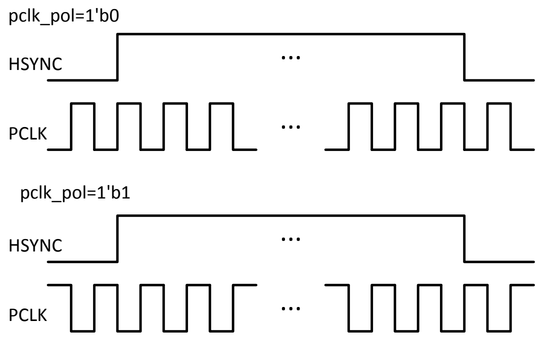


Figure 11 PCLK polarity

Table 8 Register Table - PCLK control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pclk_polarity	A	25	[2]	1'b0	RW		Change PCLK phase

Digital Parallel Interface

The digital parallel interface uses VSYNC, HSYNC, PCLK, D[11:0] PIN. Table 9 shows digital parallel interface control registers.

Table 9 Register Table - digital parallel interface

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pclk_pad_en	A	25	[3]	1'b0	RW		PCLK pad enable 1'b0 : disable 1'b1 : enable
pclk_drv	A	24	[5:4]	2'b00	RW		PCLK pad drivability control
dly_digi_PCLK	A	24	[3:0]	4'b0000	RW		PCLK timing delay delay = dly_digi_PCLK*0.4 ns
vsync_pad_en	A	25	[7]	1'b0	RW		Vsync pad enable 1'b0 : disable 1'b1 : enable
hsync_drv	A	25	[6:5]	2'b00	RW		Hsync Pad drivability control
hsync_pad_en	A	25	[4]	1'b0	RW		Hsync pad enable 1'b0 : disable 1'b1 : enable
pad_drv	A	24	[7:6]	2'b00	RW		Data pad drivability control
dpad_swap	A	25	[1]	1'b0	RW		Data pad swap option 1'b0 : [MSB:LSB] 1'b1 : [LSB:MSB]
d11_pad_en	A	26	[7]	1'b0	RW		D11 pad control 1'b0 : disable 1'b1 : enable
d10_pad_en	A	26	[6]	1'b0	RW		D10 pad control 1'b0 : disable 1'b1 : enable
d9_pad_en	A	26	[5]	1'b0	RW		D9 pad control 1'b0 : disable 1'b1 : enable
d8_pad_en	A	26	[4]	1'b0	RW		D8 pad control 1'b0 : disable 1'b1 : enable
d7_pad_en	A	26	[3]	1'b0	RW		D7 pad control 1'b0 : disable 1'b1 : enable
d6_pad_en	A	26	[2]	1'b0	RW		D6 pad control 1'b0 : disable 1'b1 : enable
d5_pad_en	A	26	[1]	1'b0	RW		D5 pad control 1'b0 : disable 1'b1 : enable
d4_pad_en	A	26	[0]	1'b0	RW		D4 pad control 1'b0 : disable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b1 : enable
d3_pad_en	A	27	[7]	1'b0	RW		D3 pad control 1'b0 : disable 1'b1 : enable
d2_pad_en	A	27	[6]	1'b0	RW		D2 pad control 1'b0 : disable 1'b1 : enable
d1_pad_en	A	27	[5]	1'b0	RW		D1 pad control 1'b0 : disable 1'b1 : enable
d0_pad_en	A	27	[4]	1'b0	RW		D0 pad control 1'b0 : disable 1'b1 : enable

Recommended Power Sequence

- AVDD : Analog block (external 3.3[V])
- HVDD : IO (external 1.8[V], 3.3[V] / MIPI only 3.3[V])
- DVDD : TG & ISP (external 1.3[V])
- DVDDM : MIPI (external 1.3[V])

Table 10 Recommended power-on/off sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From HVDD rising to DVDD rising	0	-	100	ms
t2	From DVDD rising to AVDD & DVDDM rising	0	-	100	ms
t3	Sensor reset time	8	-	-	MCLK
t4	From AVDD & DVDDM falling to DVDD falling	0	-	-	ms
t5	From DVDD falling to HVDD falling	0	-	-	ms

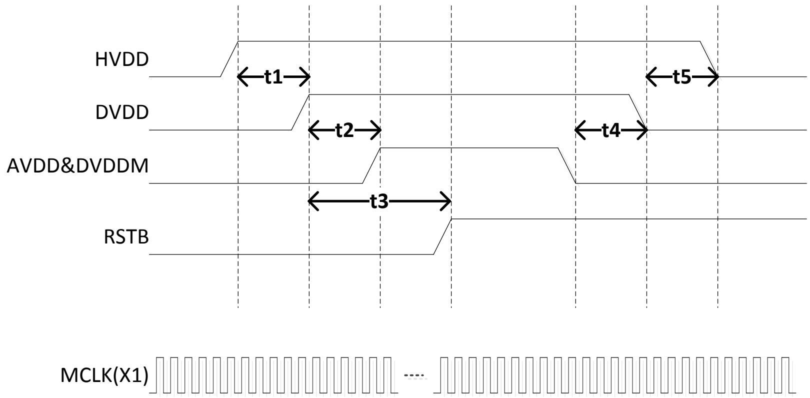


Figure 12 Timing diagram of power-on/off sequence

Clock

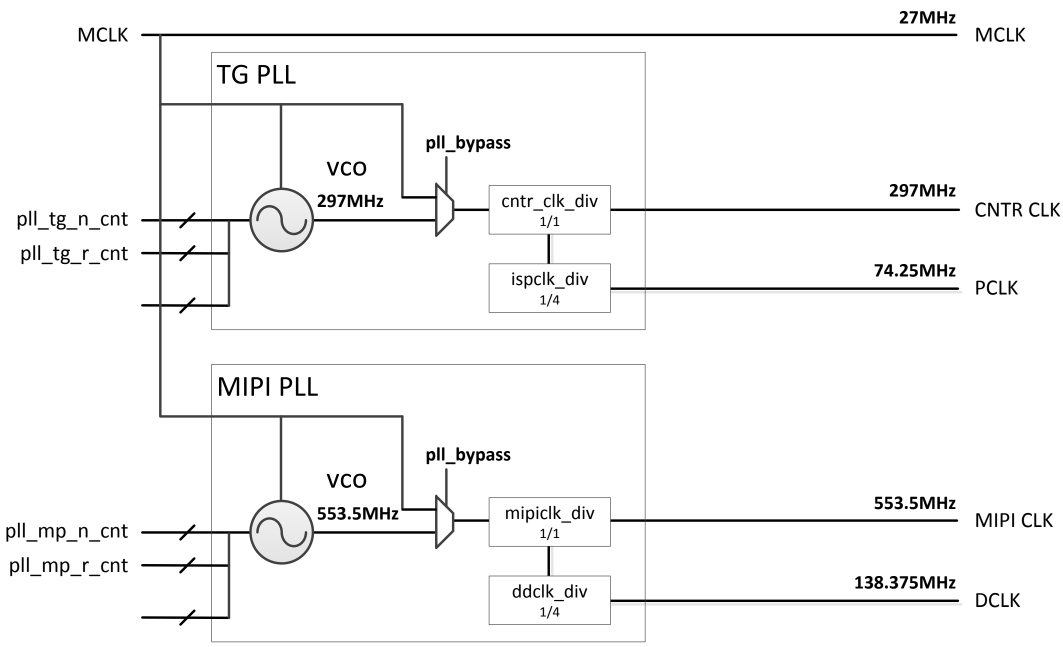


Figure 13 Clock divider

- MCLK : PLL input clock
- VCO : PLL output clock
- CNTR CLK : Clock for Counter
- PCLK : The counter values increase at the pace of pclk.
- MIPI CLK : Clock for MIPI
- DCLK : Clock for formatter

PLL

- Frequency of MCLK(PLL input clock) should be MCLK > 3.375MHz.
- Frequency of VCO(PLL output clock) should be 120MHz $\leq$ VCO $\leq$ 606MHz.

```
VCO = MCLK x pll_n_cnt/pll_r_cnt
```

- T_{Lock}(PLL Lock time) should be T_{Lock} > 20us.

Table 11 Register Table - PLL

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pll_bypass	A	4E	[4]	1'b1	RW		PLL bypass

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b0 : use pll mode 1'b1 : pll bypass mode
plltg_pd	A	4E	[5]	1'b1	RW		PLL1 power down mode 1'b0 : pll1 power on 1'b1 : pll1 power down
pll_tg_n_cnt	A	51	[7:0]	0x2C	RW		TG PLL multiplication factor
pll_tg_r_cnt	A	52	[4:0]	0x04	RW		TG PLL division factor
pllmp_pd	A	4E	[3]	1'b1	RW		PLL2 power down mode 1'b0 : pll2 power on 1'b1 : pll2 power down
pll_mp_n_cnt	A	53	[7:0]	0x2C	RW		MIPI PLL multiplication factor
pll_mp_r_cnt	A	54	[4:0]	0x04	RW		MIPI PLL division factor

Clock Divider

Table 12 Register Table - Clock divider

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
clkoff	A	23	[3]	1'b0	RW		Clock pad kill enable 1'b0 : disable (not kill) 1'b1 : enable (kill)
adcclk_div	A	56	[7:6]	2'b00	RW	aev	ADC clock divider isp_clk =vco1/(2^adcclk_div)
ispclk_div	A	56	[5:4]	2'b10	RW	aev	ISP clock divider isp_clk =vco1/(2^ispclk_div)
mipiclk_div	A	57	[7:6]	2'b01	RW	aev	MIPI clock divider mipi_clk =vco2/(2^mipiclk_div)
ddclk_div	A	57	[4:3]	2'b10	RW	aev	MIPI byte clock divider ddclk =vco2/(2^ddclk_div)
isp_clk_en	A	58	[7]	1'b1	RW	aev	isp clock enable
tm_clk_en	A	58	[6]	1'b1	RW	aev	tone map clock enable

PLL and Clock Setting Sequence

- When using PLL, set-up sequence shown in Figure 14 is necessary.
- I2C update timing register, i2c_control_1, is changed before setting clock dividers to immediately apply clock divider settings.

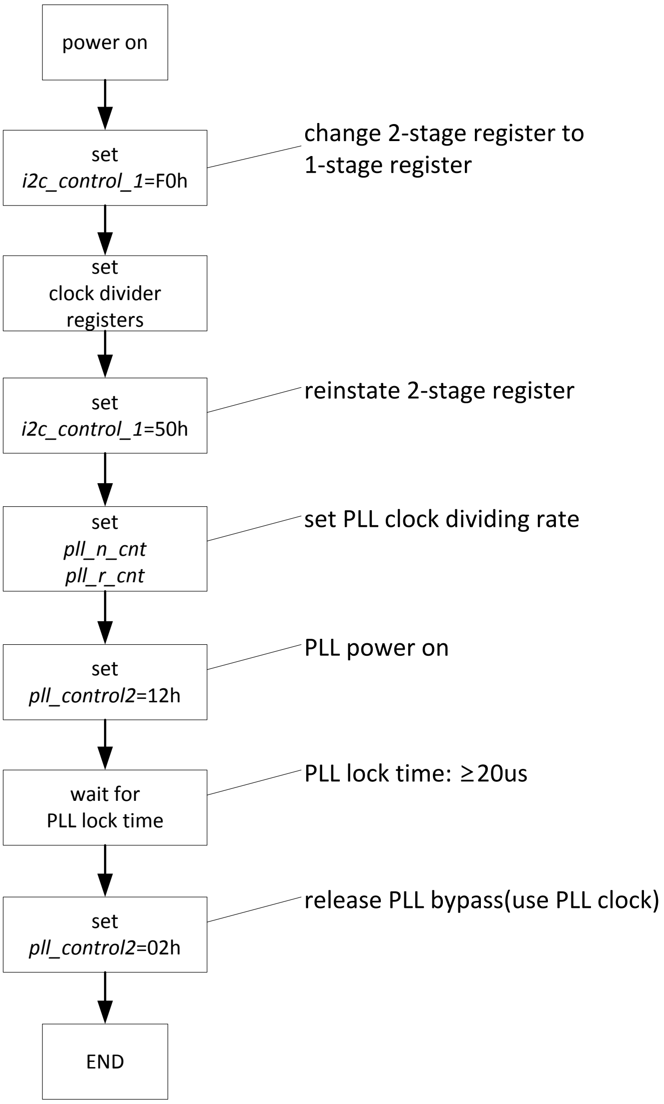


Figure 14 Clock setting sequence

STDBY Mode

The PK5210N provides hardware standby. Hardware standby mode is controlled by PWRDN PAD. I2C communication cannot be used while hardware standby mode is set.

Table 13 Register Table - STDBY mode

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
stdby_level	A	23	[5:4]	2'b10	RW		Output data pad stdby level selector 2'b00 : low 2'b01 : high 2'b1x : hiz

System Reset

The PK5210N has two methods to reset: hard reset and soft reset. Hard reset signal from RSTB PAD must remain low (active low) for at least 8 master clocks to correctly reset the sensor. All registers are set to their default values after reset.
Figure 15 shows device soft reset by setting softreset register through I2C interface. When softreset register is set, async_rstb (asynchronous reset) and sync_rstb signal changes from 1 to 0 and holds for 1 clock of SCL. Afterward, async_rstb is set back to 1 while sync_rstb holds 0 for another 16 clocks of pclk for stable reset operation. Therefore, PK5210N requires at least 1 clock of SCL and 16 clocks of pclk to perform a soft reset operation.

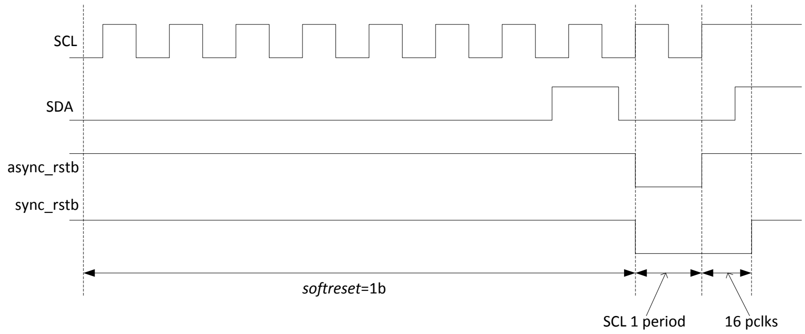


Figure 15 Soft reset

Table 14 Register Table - Soft reset

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
softreset	A	20	[0]	0x00	RW		Soft reset 1'b0 : disable 1'b1 : enable (after succesful reset value reverts to 0)

I2C Interface

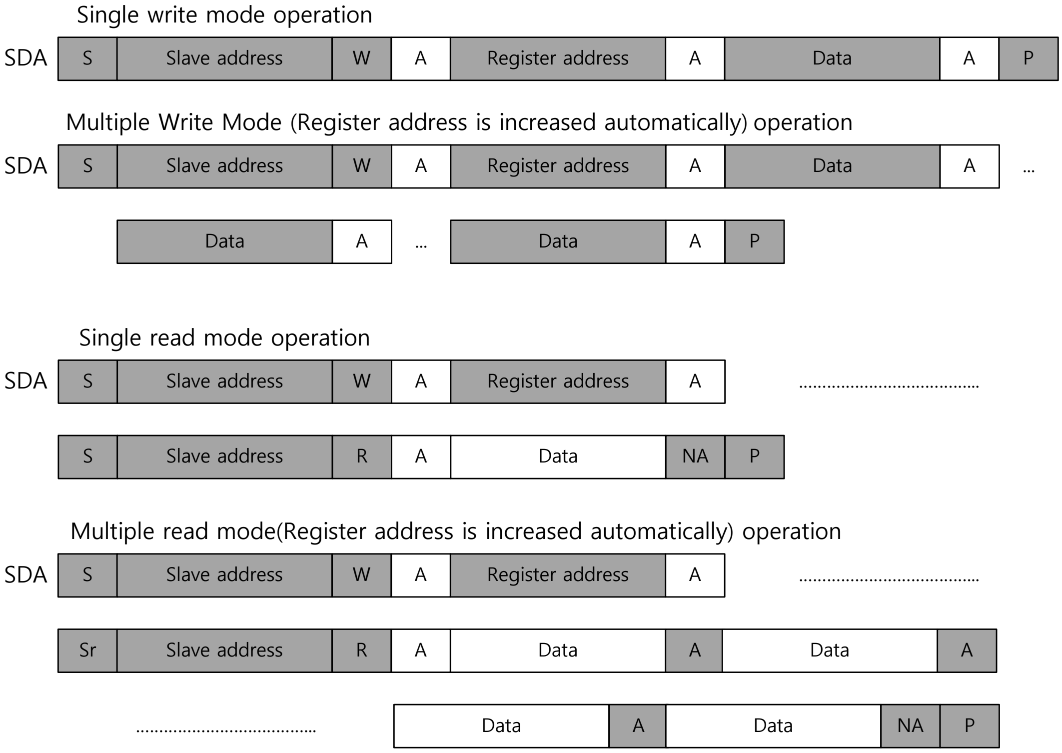
I2C Communication

I2C communication is a serial interface which utilizes SCL/SDA lines to transfer 8-bit data per transaction. PK5210N includes only I2C slave function and requires external master to access the internal registers. Each transaction requires 8-bit data and 1-bit acknowledge bit. There are four types of operations supported in PK5210N's I2C operation: single write, multiple write, single read, multiple read.

In single write operation, after the start state, 7-bit slave address and write bit are transmitted from master device to PK5210N. If correct slave address is detected, PK5210N reply with acknowledge bit as confirmation of valid address. Then master device transmits register address and waits for acknowledge bit from PK5210N. Lastly, 8-bit data is sent to PK5210N and waits for acknowledge bit again. Once acknowledge bit is recieved, master device announces the stop state to terminate I2C communication.

Multiple write operation works exactly the same until stop state procedure. Instead of announcing the stop state, master device transmits more data. If PK5210N detects multiple write operation, any data stream following the first 8-bit is stored in subsequent register addresses of the first register address.

Read operation consists of two sub-procedure: address write and data read. The procedure is performed exactly same as register address write procedure from single write operation. Afterward, master device announces repeated start and transmit slave address with read bit. When PK5210N detects read operation, PK5210N sends acknowledge bit to master device, then reads register corresponding to register address. PK5210N transmits read data to master device and waits for master device to respond. If master device responds with no acknowledge bit followed by stop state, read operation is terminated. On the other hand, if master device responds with acknowledge, PK5210N reads the subsequent register and transmits again. As long as master device replies with acknowledge bit after each data transaction, PK5210N will continuously read the subsequent register and transmit until no acknowledge bit followed by stop state is presented. If only one 8-bit data is read, the procedure is single read operation. whereas, reading more than 8-bit data is multiple read operation. Figure 16 shows read/write operation of I2C communication.



Slave address can be extended 74h to 77h by CADDR0_PAD / CADDR1_PAD

CADDR1_PAD	1'b0	1'b0	1'b1	1'b1
CADDR0_PAD	1'b0	1'b1	1'b0	1'b1
slave address	74h	75h	76h	77h
write address	E8h	EAh	ECh	EEh
read address	E9h	EBh	EDh	EFh

R/W : Read/Write selection, High = read / Low = write
A : Acknowledge bit, NA : No Acknowledge, DATA : 8-bit data. P : Stop condition
S : Start condition, Sr : Repeated start(start without preceding stop)

Figure 16 I2C functional description

Register Update Timing

Registers has three different types of update timing: "aev" and "autov" update, regular update. Registers with "aev" and "autov" update type update new values from I2C write operation at the last line of the frame. Whereas, registers with regular update type apply new values immediately after I2C write operation. However, By changing updatecontrol register value, register updates for "aev" and "autov" type can either be disabled or be updated immediately.

"m_wr" update registers only updates MPU genlock related registers. When "m_wr" is set, MPU genlock related registers value are updated and applied to the system in the next frame.

"wr_en" update registers only applies to exposure related registers (integration time, global gain, digital gain). Due to exposure controls being split across several registers which leads to unreliable exposure updates if updated one by one, all exposure related registers' update timing is control by reg_wr_en register. When reg_wr_en register is set, "wr_en" update registers are updated simultaneously.

Table 15 shows registers relevant to register update control.

Table 15 I2C update timing control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
updatecontrol	A	1A	[7:4]	4'b0101	RW		Control I2C register with autov, aev update type LSB 2-bit updatecontrol[1:0] controls aev update and MSB 2-bit updatecontrol[3:2] controls autov update 2'b00 : no update 2'b01 : aev update 2'b1x : immediate aev update
wr_en	B	8D	[0]	0x00	RW		Update exposure related register 1'b0 : no update 1'b1 : wr_en set
wr_en_off	B	8E	[0]	0x00	RW		Update exposure related register 1'b0 : update @ wr_en = 1'b1 1'b1 : Immediately update
mpu_gen_write	B	59	[0]	0x0	RW		Genlock I2C register update

Initialization Timing for I2C interface

Register control through I2C communication is possible at the point where 16 pclk has passed after RSTB becomes high (refer to Figure 17).

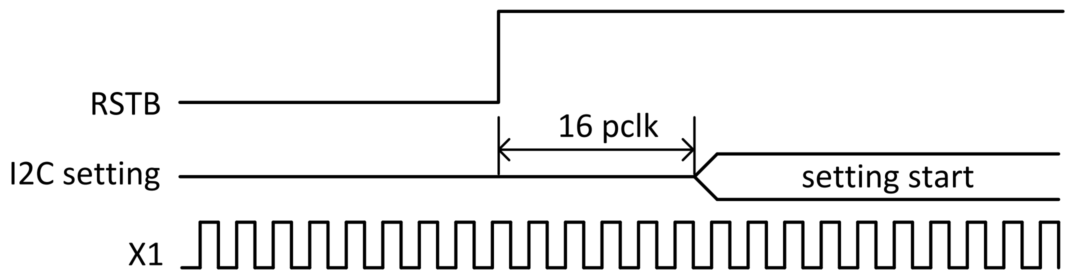


Figure 17 Available timing for I2C communication after system reset.

Exposure Control

Integration Time

PK5210N employs rolling shutter [1] for capturing image. Reset operation initializes ROBP and active pixel region in sequence row by row. Readout process reads pixel data stored in photodetector at the identical order and speed as reset operation. The difference in time between reset and readout operation is known as integration time (refer to Figure 18). Integration time controls photodetector's level of exposure to light. Integration time can be adjusted in line unit level (line inttime) and column unit level (column inttime). Under the assumption of fixed frame structure, the maximum line inttime is "frame height - 5" and column inttime is "frame width - 1". Upper 16 bits of inttime register represent number of lines for line inttime and lower 8 bits of inttime register represent number of column inttime, where number of column changes in framewidth/256 increment.

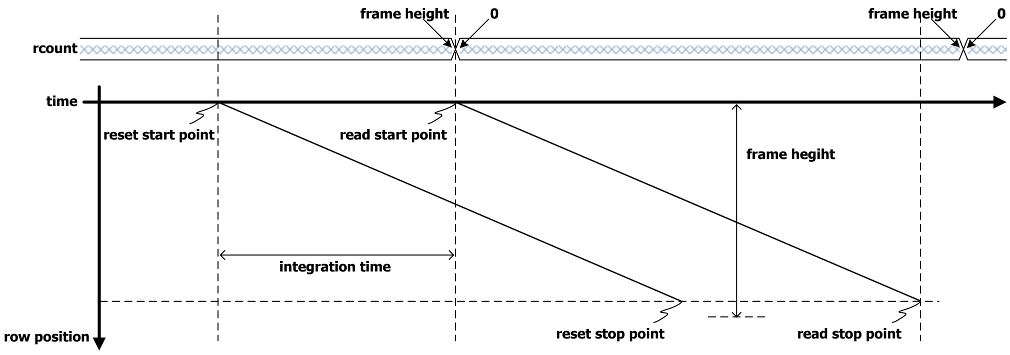


Figure 18 Fundamental concept of integration time

Table 16 shows registers relevant to integration time.

Table 16 Register Table - Integration time

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
inttime_h	B	6E	[7:0]	0x01	RW	wr_en	Integration time 0 (line) High Byte
inttime_m	B	6F	[7:0]	0x40	RW	wr_en	Integration time 0 (line) Low Byte
inttime_l	B	70	[7:0]	0x00	RW	wr_en	Iinteration time 0 (column)
inttime_vs_h	B	71	[7:0]	0x00	RW	wr_en	Integration time 1 (line) High Byte
inttime_vs_m	B	72	[7:0]	0x02	RW	wr_en	Integration time 1 (line) Low Byte
inttime_vs_l	B	73	[7:0]	0x00	RW	wr_en	Iinteration time 1 (column)
frmvar_en	B	04	[7]	1'b0	RW	aev	Variable frame enable 1'b0 : disable 1'b1 : enable

[1] Image capture method in which each frame is scanned row by row instead of capturing entire frame at once

Global Gain

Global gain affects analog gain level of comparators, which determines Bayer data values. In PK5210N, global gain is ranged from 0x00 to 0x6F.

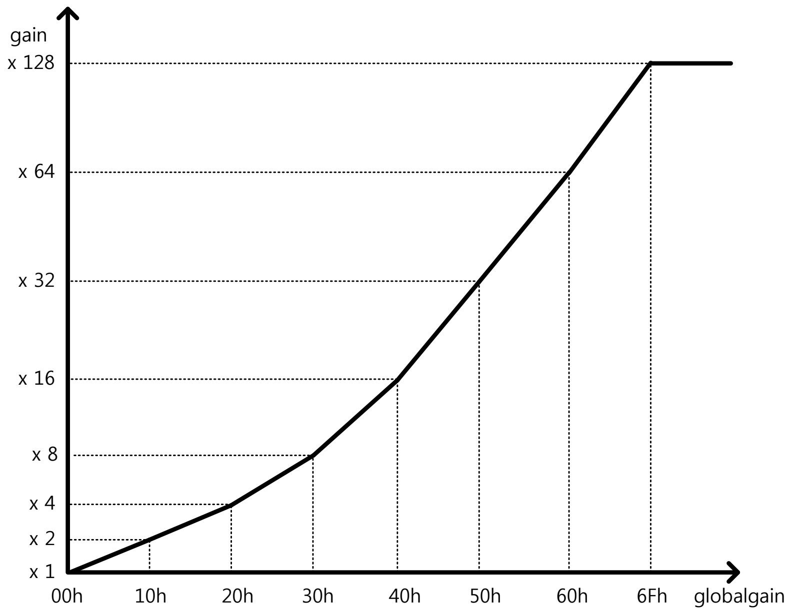


Figure 19 Globalgain's gain

Table 17 shows registers relevant to global gain.

Table 17 Register Table - Global Gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
globalgain	B	74	[7:0]	0x00	RW	wr_en	Analog gain

Digital Gain

Analog signal is converted to digital value through ADC operation, and the digital value can be amplified by digital gain. digitalgain register's upper 4 bits are positive integer and lower 4 bits are fraction.

Table 18 shows registers relevant to digital gain

Table 18 Register Table - Digital gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
digitalgain_l	B	75	[7:0]	0x10	RW	wr_en	Digital gain of long data
digitalgain_s	B	76	[7:0]	0x10	RW	wr_en	Digital gain of short data
digitalgain_vs	B	77	[7:0]	0x10	RW	wr_en	Digital gain of very short data

Exposure factor update control

If the exposure factor is changed over several frames, the brightness of the screen changes for each frame, which causes hunting. Therefore, exposure related registers are updated at once and the brightness of the screen is not changed many times.

- If wr_en = 1'b1, exposure register is updated. and then wr_en = 1'b0.
- If wr_en_off = 1'b1, wr_en is disabled.

Table 19 shows registers relevant to exposure register update

Table 19 Register Table - Exposure register update

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
wr_en	B	8D	[0]	0x00	RW		Update exposure related register 1'b0 : no update 1'b1 : wr_en set
wr_en_off	B	8E	[0]	0x00	RW		Update exposure related register 1'b0 : update @ wr_en = 1'b1 1'b1 : Immediately update

Genlock

Genlock Configuration

Generator locking (genlock) synchronizes internal synchronous timing of master and slave. The PK5210N includes genlock sync method to achieve genlock.

- Genlock Sync Method
  Master device generates reference synchronous signal, which outputs via GENLOCK pad. Slave device receives the reference synchronous signal via its GENLOCK pad to achieve genlock. Figure 20 shows example of genlock sync set-up for using external MPU as master, whereas Figure 21 uses the PK5210N as master.

  – GENLOCK signal
    Slave device requires at least 4 pclk width of the reference synchronous signal for reliable genlock operation (refer to Figure 22). If the PK5210N is the master device, the signal width can be adjusted by changing genlock_width register.

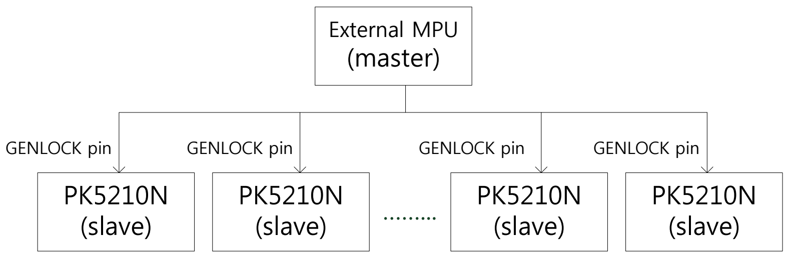


Figure 20 Genlock Sync configuration with external MPU

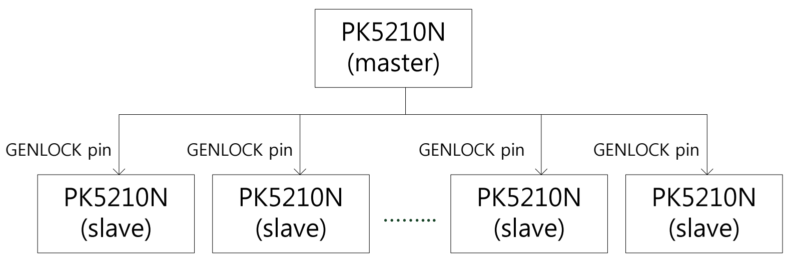


Figure 21 Genlock Sync configuration with another the PK5210N

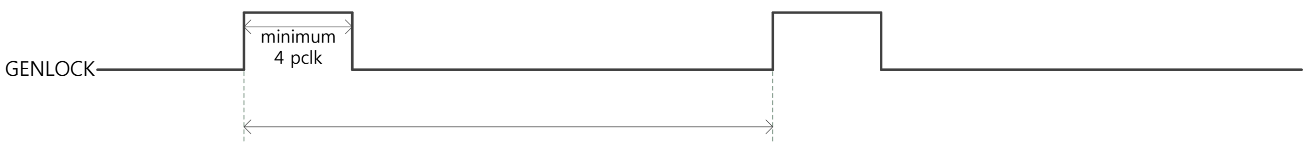


Figure 22 GENLOCK reference signal waveform

Genlock Sync Method

- Genlock Master Mode (genlock_master = 1’b1)

In the case of the PK5210N acting as the master device, if internal rcount and ccount value are equal to rcount_genlock and ccount_genlock respectively, master device outputs the reference synchronous signal via GENLOCK pad and the signal remains high for genlock_width * pclk.

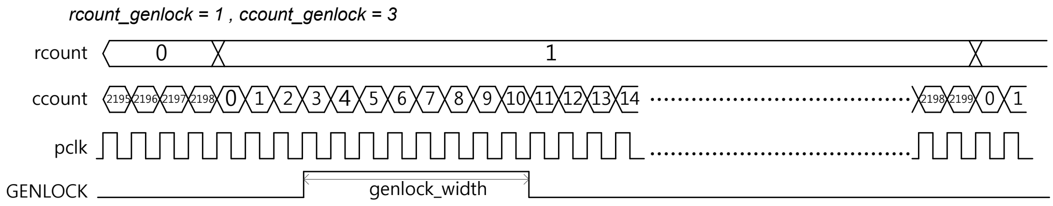


Figure 23 Example of timing diagram @master mode

- Genlock Slave Mode (genlock_master = 1’b0)
  In the case of the PK5210N acting as the slave device, if the slave device receives reference synchronous signal from master device via GENLOCK pad, internal rcount and ccount are initialized to rcount_genlock and (ccount_genlock + 1) respectively at rising edge of the signal.

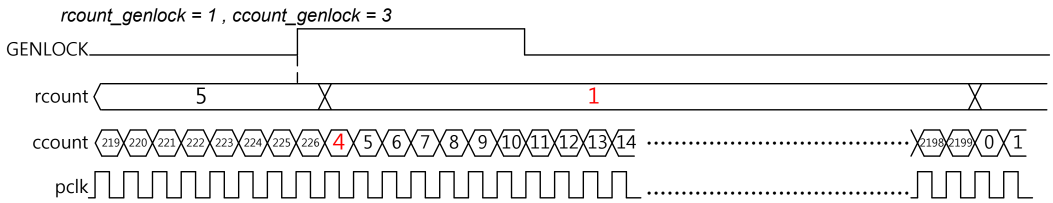


Figure 24 Example of timing diagram @slave mode

Note If the synchronization timing difference between master and slave is large, sudden shift in brightness may occur in slave device's image.

Figure 25 shows timing diagram of genlock sync method with the PK5210N as master device.

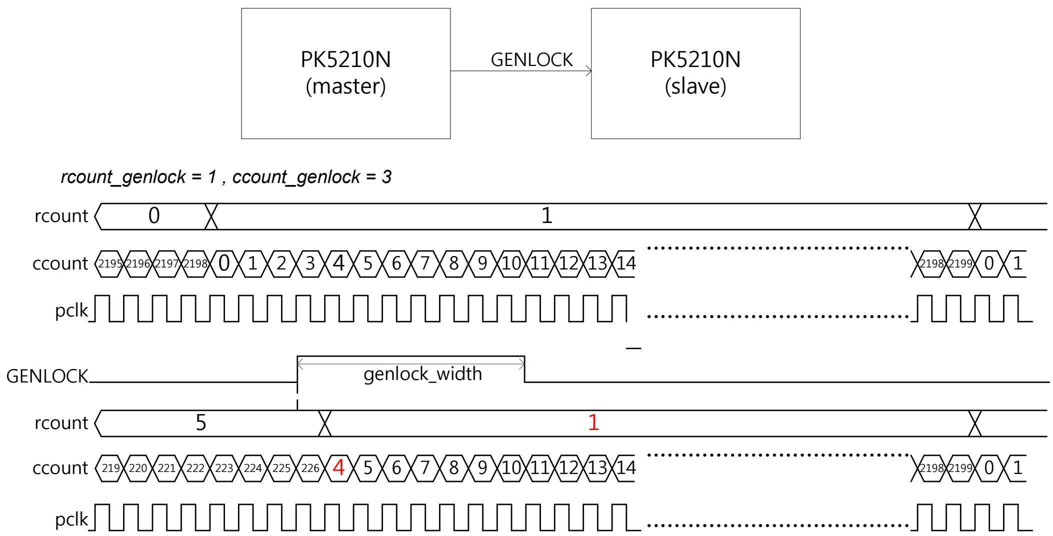


Figure 25 Example of timing diagram @genlock sync mode

Table 20 shows registers relevant to genlock sync method.

Table 20 Register Table - genlock sync mode

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
genlock_pad_en	A	25	[0]	1'b0	RW		GENLOCK pad enable 1'b0 : disable 1'b1 : enable
genlock_en	B	0A	[5]	1'b0	RW		GENLOCK enable 1'b0 : disable 1'b1 : enable
genlock_master	B	0A	[4]	1'b0	RW		GENLOCK master 1'b0 : slave 1'b1 : master
rcount_genlock_h	B	50	[4:0]	0x00	RW		Genlock row count High Byte
rcount_genlock_l	B	51	[7:0]	0x01	RW		Genlock row count Low Byte
ccount_genlock_h	B	52	[4:0]	0x00	RW		Genlock column count High Byte
ccount_genlock_l	B	53	[7:0]	0x01	RW		Genlock column count Low Byte
genlock_width	B	54	[7:0]	0x10	RW		Genlock pulse width

Test Pattern (TP) Control

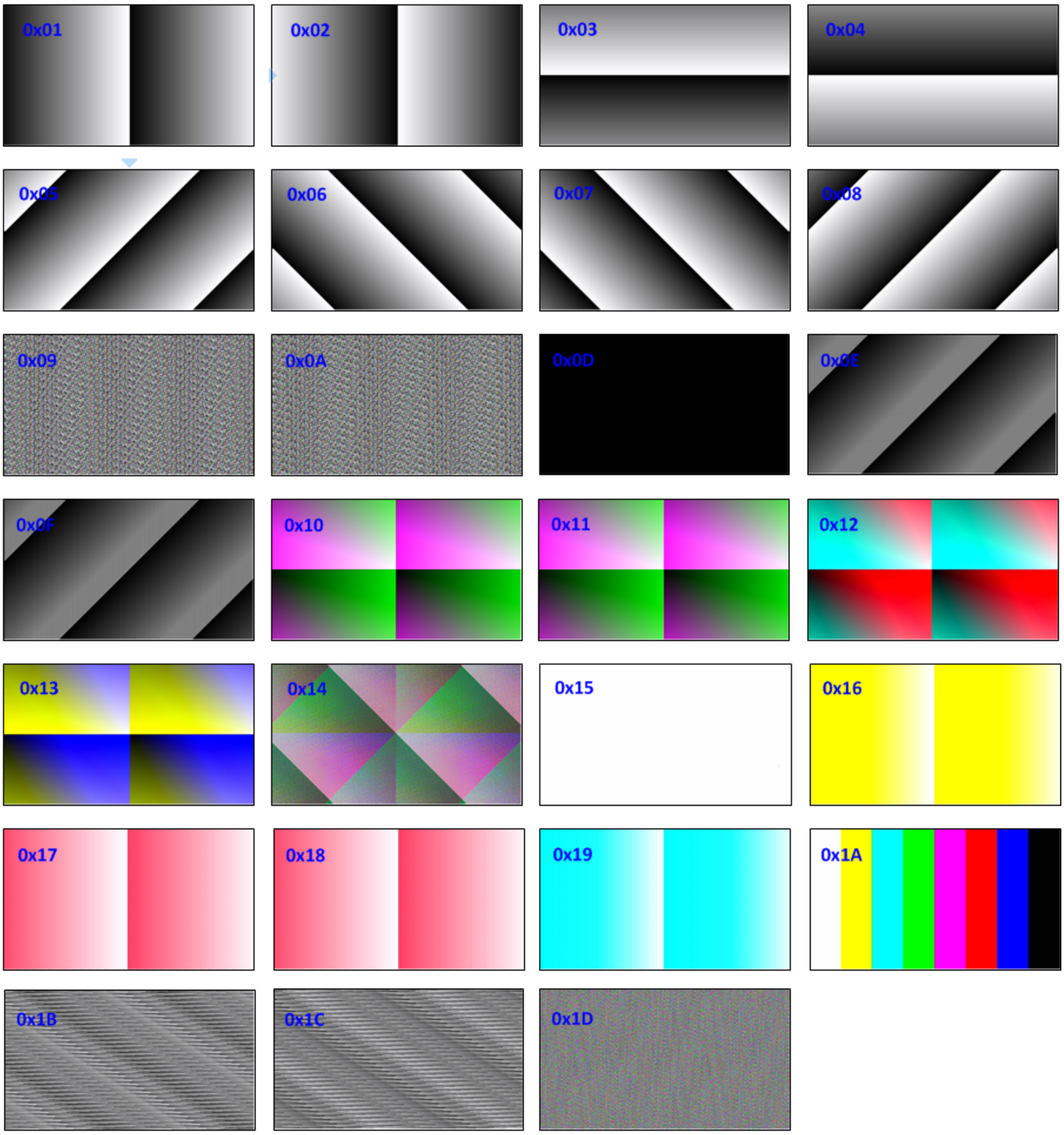
TP control generates test images from ISP block. Test images type can be selected by setting tp_ctrl_0 registers. In case of test image types from 0x15 to 0x1A values for tp_ctrl_0, tp_ctrl_1/2/3/4 registers are used as color values and the following rule shows how the color value is determined:

- R : {tp_ctrl_1_h, tp_ctrl_1_l[1:0]}
- Gr : {tp_ctrl_2_h, tp_ctrl_2_l[1:0]}
- Gb : {tp_ctrl_3_h, tp_ctrl_3_l[1:0]}
- B : {tp_ctrl_4_h, tp_ctrl_4_l[1:0]}

Table 21 shows registers relevant to Test Pattern ctrl

Table 21 Register Table - Test pattern ctrl

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
tp_seq	B	11	[4:3]	2'b00	RW		Test pattern block input sequence selection
tp_seq_vs	B	11	[2:1]	2'b00	RW		Test pattern block input sequence selection for very short
tp_control_0	B	BC	[7:0]	0x00	RW		Test pattern selection
tp_control_1_h	B	BD	[7:0]	0x00	RW		R color for test pattern High Byte
tp_control_1_l	B	BE	[7:0]	0x00	RW		R color for test pattern Low Byte
tp_control_2_h	B	BF	[7:0]	0x00	RW		G1 color for test pattern High Byte
tp_control_2_l	B	C0	[7:0]	0x00	RW		G1 color for test pattern Low Byte
tp_control_3_h	B	C1	[7:0]	0x00	RW		G2 color for test pattern High Byte
tp_control_3_l	B	C2	[7:0]	0x00	RW		G2 color for test pattern Low Byte
tp_control_4_h	B	C3	[7:0]	0x00	RW		B color for test pattern High Byte
tp_control_4_l	B	C4	[7:0]	0x00	RW		B color for test pattern Low Byte
tp_width_h	B	C5	[2:0]	0x07	RW		Test pattern width for color bar pattern High Byte
tp_width_l	B	C6	[7:0]	0xA8	RW		Test pattern width for color bar pattern Low Byte



tp_control_1, tp_control_2, tp_control_3, tp_control_4 = 0xFF

Figure 26 Test image

ISP

The ISP combines three images (long, short, and very-short) to create one WDR image. Then, the WDR image is tone mapped and output as an SDR image. The process from input to output includes features to improve image quality.

Figure 27 is shown the ISP data flow

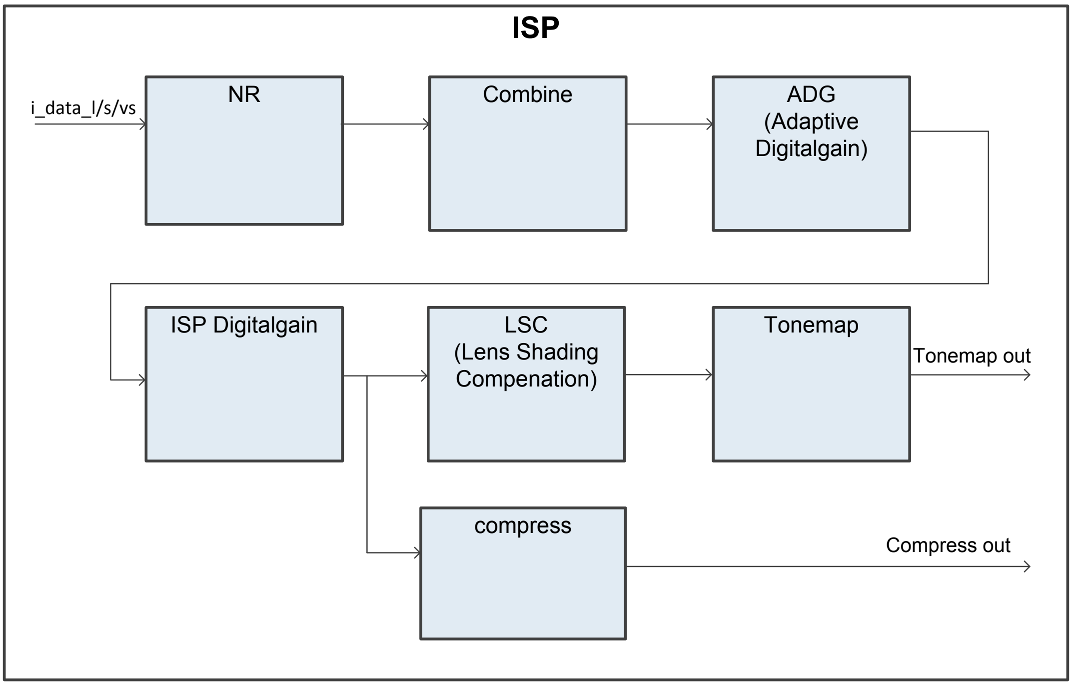


Figure 27 ISP Data flow

Noise Reduction (NR)

NR controls long, short and very-short images respectively. It is enabled when nr_en_l, nr_en_s, and nr_en_vs are set to 1'b1 respectively. The NR intensity is adjusted according to the nr_ratio setting. The larger the nr_ratio value (Max:FFh) is used, the NR effect decreases.

Table 22 Register Table - NR

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
nr_en_l	G	06	[7]	1'b0	RW	aev	NR enable (long) 1'b0 : disable 1'b1 : enable
nr_en_s	G	06	[6]	1'b0	RW	aev	NR enable (short) 1'b0 : disable 1'b1 : enable
nr_en_vs	G	06	[5]	1'b0	RW	aev	NR enable (very-short) 1'b0 : disable 1'b1 : enable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
nr_ratio_l	G	37	[7:0]	0x08	RW	aev	NR strength control (long)
nr_ratio_s	G	3A	[7:0]	0x08	RW	aev	NR strength control (short)
nr_ratio_vs	G	3D	[7:0]	0x08	RW	aev	NR strength control (very-short)

Adaptive Digital Gain (ADG)

ADG is a function to apply digital gain for each pixel differently. The gain value can be adjusted by setting ADG_ratio[3:0]. In ADG_ratio [3: 0] $\leq$ 2h, there is no effect, and in 3h $\leq$ bin_ratio [3: 0] $\leq$ Ch, x0.5 gain increases with each increment.

Table 23 Register Table - ADG

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
ADG_ratio	I	BD	[7:0]	0x08	RW	aev	ADG ratio (02h = x1)

ISP Digital gain

ISP digital gain function is enabled by setting isp_dgain_en to 1'b1. digitalgain can be adjusted by setting d gain_isp.

Table 24 Register Table - ISP digital gain

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
isp_dgain_en	G	06	[0]	1'b0	RW	aev	ISP digitalgain enable 1'b0 : disable 1'b1 : enable
dgain_isp	I	88	[7:0]	0x00	RW	aev	ISP digitalgain (10h = x1, … , FFh = x15.9735)

Compress

Compress makes the WDR image into a 12 bits image. Compress is processed in PWL (Piece-Wise Linear) method with 4 knee points as shown in Figure 28.

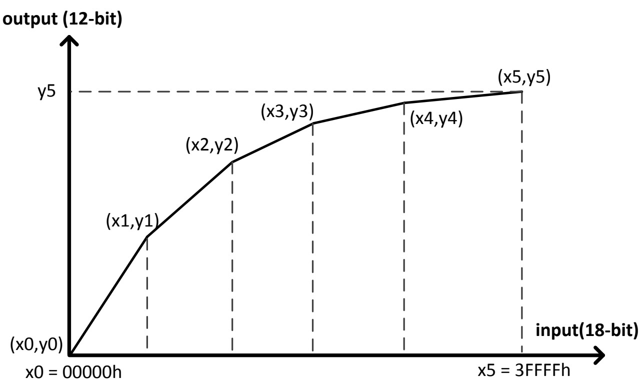


Figure 28 Compress

Table 25 Register Table - Compress

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
cmp_x1_h	G	B5	[1:0]	0x00	RW	aev	Explanatory variable point 1 for compress
cmp_x1_m	G	B6	[7:0]	0x40	RW	aev	Explanatory variable point 1 for compress
cmp_x1_l	G	B7	[7:0]	0x00	RW	aev	Explanatory variable point 1 for compress
cmp_x2_h	G	B8	[1:0]	0x00	RW	aev	Explanatory variable point 2 for compress
cmp_x2_m	G	B9	[7:0]	0x80	RW	aev	Explanatory variable point 2 for compress
cmp_x2_l	G	BA	[7:0]	0x00	RW	aev	Explanatory variable point 2 for compress
cmp_x3_h	G	BB	[1:0]	0x01	RW	aev	Explanatory variable point 3 for compress
cmp_x3_m	G	BC	[7:0]	0x00	RW	aev	Explanatory variable point 3 for compress
cmp_x3_l	G	BD	[7:0]	0x00	RW	aev	Explanatory variable point 3 for compress
cmp_x4_h	G	BE	[1:0]	0x02	RW	aev	Explanatory variable point 4 for compress
cmp_x4_m	G	BF	[7:0]	0x00	RW	aev	Explanatory variable point 4 for compress
cmp_x4_l	G	C0	[7:0]	0x00	RW	aev	Explanatory variable point 4 for compress
cmp_y0_h	G	C1	[3:0]	0x00	RW	aev	Dependent variable point 0 for compress
cmp_y0_l	G	C2	[7:0]	0x00	RW	aev	Dependent variable point 0 for compress
cmp_y1_h	G	C3	[3:0]	0x04	RW	aev	Dependent variable point 1 for compress
cmp_y1_l	G	C4	[7:0]	0x00	RW	aev	Dependent variable point 1 for compress
cmp_y2_h	G	C5	[3:0]	0x06	RW	aev	Dependent variable point 2 for compress
cmp_y2_l	G	C6	[7:0]	0x00	RW	aev	Dependent variable point 2 for compress
cmp_y3_h	G	C7	[3:0]	0x08	RW	aev	Dependent variable point 3 for compress
cmp_y3_l	G	C8	[7:0]	0x80	RW	aev	Dependent variable point 3 for compress
cmp_y4_h	G	C9	[3:0]	0x0C	RW	aev	Dependent variable point 4 for compress
cmp_y4_l	G	CA	[7:0]	0x00	RW	aev	Dependent variable point 4 for compress
cmp_y5_h	G	CB	[3:0]	0x0F	RW	aev	Dependent variable point 5 for compress
cmp_y5_l	G	CC	[7:0]	0xFF	RW	aev	Dependent variable point 5 for compress

Lens Shading Compensation (LSC)

LSC is a function to correct the darkening of the position away from the center of the image due to lens shading. LSC function control elements are LSC center and LSC scale, and the description of each is as follows.

- LSC center
  As shown in Figure 29, adjust LSC center with lens_x and lens_y settings. It is used when the center of the lens and the center of the image sensor do not match.

- LSC scale
  As shown in Figure 30, set the lens_scale to adjust the gain according to the distance from the LSC center. The larger the lens_scale value, the greater the LSC effect.

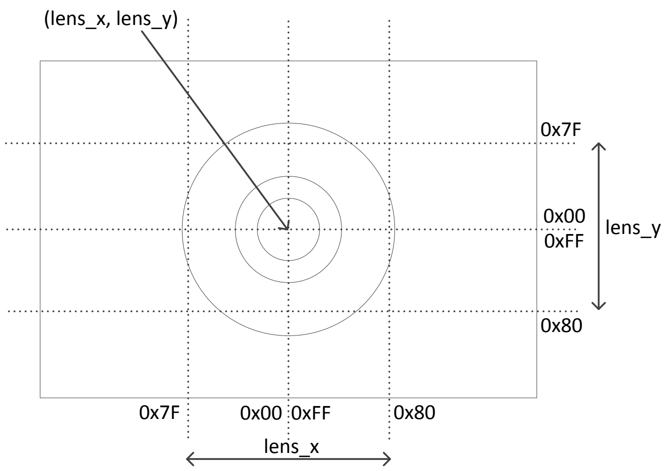


Figure 29 LSC center control

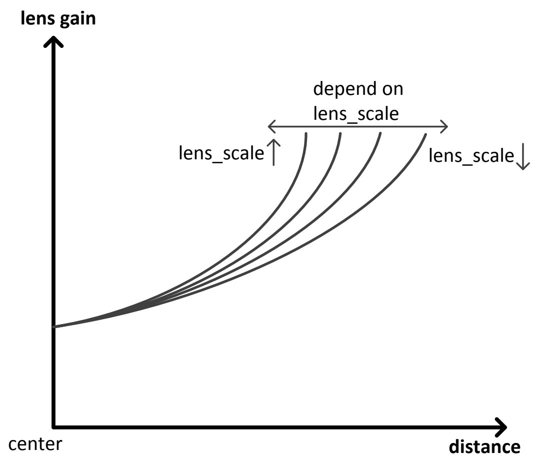


Figure 30 LSC gain fitting with LSC center and LSC scale

Table 26 Register Table - LSC

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
lens_en	H	04	[6]	1'b0	RW	aev	Lens shading compensation enable 1'b0 : disable 1'b1 : enable
lens_scale	H	80	[7:0]	0x80	RW	aev	LSC scale control
lens_x	H	81	[7:0]	0x00	RW	aev	LSC center control
lens_y	H	82	[7:0]	0x00	RW	aev	LSC center control

WDR (Wide Dynamic Range) Tonemap

Tone mapping is the process of compressing wide dynamic rage data into a low dynamic range data. Tone mapping function basically works on luminance component of input data. In order to preserve color and details which is inherently contained in input data, tone mapped luminance is transformed to bayer format data again, taking into account the color and details in the post processing stage as following Figure 31. Tone mapping is enabled by setting tm_en register (tm_en=1). When tm_en is cleared, (tm_en=0), lower 12-bit out of 20-bit input data goes out of the tonemap function block.

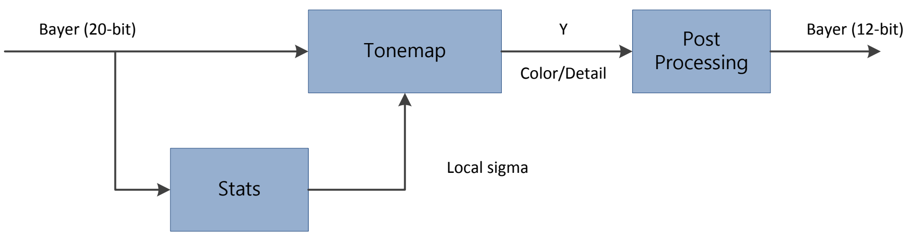


Figure 31 The post processing stage

PK5210N supports local tone mapping algorithm. Local tone mapping uses spatially varying local sigma (average brightness of the local region), which allows the local contrast and the visibility of details of the image to be much more increased than global tone mapping algorithm. Local tone mapping algorithm controls the tone mapping curve depending on the local sigma. If the local sigma is larger, then tone mapped image is darker, on the other hand, if the local sigma is smaller, tone mapped image is brighter. Tuning of local tonemap is executed by adjusting the local sigma as following order.

- Local sigma contrast
  Local sigma contrast: Local sigma which is measured on the input image is divided into two sections, dark and bright section. Based on the two sections, local sigma and contrast can be further adjusted by the slope of each section as follow in Figure 32. The decision threshold for two section is global sigma (global average brightness). If the dark section slope is increased, tone mapped dark region becomes brighter, and if the bright section slope is increased, bright region of tone mapped image becomes more dark. The bright section slope is controlled by con_sl_a register and con_sl_b register is used for dark section slope tuning.

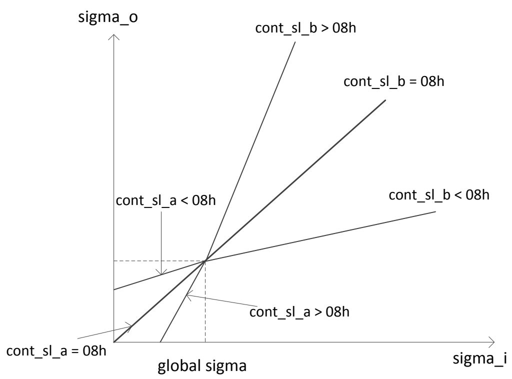


Figure 32 The sigma contrast

- Local sigma gain
  Local sigma gain is used to control the overall brightness of the tone mapped image. It is applied to the local sigma which is adjusted by local sigma contrast. If the local sigma gain is greater than 1.0, overall

brightness of the output image becomes darker, less than 1.0 local sigma gain makes tone mapped image brighter. Local sigma gain is controlled by loc_sgain_c register.

- Local sigma minimum
  If the local sigma adjusted by local sigma contrast and gain is too small, dark region contrast might be lowered. The contrast of dark region can be improved by setting the minimum local sigma value to log_sig_min register.

- Local sigma weighting
  Global tone mapping algorithm employs a single tone curve for all pixels of the image. If the global sigma is applied to all pixels instead of local sigma, local tone mapping has the same effect as a global tone mapping. Global and local tone mapping can be mixed up by setting weight value of local sigma to loc_locsig_ratio register. The weight value for local sigma ranges from 0 to 1.0.
  Y component which is tone mapped by local sigma adjustment is merged with color and details comprised in the input 20-bit WDR data, and goes out as the final 12-bit tone mapped output.

- Color saturation control
  Tone mapping function may result in some color artifacts especially in color saturation region. These color saturation can be preserved or enhanced by applying proper color gain to the wdr_cgain register during the tone mapping process.

- Detail enhancement
  Detail information is extracted during tone mapping process and used for enhancing the local contrast of tone mapped output. Detail enhancement is controlled by the value of detail gain register, wdr_dgain register.

Image sensor noise normally depends on the sensor exposure conditions (integration time, analog/digital gain) and these input noises induced by sensor itself can be enlarged during the tone mapping process. In order to be able to control noise amplification properly, some tone mapping registers (loc_sgain_c, loc_sig_min, wdr_cgain, wdr_dgain) have 6 registers for each, which allows the noise to be more adaptive to the exposure measured in the environment.

Table 27 Register Table - WDR Tonemap

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
tm_en	H	04	[4]	1'b0	RW	aev	Tonemap enable 1'b0 : disable 1'b1 : enable
con_sl_a	H	58	[7:0]	0x08	RW	aev	dark region slope for local tonemap contrast 8'h08 : corresponds to the slope 1.0
con_sl_b1	H	59	[7:0]	0x08	RW	aev	bright region slope for local tonemap contrast con_sl_b=con_sl_b1 * con_sl_b2 8'h40 : corresponds to gain 1.0 for cont_sl_b
con_sl_b2	H	5A	[7:0]	0x08	RW	aev	bright region slope for local tonemap contrast
loc_sgain_c	H	5B	[7:0]	0x00	RO		local sigma gain monitoring register to check the value currently being applied
loc_sgain_c_yref0	H	A8	[7:0]	0x10	RW	aev	local sigma gain for exposure 0 level 8'h10 : corresponds to gain 1.0

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
loc_sgain_c_yref1	H	A9	[7:0]	0x10	RW	aev	local sigma gain for exposure 1 level
loc_sgain_c_yref2	H	AA	[7:0]	0x10	RW	aev	local sigma gain for exposure 2 level
loc_sgain_c_yref3	H	AB	[7:0]	0x10	RW	aev	local sigma gain for exposure 3 level
loc_sgain_c_yref4	H	AC	[7:0]	0x10	RW	aev	local sigma gain for exposure 4 level
loc_sgain_c_yref5	H	AD	[7:0]	0x10	RW	aev	local sigma gain for exposure 5 level
loc_sig_min_c	H	67	[7:0]	0x00	RO		local sigma minimum monitoring register to check the value currently being applied
loc_sig_min_yref0	H	C6	[7:0]	0x00	RW	aev	local sigma minimum for exposure 0 level
loc_sig_min_yref1	H	C7	[7:0]	0x00	RW	aev	local sigma minimum for exposure 1 level
loc_sig_min_yref2	H	C8	[7:0]	0x00	RW	aev	local sigma minimum for exposure 2 level
loc_sig_min_yref3	H	C9	[7:0]	0x00	RW	aev	local sigma minimum for exposure 3 level
loc_sig_min_yref4	H	CA	[7:0]	0x00	RW	aev	local sigma minimum for exposure 4 level
loc_sig_min_yref5	H	CB	[7:0]	0x00	RW	aev	local sigma minimum for exposure 5 level
loc_locsig_ratio	H	65	[4:0]	0x10	RW	aev	local sigma weight 8'h00 : local sigma weight is 0% global sigma weight is 100% 8'h10 : local sigma weight is 100% global sigma weight is 0%
wdr_cgain	H	07	[7:0]	0x40	RO		color gain monitoring register to check the value currently being applied
wdr_cgain_yref0	H	AE	[7:0]	0x40	RW	aev	color gain for exposure 0 level 8'h40 corresponds to gain 1.0
wdr_cgain_yref1	H	AF	[7:0]	0x40	RW	aev	color gain for exposure 1 level
wdr_cgain_yref2	H	B0	[7:0]	0x40	RW	aev	color gain for exposure 2 level
wdr_cgain_yref3	H	B1	[7:0]	0x40	RW	aev	color gain for exposure 3 level
wdr_cgain_yref4	H	B2	[7:0]	0x40	RW	aev	color gain for exposure 4 level
wdr_cgain_yref5	H	B3	[7:0]	0x40	RW	aev	color gain for exposure 5 level
wdr_cgain	H	1B	[7:0]	0x40	RO		detail gain monitoring register to check the value currently being applied
wdr_cgain_yref0	H	B4	[7:0]	0x40	RW	aev	detail gain for exposure 0 level 8'h40 : corresponds to gain 1.0
wdr_cgain_yref1	H	B5	[7:0]	0x40	RW	aev	detail gain for exposure 1 level
wdr_cgain_yref2	H	B6	[7:0]	0x40	RW	aev	detail gain for exposure 2 level
wdr_cgain_yref3	H	B7	[7:0]	0x40	RW	aev	detail gain for exposure 3 level
wdr_cgain_yref4	H	B8	[7:0]	0x40	RW	aev	detail gain for exposure 4 level
wdr_cgain_yref5	H	B9	[7:0]	0x40	RW	aev	detail gain for exposure 5 level

MIPI

Reference For Design

MIPI design in the PK5210N is based on "MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00" and "MIPI Alliance Standard for D-PHY, Version 0.65" specification documents. Output of MIPI consists of one clock lane and two data lanes.

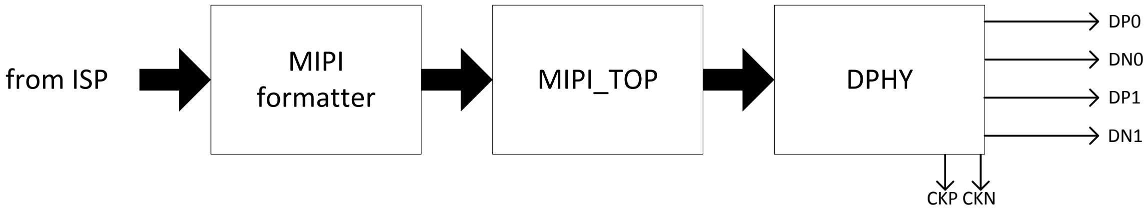


Figure 33 MIPI block diagram

MIPI Clock Relations

Figure 34 shows Clock and MIPI operation. The mipi_clk operates at a frequency four times faster than dclk. In addition, it is used for generating MIPI data and clock lane signal. The dclk is clock rate determined by isp_clk, raw bit, MIPI lane. Table 28 shows clock rate setting.

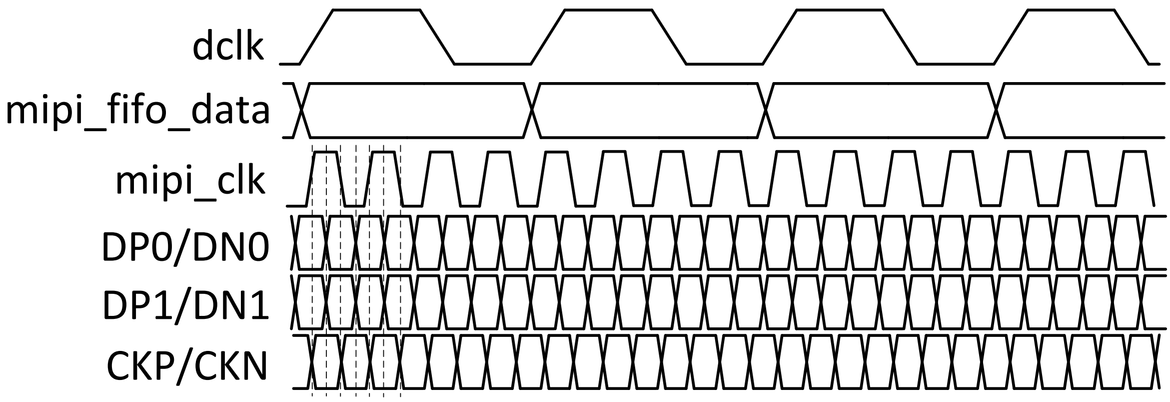


Figure 34 MIPI clock relations diagram

Table 28 MIPI clock with lane and frame rate

FPS	clock domain	MIPI 2 lane raw 12-bit(Mhz)
30fps	pclk	74.25
	dclk	55.6875
	mipi_clk	222.75
	PLL2	445.5
	PLL1	297

Figure 35 shows raw 12-bit format.

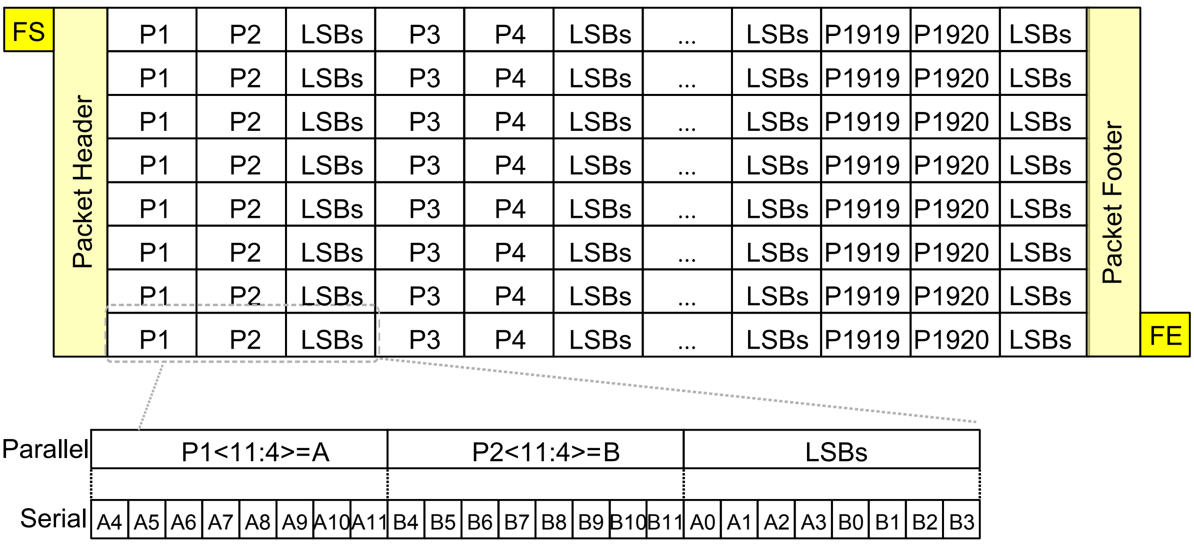


Figure 35 MIPI raw12 frame format

Table 29 shows registers relevant to MIPI and LVDS mode setting.

Table 29 Register Table - MIPI and LVDS mode setting

Register name	Address Bank	Address Hex	Bits	Init. Val.	Type	Up date	Description
mipi_en	F	04	[6]	1'b0	RW	aev	MIPI enable 1'b0 : disable 1'b1 : enable
clk_hs_mode	F	04	[4]	1'b1	RW	aev	MIPI clock lane hs mode 1'b0 : LP & HS mode 1b'1 : only HS mode

MIPI Global Operation

- Data Unit and Bit Transmission Order

MIPI transmitter serially sends data in byte unit starting from LSB. Figure 36 shows MIPI data transfer order.

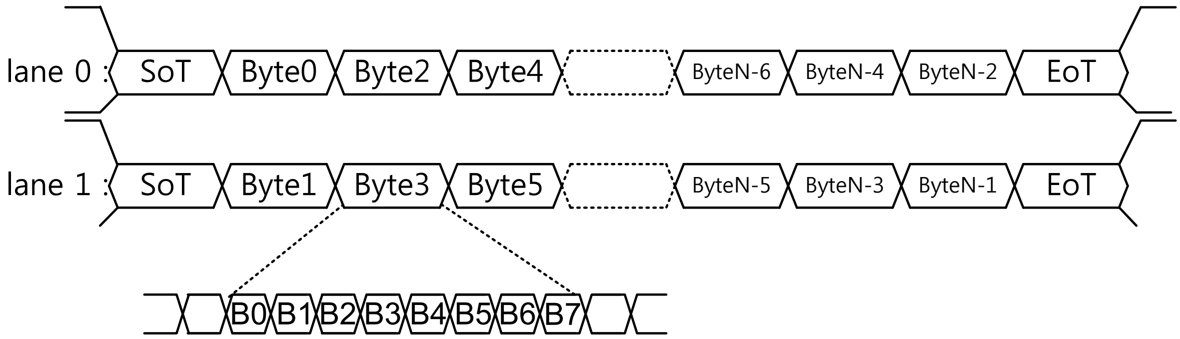


Figure 36 MIPI transmission order

- Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High-Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential-0 and Differential-1. Low Power signaling is used for both Control mode and Escape mode. The interpretation of Low-Power Lane states depends on the mode of operation.

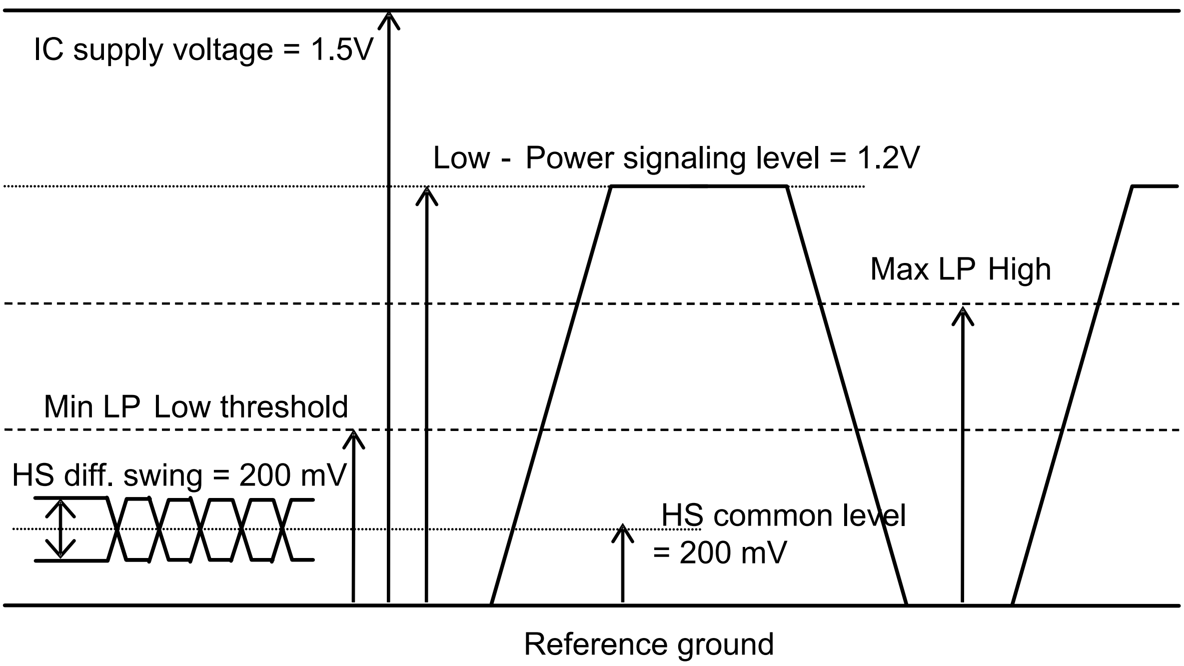


Figure 37 MIPI PAD levels

- Operating Modes : Control, High-Speed, and Escape
  During normal operation a Data Lane will be either in Control or High-Speed mode. High-Speed Data transmission happens in bursts and starts from and ends at a Stop state (LP-11), which is by definition in Control mode. The Lane is only in high-speed mode during Data bursts. The sequence to enter high speed mode is : LP-11, LP-01, LP-00 at which point the Data Lane remains in high speed mode until a LP-11 is received. The special Escape mode can only be entered via a request within Control mode. The Data Lane

shall always exit Escape mode and return to Control mode after detection of a Stop state. If not in High-Speed or Escape mode the Data Lane shall stay in Control mode. For Data Lanes and for Clock Lanes the Stop state serves as general standby state and may last for any period of time > T_{LPX}. Possible events starting from and ending in the Stop state are High-Speed Data Transmission burst (LP-11, LP-01, LP-00) and Escape mode request (LP-11, LP-10, LP-00, LP-01, LP-00). The Lane shall stay in the Stop state as long as no other state is presented on the Lane.

Table 30 Lane states description

State Code	Line Voltage Levels		High-Speed	Low-Power	
	DP-Line	DN-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

Table 31 shows registers relevant to PAD level control based on MIPI state.

Table 31 Register Table - MIPI PAD control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
mipi_ck_control	F	05	[7:4]	4'b1010	RW		MIPI CKP/CKN pad state control 4'b0000 : Normal operation mode 4'b0001 : CKP/CKN = LP-00 state 4'b0010 : CKP/CKN = LP-01 state 4'b0011 : CKP/CKN = LP-10 state 4'b0100 : CKP/CKN = LP-11 state 4'b0101 : CKP/CKN = HS-0 state 4'b0110 : CKP/CKN = HS-1 state 4'b0111 : CKP/CKN = Hi-z state 4'b1000 : CKP/CKN = ULP state 4'b1010 : CKP/CKN = power down
mipi_d0_control	F	06	[7:4]	4'b1010	RW		MIPI DP0/DN0 pad state control 4'b0000 : Normal operation mode 4'b0001 : DP0/DN0 = LP-00 state 4'b0010 : DP0/DN0 = LP-01 state 4'b0011 : DP0/DN0 = LP-10 state 4'b0100 : DP0/DN0 = LP-11 state 4'b0101 : DP0/DN0 = HS-0 state 4'b0110 : DP0/DN0 = HS-1 state 4'b0111 : DP0/DN0 = Hi-z state 4'b1000 : DP0/DN0 = ULP state 4'b1001 : DP0/DN0 = Serializer Test mode 4'b1010 : DP0/DN0 = power down
mipi_d1_control	F	06	[3:0]	4'b1010	RW		MIPI DP1/DN1 pad state control 4'b0000 : Normal operation mode 4'b0001 : DP1/DN1 = LP-00 state 4'b0010 : DP1/DN1 = LP-01 state

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							4'b0011 : DP1/DN1 = LP-10 state 4'b0100 : DP1/DN1 = LP-11 state 4'b0101 : DP1/DN1 = HS-0 state 4'b0110 : DP1/DN1 = HS-1 state 4'b0111 : DP1/DN1 = Hi-z state 4'b1000 : DP1/DN1 = ULP state 4'b1001 : DP1/DN1 = Serializer Test mode 4'b1010 : DP1/DN1 = power down
d0_lane_swap	F	09	[3:2]	2'b10	RW		Data0 lane data swap 2'b00 : d0 lane data 2'b01 : d1 lane data else : not used
d1_lane_swap	F	09	[1:0]	2'b11	RW		Data1 lane data swap 2'b00 : d0 lane data 2'b01 : d1 lane data else : not used
mipi_ck_NP_swap	F	0B	[3]	1'b0	RW		Mipi clock N/P swap
d0_NP_swap	F	0B	[7]	1'b0	RW		Data0 N/P swap
d1_NP_swap	F	0B	[6]	1'b0	RW		Data1 N/P swap
mipi_test_d0	F	2D	[7:0]	0xAA	RW		MIPI test data 0 for HS state
mipi_test_d1	F	2E	[7:0]	0xFF	RW		MIPI test data 1 for HS state

Low Level Protocol

The Low Level Protocol (LLP) is a byte oriented, packet based protocol that supports the transport of image data using Short and Long packet formats. For each packet structure, exit from the low power state followed by the Start of Transmission (SoT) sequence indicates the start of the packet. The End of Transmission (EoT) sequence followed by the low power state indicates the end of the packet.

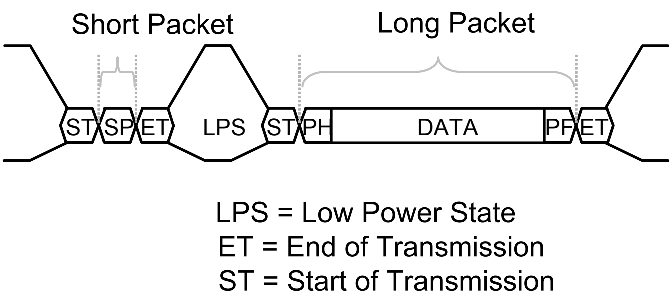


Figure 38 MIPI low level protocol

- Short Packet Format
  The PK5210N supports two types of Short Packets for frame synchronization : Frame Start (FS) Packet and Frame End (FE) Packet. Data ID field is 00h for FS and 01h for FE. Each image frame shall begin with a FS packet containing the Frame Start Code. The FS Packet shall be followed by one or more long packets containing image data. Each image frame shall end with a FE packet containing the Frame End Code. For FS and FE synchronization packets the Short Packet Data Field shall contain a 16-bit frame number. This

frame number is the same for the FS and FE synchronization packets corresponding to a given frame. The 16-bit frame number shall always be non-zero to distinguish it from the use-case where frame number is inoperative and remains set to zero. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short Packet.

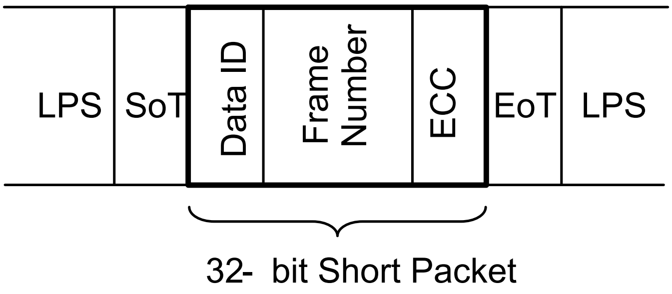


Figure 39 MIPI short packet structure

- Long Packet Format
  A Long Packet shall consist of 3 elements : a 32-bit Packet Header (PH), an application Data Payload with a variable number of 8-bit words and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements : an 8-bit Data Identifier, a 16-bit Word Count field and an 8-bit ECC. The Packet Footer has one element : a 16-bit checksum. The Word Count defines the number of 8-bit data words in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count. After the end of the Packet Header the receiver reads the next WC*8-bits data words of the Data Payload. While reading the Data Payload the receiver shall not look for any embedded sync codes. Therefore, there are no limitations on the value of a data word. Once the receiver has read the Data Payload it reads the checksum in the Packet Footer. In the generic case, the length of the Data Payload shall be a multiple of 8-bit data words. In addition, each image data format may impose additional restrictions on the length of the payload data. Each byte shall be transmitted least significant bit first. Multi-byte elements such as Word Count, Checksum and the Short packet 16-bit Data Field shall be transmitted least significant byte first.

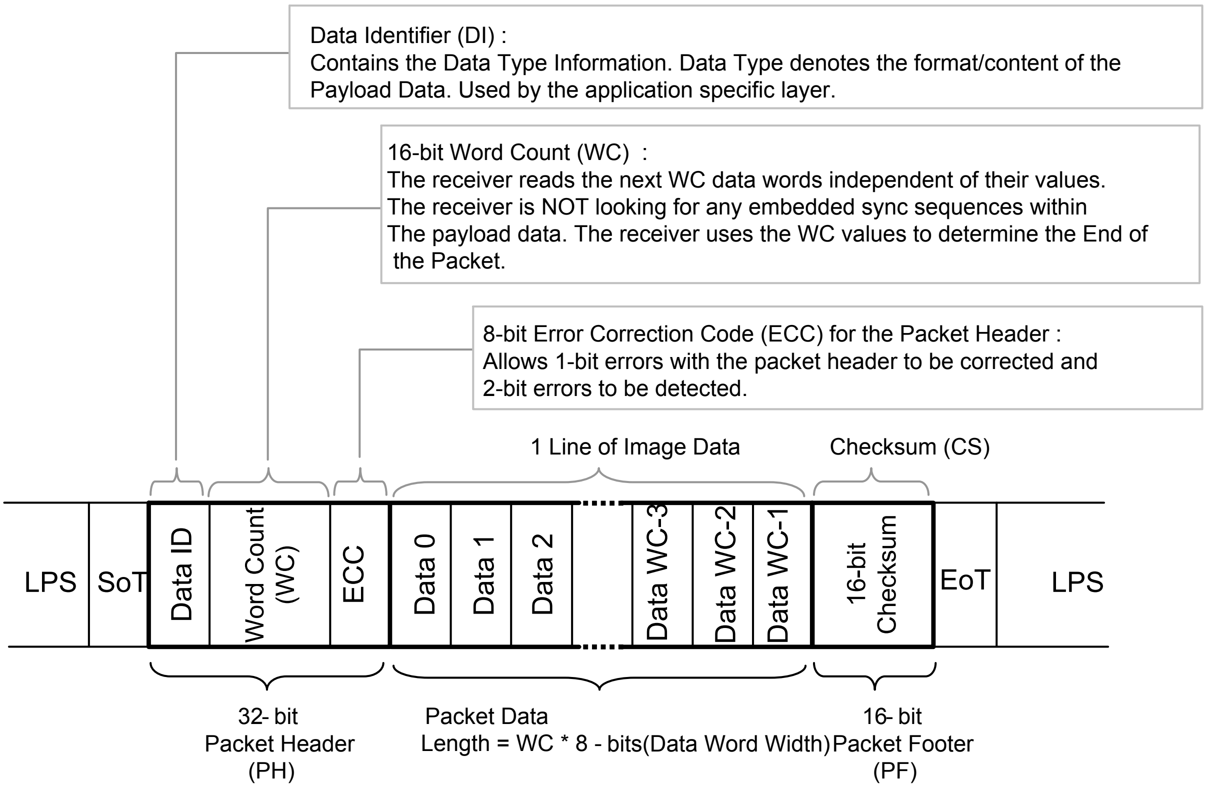


Figure 40 MIPI long packet structure

Table 32 MIPI Data Type and Data ID

Data ID	Data Type (Image Format)	Packet Type
00 hex	Frame start	Short
01 hex	Frame end	Short
2C hex	Raw bayer 12-bit	Long

Table 33 shows registers relevant to MIPI packet.

Table 33 Register Table - MIPI packet control

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
mipi_pkt_size0_h	F	36	[7:0]	0x09	RW		MIPI word counter size 0 control for image data High Byte
mipi_pkt_size0_l	F	37	[7:0]	0x6F	RW		MIPI word counter size 0 control for image data Low Byte
mipi_pkt_size1_h	F	38	[7:0]	0x09	RW		MIPI word counter size 1 control for image data High Byte
mipi_pkt_size1_l	F	39	[7:0]	0x6F	RW		MIPI word counter size 1 control for image data Low Byte
mipi_pkt_size2_h	F	3A	[7:0]	0x09	RW		MIPI word counter size 2 control for image data High Byte

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
mipi_pkt_size2_l	F	3B	[7:0]	0x6F	RW		MIPI word counter size 2 control for image data Low Byte
mipi_data_id0	F	42	[7:0]	0x2B	RW		MIPI data 0 identifier
mipi_data_id1	F	43	[7:0]	0x6B	RW		MIPI data 1 identifier
mipi_data_id2	F	44	[7:0]	0xAB	RW		MIPI data 2 identifier

- Packet Spacing and Frame Format
  Between Low Level Protocol packets there must always be a transition into and out of the Low Power State (LPS). The packet spacing does not have to be a multiple of 8-bit data words as the receiver will synchronize to the correct byte boundary during the SoT sequence prior to the Packet Header of the next packet.

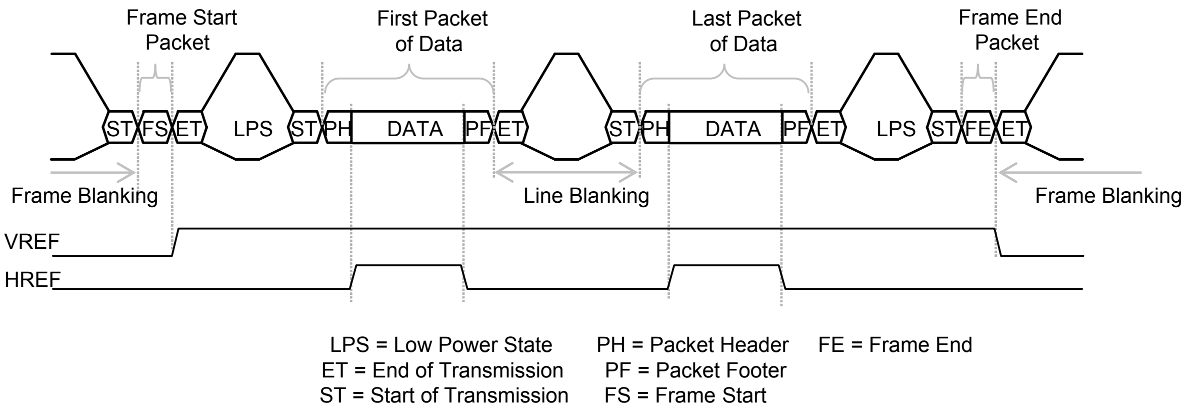


Figure 41 MIPI multiple packet

MIPI Electrical Characteristics

- Low-Power Transmitter
  The Low-Power transmitter is a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes. It is therefore important that the static power consumption of a LP transmitter be as low as possible. The slew-rate of signal transitions is bounded in order to keep EMI low.

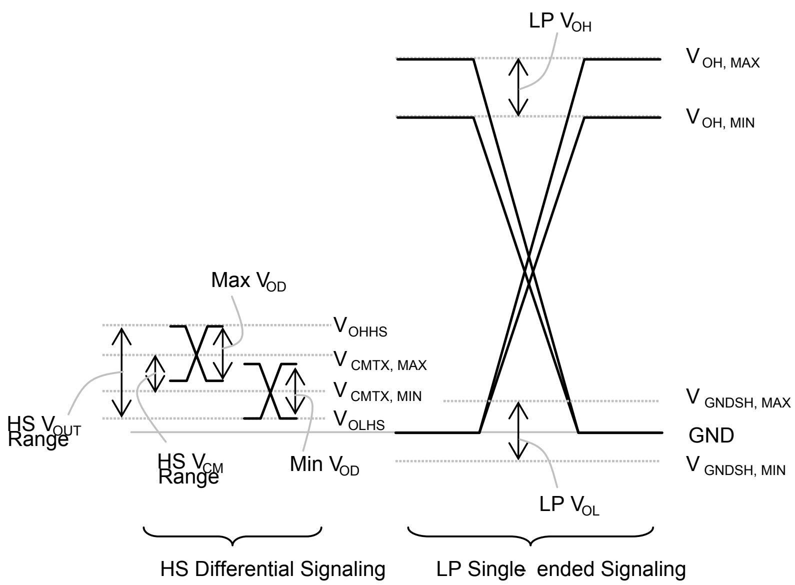


Figure 42 D-PHY signaling levels

Table 34 LP transmitter DC characteristics

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OL}	Thevenin output low level	-50		50	mV	
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
Z_{OLP}	Output Impedance of LP transmitter	110			Ohm	

Table 35 LP transmitter DC characteristics

Parameter	Description	Min	Nom	Max	Units	Notes
t_{RLP} / t_{FLP}	15%-85% rise time and fall time			25	ns	1, 5
t_{REOT}	30%-85% rise time in EOT state			35	ns	4, 5, 6
dV/dt_{SR}	Slew rate			120	mV/ns	1, 2, 3
C_{LOAD}	Load Capacitance	0		70	pF	

Notes 1. When the output is loaded with a capacitive load C_{LOAD}
Notes 2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
Notes 3. Measured as average across 50mV segment of the output signal transition.
Notes 4. The rise-time of t_{REOT} starts from the HS common level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
Notes 5. For capacitive loads from 0-70pF
Notes 6. With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the link.

- High-Speed Transmitter
  The reference characteristic impedance level is 100 Ohm differential, 50 Ohm single-ended per wire, and 25 Ohm common-mode for both wires together. A HS differential signal driven on the DP and DN pins is generated by a differential output driver. For reference, DP is considered as the positive side and DN as the negative side. The Lane state is called Differential-1 (HS-1) when the potential on DP is higher than the potential of DN. The Lane state is called Differential-0 (HS-0), when the potential on DP is lower than the potential of DN.

The differential output voltage V_{OD} is defined as the difference of the voltages V_{DP} and V_{DN} at the DP and DN pins, respectively.

$V_{OD}=V_{DP}-V_{DN}$

The output voltages V_{DP} and V_{DN} at the DP and DN pins shall not exceed the high-speed output high voltage V_{OHHS}. The common-mode voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the DP and DN pins :

$V_{CMTX}=(V_{DP}+V_{DN})/2$

Table 36 HS transmitter DC characteristics

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OD}	HS transmit differential voltage	140	200	270	mV	1
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV	1
ΔV_{OD}	VOD mismatch when output is Differential-1 or Differential-0			10	mV	
ΔV_{CMTX}	VCMTX mismatch when output is Differential-1 or Differential-0			5	mV	
V_{OHHS}	HS output high voltage			360	mV	1
Z_{OS}	Single ended output impedance	40	50	62.5	W	
ΔZ_{OS}	Single ended output impedance mismatch			10	%	
Notes 1. Value when driving into load impedance						

Table 37 HS transmitter AC characteristics

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variation above 450MHz			15	mV_{RMS}	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz			25	mV_{PEAK}	1
t_R / t_F	20%-80% rise time and fall time	150		$0.3UI_{NOM}$	ps	2
Notes 1. VPP is the voltage difference compared to the DC average common-mode potential. Notes 2. UI_{NOM} is the long term average Unit Interval.						

- High-Speed Data-Clock Timing
  The Master side of the Link shall send a differential clock to the Slave side to be used for data sampling. This clock is at a fixed nominal frequency and stable for the entire duration of a data transfer. The DDR [Double Data Rate] Clock signal maintains a quadrature phase relationship to the data signal. Data will be sampled by both the rising and falling edges of the Clock signal. The Clock signal is a differential signal. Use of the term “rising-edge” means “rising edge of the signal (CLPp – CLKn)” and similarly for “falling edge”. Therefore, the frequency of the Clock signal will be half the desired data rate in bits per second. The timing relationship of the DDR Clock differential signal to the NRZ Data differential signal is shown in Figure 43 . Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data. The rising edge of the DDR Clock is sent during the first bit of each byte, such that the receiver can sample the bits of each byte starting with a rising edge.

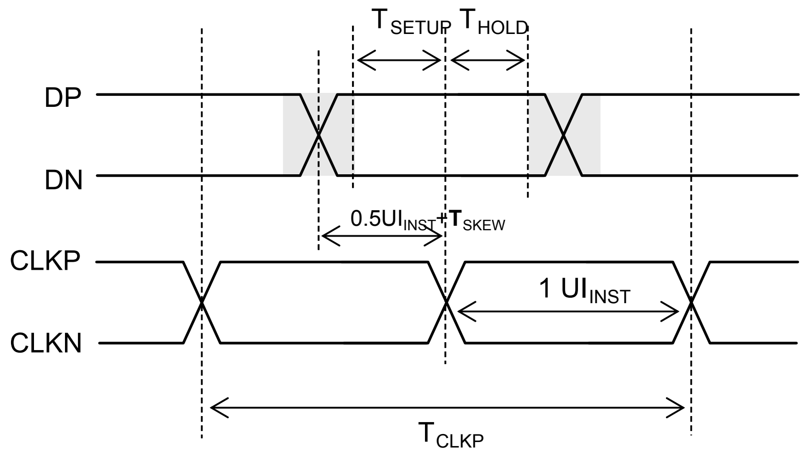


Figure 43 Data to clock timing

Table 38 MIPI clock signal spec

Clock Parameter	Symbol	Min	Nom	Max	Units	Notes
$UI_{instantaneous}$	UI_{INST}	0.8		1.2	UI_{NOM}	
Data to Clock Skew	T_{SKEW}	-0.075		0.075	U_{INOM}	

Electrical Characteristics

PK5210N does not have tolerant input pads. The input signal must have HVDD power level for stable operation. If the power of input signal is higher than the recommended level, leakage current may flow via short circuit path in the input pads.

DC Characteristics

Absolute maximum ratings [1]
AVDD supply voltage : -0.3 [V] to 4.0 [V]
HVDD supply voltage : -0.3 [V] to 4.0 [V]
DVDD supply voltage : -0.3 [V] to 1.8 [V]
DVDDM supply voltage : -0.3 [V] to 1.8 [V]
DC VTG at any input pin : -0.3 [V] to HVDD+0.3 [V]
DC VTG at any output pin : -0.3 [V] to HVDD+0.3 [V]
Storage temperature : -40 [^{o}C] to + 125 [^{o}C]

Table 39 DC characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
AVDD	Analog VDD(AVDD) voltage relative to GND(AGND) level	3.1	3.3	3.5	[V]
HVDD	High VDD(HVDD) voltage relative to GND(HGND) level @ DVP	1.62	1.8	3.5	[V]
			3.3		
	High VDD(HVDD) voltage relative to GND(HGND) level @ MIPI	3.1	3.3	3.5	[V]
DVDD	Digital VDD(DVDD) voltage relative to GND(DGND) level	1.28	1.3	1.35	[V]
DVDDM	Digital MIPI VDD(DVDDM) voltage relative to GND(DGND) level	1.28	1.3	1.35	[V]
I_{DDD}	HVDD=3.3 [V] @DVP	-	26	28	[mA]
	HVDD=1.8 [V] @DVP	-	12	13	
	AVDD= 3.3 [V] @ DVP	-	28	30	
	DVDD= 1.3 [V] @ DVP	-	130	146	
	HVDD=3.3 [V] @MIPI	-	1	2	
	AVDD= 3.3 [V] @ MIPI	-	28	30	
	DVDD= 1.3 [V] @ MIPI	-	130	149	
I_{DDS}	Standby supply current	-	0.7	10.3	[mA]
V_{IL1}	Input voltage low level	-	-	HVDD*0.3	[V]
V_{IH1}	Input voltage high level	HVDD*0.7	-	-	[V]
V_{IL2}	Input voltage low level for rClk, rData.	-	-	HVDD*0.3	[V]
V_{IH2}	Input voltage high level for rClk, rData .	HVDD*0.7	-	-	[V]
C_{IN}	Input pin capacitance	-	-	10	[pF]
V_{OL1}	Output voltage low	-	-	HVDD*0.2	[V]

[1]Excessive stresses may cause permanent damage to the device.

Symbol	Descriptions	Min	Typ	Max	Unit
V_{OH1}	Output voltage high	HVDD*0.8	-	-	[V]
V_{OL2}	Output voltage low level for rClk, rData.	-	-	HVDD*0.2	[V]
V_{OH2}	Output voltage high level for rData.	HVDD*0.8	-	-	[V]
I_{IN}	Input leakage current	-10	-	10	[uA]
I_{OT}	Output leakage current	-10	-	10	[uA]

AC Characteristics

Table 40 2-wire serial interface characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
f_{SCL}	2-wire serial interface Clock frequency	-	-	400	kHz
T_{ic}	2-wire serial interface Clock period	2.5	-	-	us
T_{icl}	2-wire serial interface Clock low level width	1.66	-	-	us
T_{ich}	2-wire serial interface Clock high level width	0.83	-	-	us
T_{iss}	Setup time for start condition	0.83	-	-	us
T_{ihs}	Hold time for start condition	0.83	-	-	us
T_{isd}	Setup time for input data	266	-	-	ns
T_{ihd}	Hold time for input data	0	-	-	ns
T_{isp}	Setup time for stop condition	0.83	-	-	us
T_{buf}	Bus free time between a stop and a new start condition	1.66	-	-	us
T_{oaa}	Delay from SCL falling edge to output data transition	-	-	354	ns
T_r	10% to 90% rising time for SCL/SDA (load : 10pF)	-	-	46	ns
T_f	90% to 10% falling time for SCL/SDA (load : 10pF)	-	-	37	ns
R_p	SCL, SDA pull-up resistor	-	2	-	kΩ

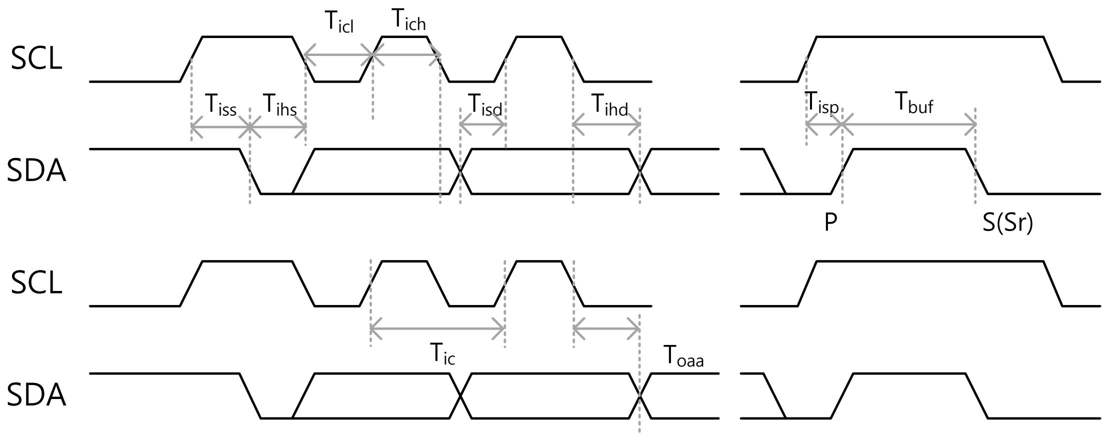


Figure 44 Timing diagram of SCL and SDA

Register Map

Table 41   Register Table - Group A

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bank	A	03	[7:0]	0x00	RW		Register group selector
mirror	A	05	[1:0]	0x00	RW	aev	Image Inversion mirror[1] : vertical inversion mirror[0] : horizontal inversion
framewidth_h	A	06	[4:0]	0x08	RW	aev	Framewidth High Byte (must be larger than window width)
framewidth_l	A	07	[7:0]	0x97	RW	aev	Framewidth Low Byte (must be larger than window width)
fheight_a_h	A	08	[4:0]	0x04	RW	aev	Frameheight High Byte (must be larger than window height)
fheight_a_l	A	09	[7:0]	0x7C	RW	aev	Frameheight Low Byte (must be larger than window height)
i2c_control_1	A	1A	[7:0]	0x50	RW		I2c control register 1
softreset	A	20	[0]	0x00	RW		Soft reset 1'b0 : disable 1'b1 : enable (after succesful reset value reverts to 0)
pad_control1	A	23	[7:0]	0x60	RW		Pad control 1
pad_control2	A	24	[7:0]	0x00	RW		Pad control 2
pad_control3	A	25	[7:0]	0x00	RW		Pad control 3
pad_control4	A	26	[7:0]	0x00	RW		Pad control 4
pad_control5	A	27	[7:0]	0x00	RW		Pad control 5
pll_control2	A	4E	[7:0]	0x7A	RW		PLL control 2
pll_tg_n_cnt	A	51	[7:0]	0x2C	RW		TG PLL multiplication factor
pll_tg_r_cnt	A	52	[4:0]	0x04	RW		TG PLL division factor
pll_mp_n_cnt	A	53	[7:0]	0x2C	RW		MIPI PLL multiplication factor
pll_mp_r_cnt	A	54	[4:0]	0x04	RW		MIPI PLL division factor
clkdiv1	A	56	[7:0]	0x20	RW	aev	Clock divider 1
clkdiv2	A	57	[7:0]	0x50	RW	aev	Clock divider 2
clkdiv3	A	58	[7:0]	0xF3	RW	aev	Clock divider 3
sync_blankEAV_h	A	63	[3:0]	0x0B	RW		Blanking EAV control High Byte
sync_blankEAV_l	A	64	[7:0]	0x60	RW		Blanking EAV control Low Byte
sync_blankSAV_h	A	65	[3:0]	0x0A	RW		Blanking SAV control High Byte
sync_blankSAV_l	A	66	[7:0]	0xB0	RW		Blanking SAV control Low Byte
sync_activeEAV_h	A	67	[3:0]	0x09	RW		Active EAV control High Byte
sync_activeEAV_l	A	68	[7:0]	0xD0	RW		Active EAV control Low Byte
sync_activeSAV_h	A	69	[3:0]	0x08	RW		Active SAV control High Byte

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
sync_activeSAV_l	A	6A	[7:0]	0x00	RW		Active SAV control Low Byte
sync_CCIR_FF_h	A	6B	[3:0]	0x0F	RW		Format header control 0 (FF) High Byte
sync_CCIR_FF_l	A	6C	[7:0]	0xFF	RW		Format header control 0 (FF) Low Byte
sync_CCIR_00_h	A	6D	[3:0]	0x00	RW		Format header control 1 (00) High Byte
sync_CCIR_00_l	A	6E	[7:0]	0x00	RW		Format header control 1 (00) Low Byte
sync_CCIR_80_h	A	6F	[3:0]	0x08	RW		Blank data control 0 (80) High Byte
sync_CCIR_80_l	A	70	[7:0]	0x00	RW		Blank data control 0 (80) Low Byte
sync_CCIR_10_h	A	71	[3:0]	0x01	RW		Blank data control 1 (10) High Byte
sync_CCIR_10_l	A	72	[7:0]	0x00	RW		Blank data control 1 (10) Low Byte
vsyncstartrow0_h	A	74	[4:0]	0x00	RW	aev	Parallel interface - Vertical sync start control High Byte MIPI interface @ Virtual channel 0 - Frame start control High Byte
vsyncstartrow0_l	A	75	[7:0]	0x17	RW	aev	Parallel interface - Vertical sync start control Low Byte MIPI interface @ Virtual channel 0 - Frame start control Low Byte
vsyncstoprow0_h	A	76	[4:0]	0x04	RW	aev	Parallel interface - Vertical sync end control High Byte MIPI interface @ Virtual channel 0 - Frame end control High Byte
vsyncstoprow0_l	A	77	[7:0]	0x5F	RW	aev	Parallel interface - Vertical sync end control Low Byte MIPI interface @ Virtual channel 0 - Frame end control Low Byte
vsynccolumn0_h	A	78	[4:0]	0x00	RW	aev	Internal vsync 0 start point High Byte @ column counter
vsynccolumn0_l	A	79	[7:0]	0x02	RW	aev	Internal vsync 0 start point Low Byte @ column counter
sync_control_0	A	AD	[7:0]	0x80	RW	aev	Sync_control 0
sync_control_1	A	AE	[7:0]	0x00	RW	aev	Sync_control 1
data_min_h	A	B0	[3:0]	0x00	RW		Minimum active data High Byte
data_min_l	A	B1	[7:0]	0x00	RW		Minimum active data Low Byte
data_max_h	A	B2	[3:0]	0x0F	RW		Maximum active data High Byte
							d0_lane_swap Data0 lane data swap 2'b00 : d0 lane data 2'b01 : d1 lane data else : not used
							d1_lane_swap Data1 lane data swap 2'b00 : d0 lane data 2'b01 : d1 lane data else : not used

Table 42 Register Table - Group B

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
bayer_control_07	B	0A	[7:0]	0x00	RW		bayer control 07
bayer_control_14	B	11	[7:0]	0x00	RW		bayer control 14
rcount_genlock_h	B	50	[4:0]	0x00	RW		Genlock row count High Byte
rcount_genlock_l	B	51	[7:0]	0x01	RW		Genlock row count Low Byte
ccount_genlock_h	B	52	[4:0]	0x00	RW		Genlock column count High Byte
ccount_genlock_l	B	53	[7:0]	0x01	RW		Genlock column count Low Byte
genlock_width	B	54	[7:0]	0x10	RW		Genlock pulse width
inttime_h	B	6E	[7:0]	0x01	RW	wr_en	Integration time 0 (line) High Byte
inttime_m	B	6F	[7:0]	0x40	RW	wr_en	Integration time 0 (line) Low Byte
inttime_l	B	70	[7:0]	0x00	RW	wr_en	Iinteration time 0 (column)
inttime_vs_h	B	71	[7:0]	0x00	RW	wr_en	Integration time 1 (line) High Byte
inttime_vs_m	B	72	[7:0]	0x02	RW	wr_en	Integration time 1 (line) Low Byte
inttime_vs_l	B	73	[7:0]	0x00	RW	wr_en	Iinteration time 1 (column)
globalgain	B	74	[7:0]	0x00	RW	wr_en	Analog gain
digitalgain_l	B	75	[7:0]	0x10	RW	wr_en	Digital gain of long data
digitalgain_s	B	76	[7:0]	0x10	RW	wr_en	Digital gain of short data
digitalgain_vs	B	77	[7:0]	0x10	RW	wr_en	Digital gain of very short data
wr_en	B	8D	[0]	0x00	RW		Update exposure related register 1'b0 : no update 1'b1 : wr_en set
wr_en_off	B	8E	[0]	0x00	RW		Update exposure related register 1'b0 : update @ wr_en = 1'b1 1'b1 : Immediately update
tp_control_0	B	BC	[7:0]	0x00	RW		Test pattern selection
tp_control_1_h	B	BD	[7:0]	0x00	RW		R color for test pattern High Byte
tp_control_1_l	B	BE	[7:0]	0x00	RW		R color for test pattern Low Byte
tp_control_2_h	B	BF	[7:0]	0x00	RW		G1 color for test pattern High Byte
tp_control_2_l	B	C0	[7:0]	0x00	RW		G1 color for test pattern Low Byte
tp_control_3_h	B	C1	[7:0]	0x00	RW		G2 color for test pattern High Byte
tp_control_3_l	B	C2	[7:0]	0x00	RW		G2 color for test pattern Low Byte
tp_control_4_h	B	C3	[7:0]	0x00	RW		B color for test pattern High Byte
tp_control_4_l	B	C4	[7:0]	0x00	RW		B color for test pattern Low Byte
tp_width_h	B	C5	[2:0]	0x07	RW		Test pattern width for color bar pattern High Byte
tp_width_l	B	C6	[7:0]	0xA8	RW		Test pattern width for color bar pattern Low Byte

Table 43 Register Table - Group F

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
mipi_control_0	F	04	[7:0]	0x30	RW	aev	MIPI control 0
mipi_control_1	F	05	[7:0]	0xAB	RW		MIPI control 1
mipi_control_2	F	06	[7:0]	0xAA	RW		MIPI control 2
mipi_control_5	F	09	[7:0]	0x1B	RW		MIPI control 5
mipi_control_7	F	0B	[7:0]	0x00	RW		MIPI control 7
mipi_test_d0	F	2D	[7:0]	0xAA	RW		MIPI test data 0 for HS state
mipi_test_d1	F	2E	[7:0]	0xFF	RW		MIPI test data 1 for HS state
mipi_pkt_size0_h	F	36	[7:0]	0x09	RW		MIPI word counter size 0 control for image data High Byte
mipi_pkt_size0_l	F	37	[7:0]	0x6F	RW		MIPI word counter size 0 control for image data Low Byte
mipi_pkt_size1_h	F	38	[7:0]	0x09	RW		MIPI word counter size 1 control for image data High Byte
mipi_pkt_size1_l	F	39	[7:0]	0x6F	RW		MIPI word counter size 1 control for image data Low Byte
mipi_pkt_size2_h	F	3A	[7:0]	0x09	RW		MIPI word counter size 2 control for image data High Byte
mipi_pkt_size2_l	F	3B	[7:0]	0x6F	RW		MIPI word counter size 2 control for image data Low Byte
mipi_data_id0	F	42	[7:0]	0x2B	RW		MIPI data 0 identifier
mipi_data_id1	F	43	[7:0]	0x6B	RW		MIPI data 1 identifier
mipi_data_id2	F	44	[7:0]	0xAB	RW		MIPI data 2 identifier

Table 44 Register Table - Group G

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
isp_func_2	G	06	[7:0]	0x00	RW	aev	ISP_control 2
nr_ratio_l	G	37	[7:0]	0x08	RW	aev	NR strength control (long)
nr_ratio_s	G	3A	[7:0]	0x08	RW	aev	NR strength control (short)
nr_ratio_vs	G	3D	[7:0]	0x08	RW	aev	NR strength control (very-short)
cmp_x1_h	G	B5	[1:0]	0x00	RW	aev	Explanatory variable point 1 for compress
cmp_x1_m	G	B6	[7:0]	0x40	RW	aev	Explanatory variable point 1 for compress
cmp_x1_l	G	B7	[7:0]	0x00	RW	aev	Explanatory variable point 1 for compress
cmp_x2_h	G	B8	[1:0]	0x00	RW	aev	Explanatory variable point 2 for compress
cmp_x2_m	G	B9	[7:0]	0x80	RW	aev	Explanatory variable point 2 for compress
cmp_x2_l	G	BA	[7:0]	0x00	RW	aev	Explanatory variable point 2 for compress
cmp_x3_h	G	BB	[1:0]	0x01	RW	aev	Explanatory variable point 3 for compress
cmp_x3_m	G	BC	[7:0]	0x00	RW	aev	Explanatory variable point 3 for compress
cmp_x3_l	G	BD	[7:0]	0x00	RW	aev	Explanatory variable point 3 for compress
cmp_x4_h	G	BE	[1:0]	0x02	RW	aev	Explanatory variable point 4 for compress
cmp_x4_m	G	BF	[7:0]	0x00	RW	aev	Explanatory variable point 4 for compress
cmp_x4_l	G	C0	[7:0]	0x00	RW	aev	Explanatory variable point 4 for compress
cmp_y0_h	G	C1	[3:0]	0x00	RW	aev	Dependent variable point 0 for compress
cmp_y0_l	G	C2	[7:0]	0x00	RW	aev	Dependent variable point 0 for compress
cmp_y1_h	G	C3	[3:0]	0x04	RW	aev	Dependent variable point 1 for compress
cmp_y1_l	G	C4	[7:0]	0x00	RW	aev	Dependent variable point 1 for compress
cmp_y2_h	G	C5	[3:0]	0x06	RW	aev	Dependent variable point 2 for compress
cmp_y2_l	G	C6	[7:0]	0x00	RW	aev	Dependent variable point 2 for compress
cmp_y3_h	G	C7	[3:0]	0x08	RW	aev	Dependent variable point 3 for compress
cmp_y3_l	G	C8	[7:0]	0x80	RW	aev	Dependent variable point 3 for compress
cmp_y4_h	G	C9	[3:0]	0x0C	RW	aev	Dependent variable point 4 for compress
cmp_y4_l	G	CA	[7:0]	0x00	RW	aev	Dependent variable point 4 for compress
cmp_y5_h	G	CB	[3:0]	0x0F	RW	aev	Dependent variable point 5 for compress
cmp_y5_l	G	CC	[7:0]	0xFF	RW	aev	Dependent variable point 5 for compress

Table 45 Register Table - Group H

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
wdr_ctrl_0	H	04	[7:0]	0x00	RW	aev	Control signals for WDR
wdr_cgain	H	07	[7:0]	0x40	RO		color gain monitoring register to check the value currently being applied
wdr_cgain	H	1B	[7:0]	0x40	RO		detail gain monitoring register to check the value currently being applied
con_sl_a	H	58	[7:0]	0x08	RW	aev	dark region slope for local tonemap contrast 8'h08 : corresponds to the slope 1.0
con_sl_b1	H	59	[7:0]	0x08	RW	aev	bright region slope for local tonemap contrast con_sl_b=con_sl_b1 * con_sl_b2 8'h40 : corresponds to gain 1.0 for cont_sl_b
con_sl_b2	H	5A	[7:0]	0x08	RW	aev	bright region slope for local tonemap contrast
loc_sgain_c	H	5B	[7:0]	0x00	RO		local sigma gain monitoring register to check the value currently being applied
loc_locsig_ratio	H	65	[4:0]	0x10	RW	aev	local sigma weight 8'h00 : local sigma weight is 0% global sigma weight is 100% 8'h10 : local sigma weight is 100% global sigma weight is 0%
loc_sig_min_c	H	67	[7:0]	0x00	RO		local sigma minimum monitoring register to check the value currently being applied
lens_scale	H	80	[7:0]	0x80	RW	aev	LSC scale control
lens_x	H	81	[7:0]	0x00	RW	aev	LSC center control
lens_y	H	82	[7:0]	0x00	RW	aev	LSC center control
loc_sgain_c_yref0	H	A8	[7:0]	0x10	RW	aev	local sigma gain for exposure 0 level 8'h10 : corresponds to gain 1.0
loc_sgain_c_yref1	H	A9	[7:0]	0x10	RW	aev	local sigma gain for exposure 1 level
loc_sgain_c_yref2	H	AA	[7:0]	0x10	RW	aev	local sigma gain for exposure 2 level
loc_sgain_c_yref3	H	AB	[7:0]	0x10	RW	aev	local sigma gain for exposure 3 level
loc_sgain_c_yref4	H	AC	[7:0]	0x10	RW	aev	local sigma gain for exposure 4 level
loc_sgain_c_yref5	H	AD	[7:0]	0x10	RW	aev	local sigma gain for exposure 5 level
wdr_cgain_yref0	H	AE	[7:0]	0x40	RW	aev	color gain for exposure 0 level 8'h40 corresponds to gain 1.0
wdr_cgain_yref1	H	AF	[7:0]	0x40	RW	aev	color gain for exposure 1 level
wdr_cgain_yref2	H	B0	[7:0]	0x40	RW	aev	color gain for exposure 2 level
wdr_cgain_yref3	H	B1	[7:0]	0x40	RW	aev	color gain for exposure 3 level
wdr_cgain_yref4	H	B2	[7:0]	0x40	RW	aev	color gain for exposure 4 level
wdr_cgain_yref5	H	B3	[7:0]	0x40	RW	aev	color gain for exposure 5 level
wdr_cgain_yref0	H	B4	[7:0]	0x40	RW	aev	detail gain for exposure 0 level 8'h40 : corresponds to gain 1.0

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
wdr_cgain_yref1	H	B5	[7:0]	0x40	RW	aev	detail gain for exposure 1 level
wdr_cgain_yref2	H	B6	[7:0]	0x40	RW	aev	detail gain for exposure 2 level
wdr_cgain_yref3	H	B7	[7:0]	0x40	RW	aev	detail gain for exposure 3 level
wdr_cgain_yref4	H	B8	[7:0]	0x40	RW	aev	detail gain for exposure 4 level
wdr_cgain_yref5	H	B9	[7:0]	0x40	RW	aev	detail gain for exposure 5 level
loc_sig_min_yref0	H	C6	[7:0]	0x00	RW	aev	local sigma minimum for exposure 0 level
loc_sig_min_yref1	H	C7	[7:0]	0x00	RW	aev	local sigma minimum for exposure 1 level
loc_sig_min_yref2	H	C8	[7:0]	0x00	RW	aev	local sigma minimum for exposure 2 level
loc_sig_min_yref3	H	C9	[7:0]	0x00	RW	aev	local sigma minimum for exposure 3 level
loc_sig_min_yref4	H	CA	[7:0]	0x00	RW	aev	local sigma minimum for exposure 4 level
loc_sig_min_yref5	H	CB	[7:0]	0x00	RW	aev	local sigma minimum for exposure 5 level

Table 46 Register Table - Group I

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
dgain_isp	I	88	[7:0]	0x00	RW	aev	ISP digitalgain (10h = x1, … , FFh = x15.9735)
ADG_ratio	I	BD	[7:0]	0x08	RW	aev	ADG ratio (02h = x1)

Table 47 Register Table - Control register map

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
pad_control1	A	23	[5:4]	2'b10	RW		**stdby_level** Output data pad stdby level selector 2'b00 : low 2'b01 : high 2'b1x : hiz
	A	23	[3]	1'b0	RW		**clkoff** Clock pad kill enable 1'b0 : disable (not kill) 1'b1 : enable (kill)
pad_control2	A	24	[7:6]	2'b00	RW		**pad_drv** Data pad drivability control
	A	24	[5:4]	2'b00	RW		**pclk_drv** PCLK pad drivability control
	A	24	[3:0]	4'b0000	RW		**dly_digi_PCLK** PCLK timing delay delay = dly_digi_PCLK*0.4 ns
pad_control3	A	25	[7]	1'b0	RW		**vsync_pad_en** Vsync pad enable 1'b0 : disable 1'b1 : enable
	A	25	[6:5]	2'b00	RW		**hsync_drv** Hsync Pad drivability control
	A	25	[4]	1'b0	RW		**hsync_pad_en** Hsync pad enable 1'b0 : disable 1'b1 : enable
	A	25	[3]	1'b0	RW		**pclk_pad_en** PCLK pad enable 1'b0 : disable 1'b1 : enable
	A	25	[2]	1'b0	RW		**pclk_polarity** Change PCLK phase
	A	25	[1]	1'b0	RW		**dpad_swap** Data pad swap option 1'b0 : [MSB:LSB] 1'b1 : [LSB:MSB]
	A	25	[0]	1'b0	RW		**genlock_pad_en** GENLOCK pad enable 1'b0 : disable 1'b1 : enable
pad_control4	A	26	[7]	1'b0	RW		**d11_pad_en** D11 pad control 1'b0 : disable 1'b1 : enable
	A	26	[6]	1'b0	RW		**d10_pad_en** D10 pad control 1'b0 : disable

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							1'b1 : enable
	A	26	[5]	1'b0	RW		**d9_pad_en** D9 pad control 1'b0 : disable 1'b1 : enable
	A	26	[4]	1'b0	RW		**d8_pad_en** D8 pad control 1'b0 : disable 1'b1 : enable
	A	26	[3]	1'b0	RW		**d7_pad_en** D7 pad control 1'b0 : disable 1'b1 : enable
	A	26	[2]	1'b0	RW		**d6_pad_en** D6 pad control 1'b0 : disable 1'b1 : enable
	A	26	[1]	1'b0	RW		**d5_pad_en** D5 pad control 1'b0 : disable 1'b1 : enable
	A	26	[0]	1'b0	RW		**d4_pad_en** D4 pad control 1'b0 : disable 1'b1 : enable
pad_control5	A	27	[7]	1'b0	RW		**d3_pad_en** D3 pad control 1'b0 : disable 1'b1 : enable
	A	27	[6]	1'b0	RW		**d2_pad_en** D2 pad control 1'b0 : disable 1'b1 : enable
	A	27	[5]	1'b0	RW		**d1_pad_en** D1 pad control 1'b0 : disable 1'b1 : enable
	A	27	[4]	1'b0	RW		**d0_pad_en** D0 pad control 1'b0 : disable 1'b1 : enable
i2c_control_1	A	1A	[7:4]	4'b0101	RW		**updatecontrol** Control I2C register with autov, aev update type LSB 2-bit updatecontrol[1:0] controls aev update and MSB 2-bit updatecontrol[3:2] controls autov update 2'b00 : no update

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							2'b01 : aev update 2'b1x : immediate aev update
clkdiv1	A	56	[7:6]	2'b00	RW	aev	**adcclk_div** ADC clock divider isp_clk =vco1/(2^adcclk_div)
	A	56	[5:4]	2'b10	RW	aev	**ispclk_div** ISP clock divider isp_clk =vco1/(2^ispclk_div)
clkdiv2	A	57	[7:6]	2'b01	RW	aev	**mipiclk_div** MIPI clock divider mipi_clk =vco2/(2^mipiclk_div)
	A	57	[4:3]	2'b10	RW	aev	**ddclk_div** MIPI byte clock divider ddclk =vco2/(2^ddclk_div)
clkdiv3	A	58	[7]	1'b1	RW	aev	**isp_clk_en** isp clock enable
	A	58	[6]	1'b1	RW	aev	**tm_clk_en** tone map clock enable
pll_control2	A	4E	[5]	1'b1	RW		**plltg_pd** PLL1 power down mode 1'b0 : pll1 power on 1'b1 : pll1 power down
	A	4E	[4]	1'b1	RW		**pll_bypass** PLL bypass 1'b0 : use pll mode 1'b1 : pll bypass mode
	A	4E	[3]	1'b1	RW		**pllmp_pd** PLL2 power down mode 1'b0 : pll2 power on 1'b1 : pll2 power down
bayer_control_07	B	0A	[5]	1'b0	RW		**genlock_en** GENLOCK enable 1'b0 : disable 1'b1 : enable
	B	0A	[4]	1'b0	RW		**genlock_master** GENLOCK master 1'b0 : slave 1'b1 : master
bayer_control_14	B	11	[4:3]	2'b00	RW		**tp_seq** Test pattern block input sequence selection
	B	11	[2:1]	2'b00	RW		**tp_seq_vs** Test pattern block input sequence selection for very short
sync_control_0	A	AD	[6:5]	2'b00	RW	aev	**sync_drop** Vsync, hsync drop control 2'b00 : No drop 2'b01 : vsync drop

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							2'b10 : hsync drop 2'b11 : hsync and vsync drop
sync_control_1	A	AE	[6]	1'b0	RW	aev	**sync_vsyncPolarity** Vsync polarity change 1'b0 : disable 1'b1 : enable
	A	AE	[5]	1'b0	RW	aev	**sync_hsyncAllLines** Hsync output all lines enable(black and active) 1'b0 : No hsync during vertical blank 1'b1 : hsync during vertical blank
	A	AE	[4]	1'b0	RW	aev	**sync_hsyncPolarity** Hsync polarity change 1'b0 : disable 1'b1 : enable
	A	AE	[1]	1'b0	RW	aev	**data_clamp** Effective data clamping enable 1'b0 : disable 1'b1 : enable
mipi_control_0	F	04	[6]	1'b0	RW	aev	**mipi_en** MIPI enable 1'b0 : disable 1'b1 : enable
	F	04	[4]	1'b1	RW	aev	**clk_hs_mode** MIPI clock lane hs mode 1'b0 : LP & HS mode 1b'1 : only HS mode
mipi_control_1	F	05	[7:4]	4'b1010	RW		**mipi_ck_control** MIPI CKP/CKN pad state control 4'b0000 : Normal operation mode 4'b0001 : CKP/CKN = LP-00 state 4'b0010 : CKP/CKN = LP-01 state 4'b0011 : CKP/CKN = LP-10 state 4'b0100 : CKP/CKN = LP-11 state 4'b0101 : CKP/CKN = HS-0 state 4'b0110 : CKP/CKN = HS-1 state 4'b0111 : CKP/CKN = Hi-z state 4'b1000 : CKP/CKN = ULP state 4'b1010 : CKP/CKN = power down
mipi_control_2	F	06	[7:4]	4'b1010	RW		**mipi_d0_control** MIPI DP0/DN0 pad state control 4'b0000 : Normal operation mode 4'b0001 : DP0/DN0 = LP-00 state 4'b0010 : DP0/DN0 = LP-01 state 4'b0011 : DP0/DN0 = LP-10 state 4'b0100 : DP0/DN0 = LP-11 state 4'b0101 : DP0/DN0 = HS-0 state 4'b0110 : DP0/DN0 = HS-1 state 4'b0111 : DP0/DN0 = Hi-z state 4'b1000 : DP0/DN0 = ULP state 4'b1001 : DP0/DN0 = Serializer Test

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							mode 4'b1010 : DP0/DN0 = power down
	F	06	[3:0]	4'b1010	RW		**mipi_d1_control** MIPI DP1/DN1 pad state control 4'b0000 : Normal operation mode 4'b0001 : DP1/DN1 = LP-00 state 4'b0010 : DP1/DN1 = LP-01 state 4'b0011 : DP1/DN1 = LP-10 state 4'b0100 : DP1/DN1 = LP-11 state 4'b0101 : DP1/DN1 = HS-0 state 4'b0110 : DP1/DN1 = HS-1 state 4'b0111 : DP1/DN1 = Hi-z state 4'b1000 : DP1/DN1 = ULP state 4'b1001 : DP1/DN1 = Serializer Test mode 4'b1010 : DP1/DN1 = power down
mipi_control_5	F	09	[3:2]	2'b10	RW		**d0_lane_swap** Data0 lane data swap 2'b00 : d0 lane data 2'b01 : d1 lane data else : not used
	F	09	[1:0]	2'b11	RW		**d1_lane_swap** Data1 lane data swap 2'b00 : d0 lane data 2'b01 : d1 lane data else : not used
mipi_control_7	F	0B	[7]	1'b0	RW		**d0_NP_swap** Data0 N/P swap
	F	0B	[6]	1'b0	RW		**d1_NP_swap** Data1 N/P swap
	F	0B	[3]	1'b0	RW		**mipi_ck_NP_swap** Mipi clock N/P swap
isp_func_2	G	06	[7]	1'b0	RW	aev	**nr_en_l** NR enable (long) 1'b0 : disable 1'b1 : enable
	G	06	[6]	1'b0	RW	aev	**nr_en_s** NR enable (short) 1'b0 : disable 1'b1 : enable
	G	06	[5]	1'b0	RW	aev	**nr_en_vs** NR enable (very-short) 1'b0 : disable 1'b1 : enable
	G	06	[0]	1'b0	RW	aev	**isp_dgain_en** ISP digitalgain enable 1'b0 : disable 1'b1 : enable
wdr_ctrl_0	H	04	[6]	1'b0	RW	aev	**lens_en**

Register name	Address		Bits	Init. Val.	Type	Up date	Description
	Bank	Hex					
							Lens shading compensation enable 1'b0 : disable 1'b1 : enable
	H	04	[4]	1'b0	RW	aev	**tm_en** Tonemap enable 1'b0 : disable 1'b1 : enable

Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	06/01/2021	(Preliminary)	Jaedong Park
0.1	21/01/2021	• Update General Description. - P.6 – DVDD, DVDDM – Power consumption TBD • Update Chip Arcchitecture. - P.7 – DVDD, DVDDM • Update Recommended Power Sequence. - P.17 – DVDD, DVDDM • Update DC characteristics. - P.52~53 – DVDD, DVDDM – IDDD, IDDS TBD	Jaedong Park
0.2	02/02/2021	• Update General Description. - P.6 – Power consumption – Operating temp. • Update DC characteristics. - P.52~53 – IDDD, IDDS	Jaedong Park
0.3	20/04/2021	• Update Features. - P.5 • Update General Description. - P.6 • Update Chip Architecture. - P.7 • Update MIPI - P.40~44 • Update Register Map. - P.57, P65~66 – Deleted mipi 4-lane. • Update General Description. - P.6 – Dark signal – Power consumption • Update DC characteristics. - P.51 – IDDD, IDDS	Jaedong Park
0.4	01/06/2021	• Update DC characteristics. - P.51 – DVDD, DVDDM	Jaedong Park