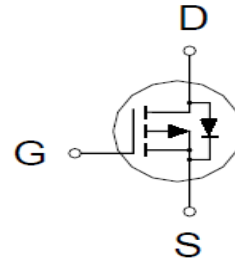
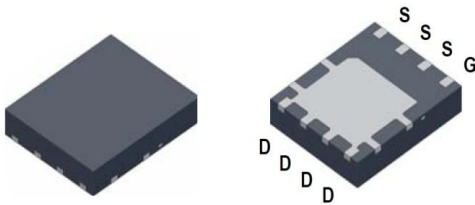


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PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	14m Ω @ $V_{GS} = -10V$	-31A



PDFN 5X6P

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	-31	A
	$T_C = 100\text{ }^\circ\text{C}$		-20	
	$T_A = 25\text{ }^\circ\text{C}$		-10	
	$T_A = 70\text{ }^\circ\text{C}$		-7.8	
Pulsed Drain Current ¹		I_{DM}	-90	
Avalanche Current		I_{AS}	-30	
Avalanche Energy	L=0.1mH	E_{AS}	45	mJ
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	25	W
	$T_C = 100\text{ }^\circ\text{C}$		10	
	$T_A = 25\text{ }^\circ\text{C}$		2.4	
	$T_A = 70\text{ }^\circ\text{C}$		1.5	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		52	$^\circ\text{C} / \text{W}$
Junction-to-Case	$R_{\theta JC}$		5	

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

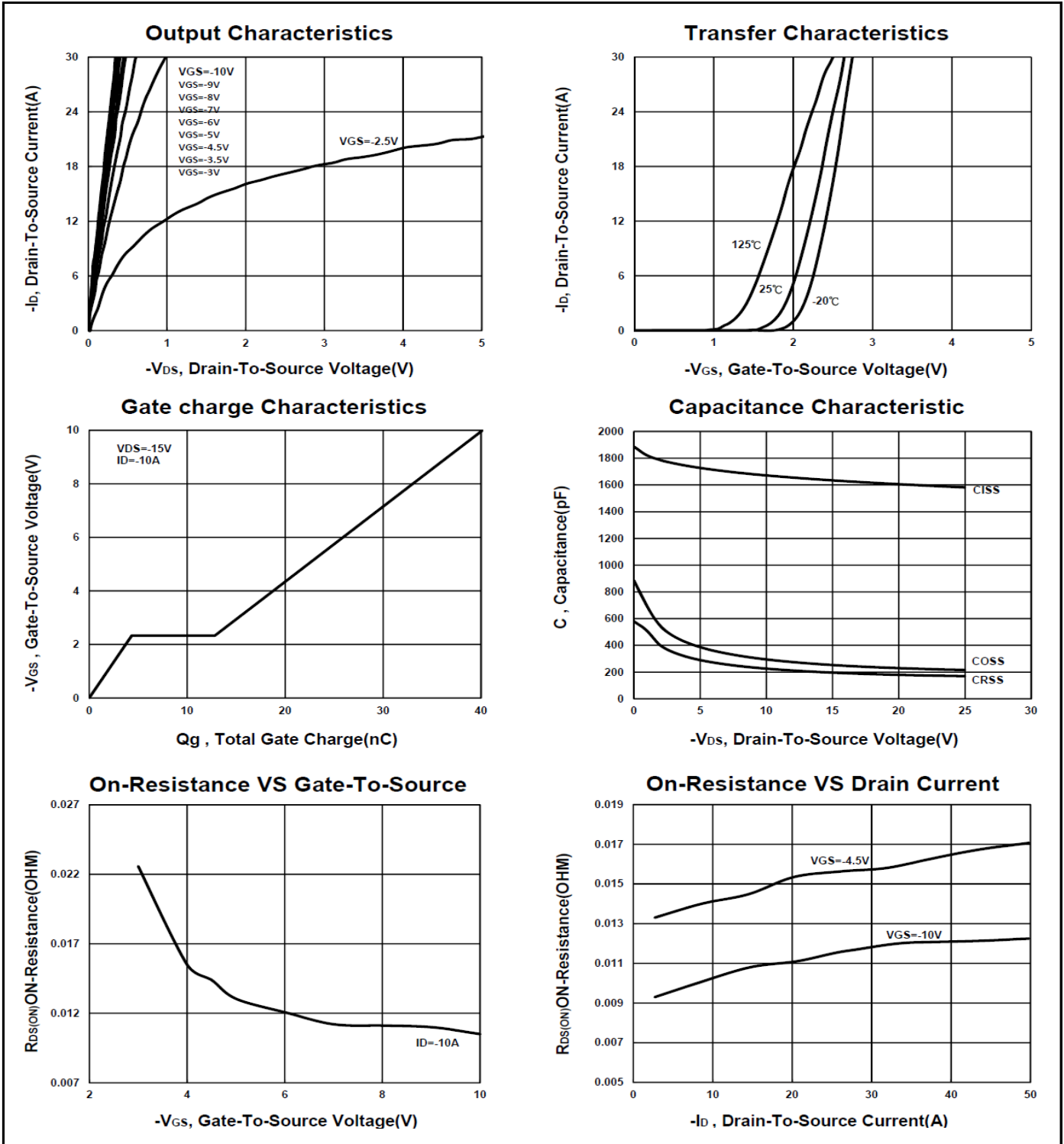
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.1	-1.6	-2.1	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±25V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			-1	μA
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C			-10	
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -9A		16	22	mΩ
		V _{GS} = -10V, I _D = -10A		12.2	14	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -10A		30		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		1730		pF
Output Capacitance	C _{oss}			252		
Reverse Transfer Capacitance	C _{rss}			198		
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		4.2		Ω
Total Gate Charge ²	Q _g	V _{DS} = -15V, I _D = -10A	V _{GS} = -10V		34	nC
			V _{GS} = -4.5V		17.3	
Gate-Source Charge ²	Q _{gs}				5	
Gate-Drain Charge ²	Q _{gd}				7.8	
Turn-On Delay Time ²	t _{d(on)}		V _{DS} = -15V, I _D ≅ -1A, V _{GS} = -10V, R _{GS} = 6Ω		25	nS
Rise Time ²	t _r				26	
Turn-Off Delay Time ²	t _{d(off)}			75		
Fall Time ²	t _f			46		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I _S				-20	A
Forward Voltage ¹	V _{SD}	I _F = -10A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = -10A, di _F /dt = 100A / μS		16		nS
Reverse Recovery Charge	Q _{rr}				5	

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

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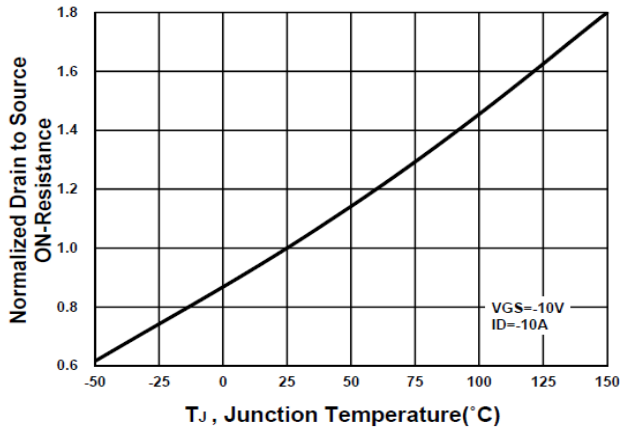
P-Channel Logic Level Enhancement Mode MOSFET



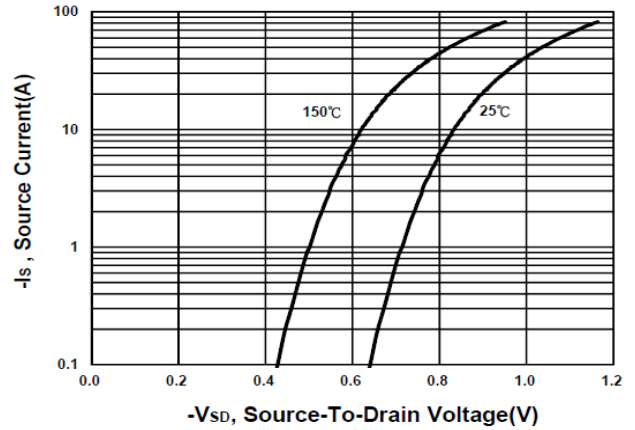
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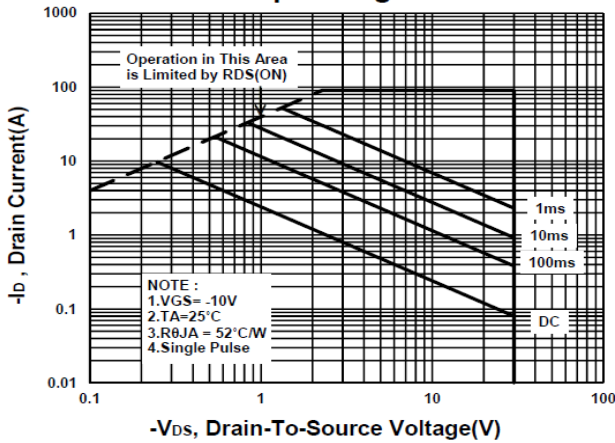
On-Resistance VS Temperature



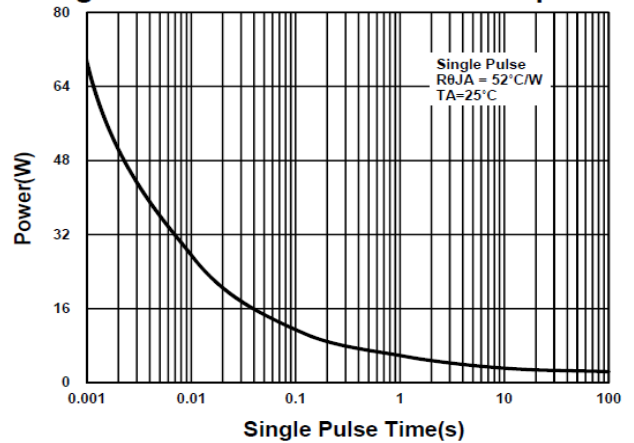
Source-Drain Diode Forward Voltage



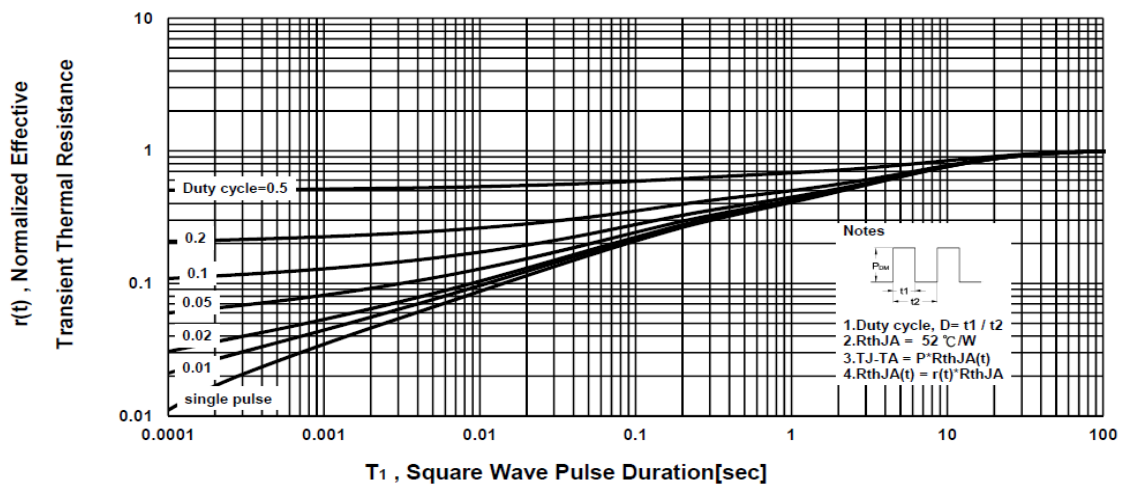
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

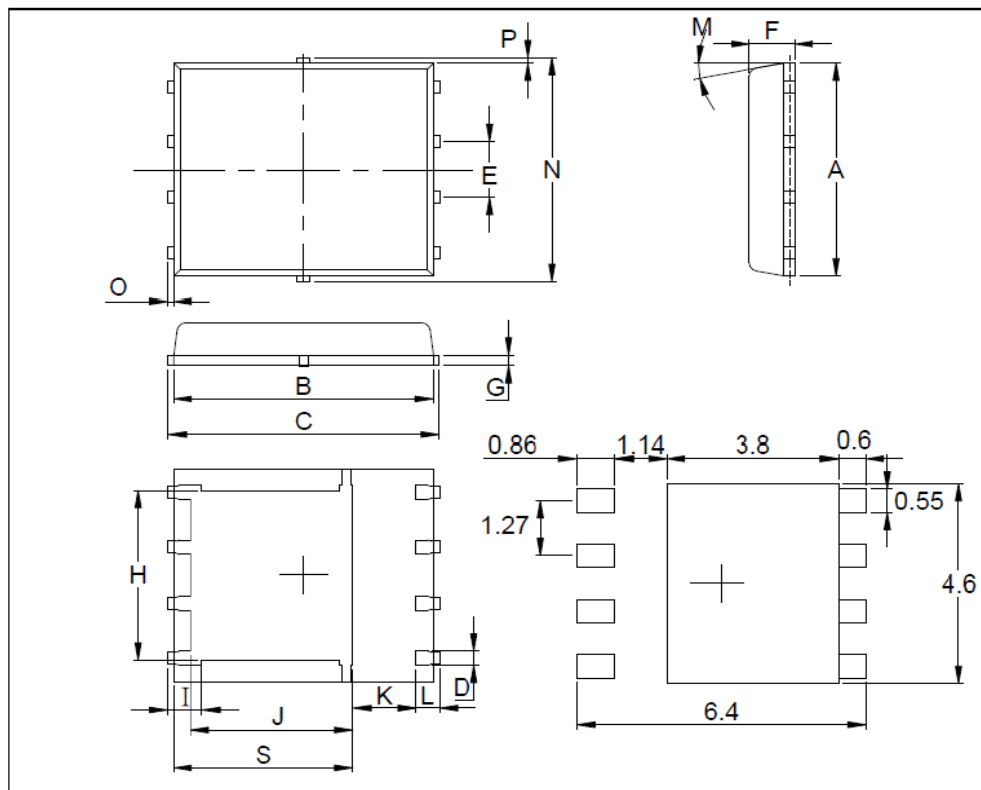


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PDFN 5x6P MECHANICAL DATA

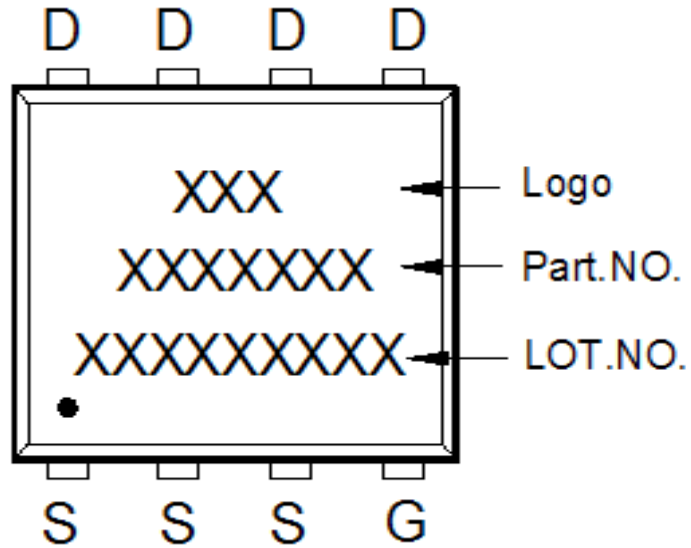
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8		5.15	J	3.33		3.78
B	5.44		5.9	K	0.9		
C	5.9		6.35	L	0.35		0.712
D	0.33		0.51	M	0°		12°
E		1.27		N	4.8		5.5
F	0.8		1.25	O	0.05		0.3
G	0.15		0.34	P	0.06		0.2
H	3.61		4.31	S	3.69		4.19
I	0.35		0.71				



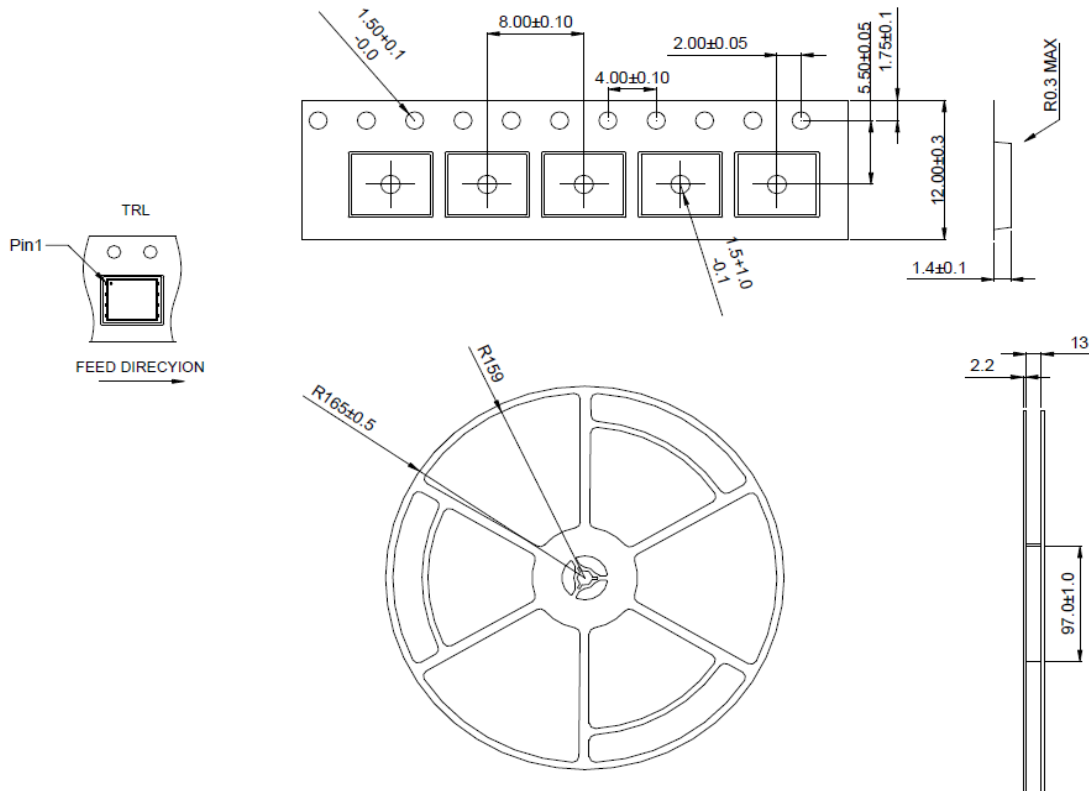
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A. Marking Information



B. Tape & Reel Information: 3000pcs/Reel

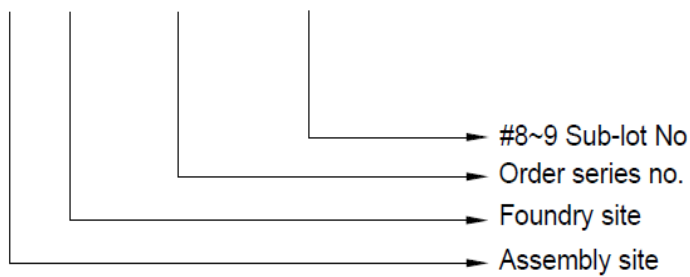


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C. Lot.No. & Date Code rule

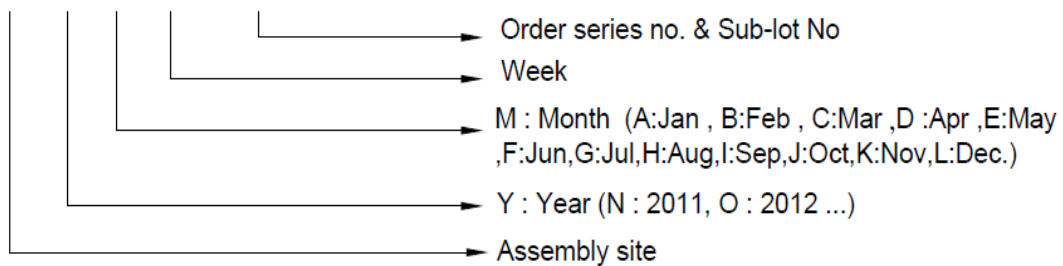
1.LOT.NO.

M N 15M21 03



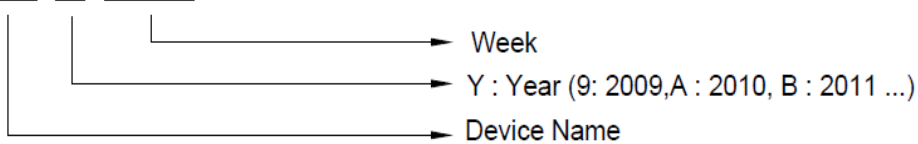
2.Date Code

D Y M X XXX



3.Date Code (for Small package)

XX Y WW





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D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文"0"和数字"0", "G"和"Q"的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert " / " between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least