UNIKC Semiconductor

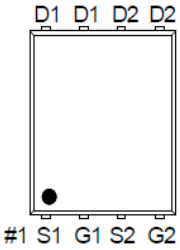
RoHS Compliant

PK552DX

Dual N-Channel Enhancement Mode MOSFET

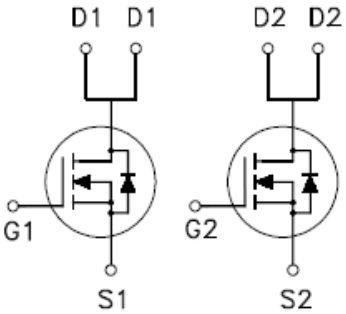
PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
20V	5.7mΩ @V_{GS} = 4.5V	56A



PDFN 5*6P

G. GATE
D. DRAIN
S. SOURCE



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current[3]	T_C = 25 °C	I_D	56	A
	T_C = 100 °C		36	
Pulsed Drain Current[1]		I_{DM}	70	
Continuous Drain Current	T_A = 25 °C	I_D	17	
	T_A = 70 °C		14	
Avalanche Current		I_{AS}	40	
Avalanche Energy	L = 0.1mH	E_{AS}	79	mJ
Power Dissipation	T_C = 25 °C	P_D	31	W
	T_C = 100 °C		12.5	
Power Dissipation	T_A = 25 °C	P_D	2.9	
	T_A = 70 °C		1.8	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		4	°C / W
Junction-to-Ambient[2]	$R_{\theta JA}$		43	

[1]Pulse width limited by maximum junction temperature.

[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[3]Package limitation current is 22A.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.3	0.7	1	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V ,			1	μA
		V_{DS} = 10V, V_{GS} = 0V , T_J = 70 °C			10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 17A		4.4	5.7	mΩ
		V_{GS} = 2.5V, I_D = 17A		4.9	6.2	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 17A		100		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		4120		pF
Output Capacitance	C_{oss}			481		
Reverse Transfer Capacitance	C_{rss}			409		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		1		Ω
Total Gate Charge[2]	Q_g V_{GS}=2.5V	V_{DS} = 10V, I_D = 17A		28.8		nC
	Q_g V_{GS}=4.5V			48.2		
Gate-Source Charge[2]	Q_{gs}			6		
Gate-Drain Charge[2]	Q_{gd}			14		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = 10V, I_D ≅ 17A, V_{GS}= 4.5V, R_{GEN}= 6Ω		20		nS
Rise Time[2]	t_r			25		
Turn-Off Delay Time[2]	$t_{d(off)}$			180		
Fall Time[2]	t_f			85		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current[3]	I_S				24	A
Forward Voltage[1]	V_{SD}	I_F = 17A, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 17A, dI_F/dt = 100A /μS		25		nS
Reverse Recovery Charge	Q_{rr}			14		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Package limitation current is 22A.

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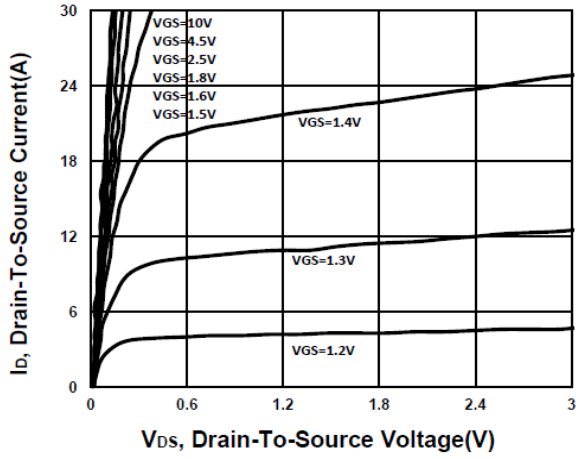
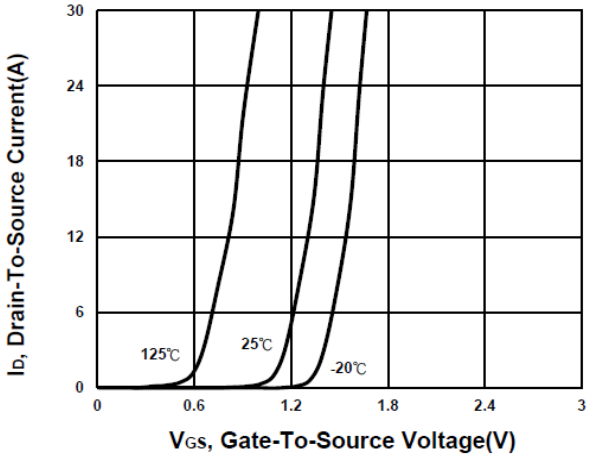
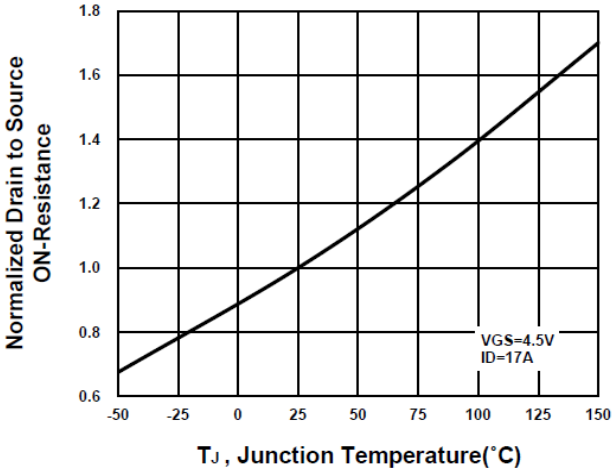
Output Characteristics



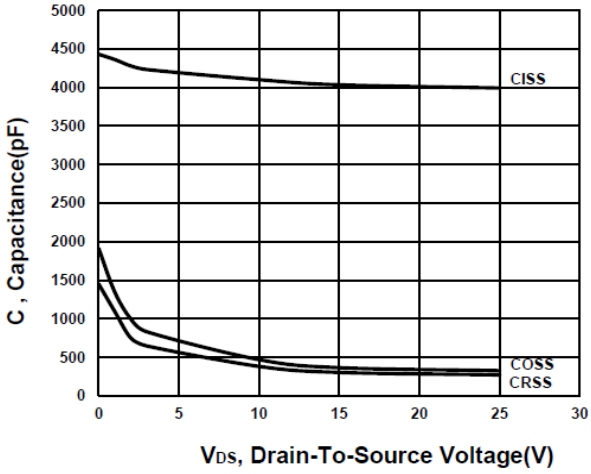
Transfer Characteristics



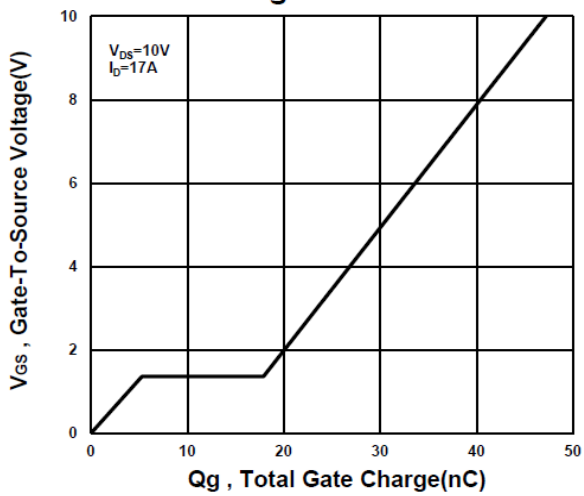
On-Resistance VS Temperature



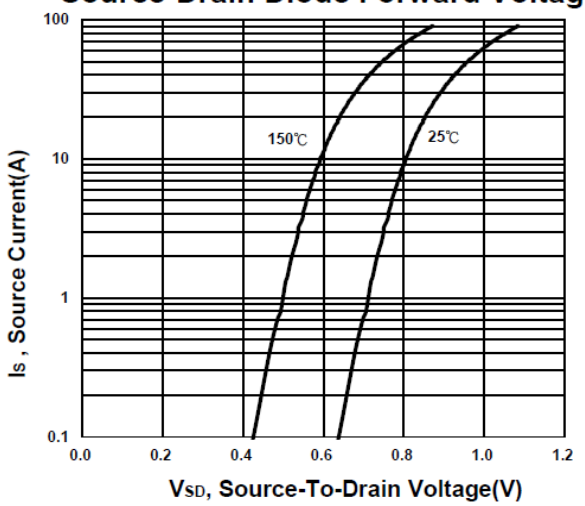
Capacitance Characteristic



Gate charge Characteristics



Source-Drain Diode Forward Voltage



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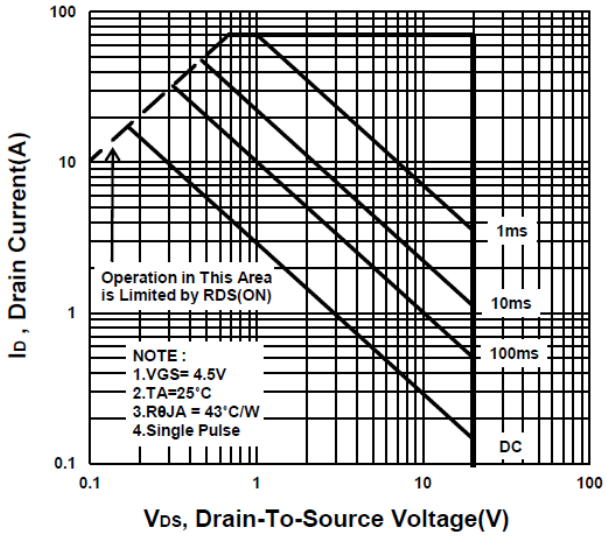
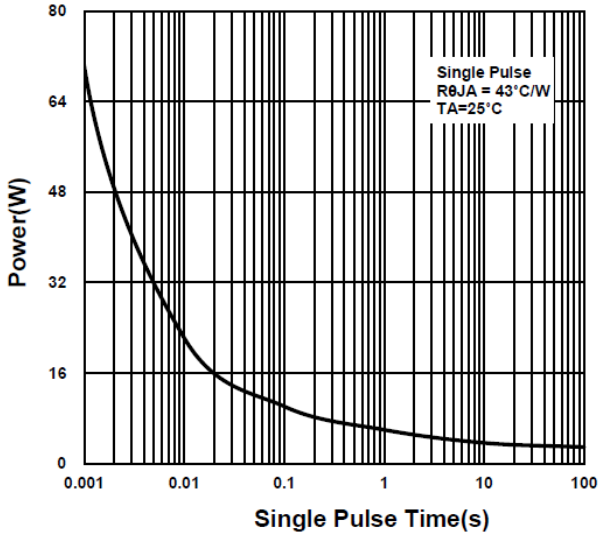
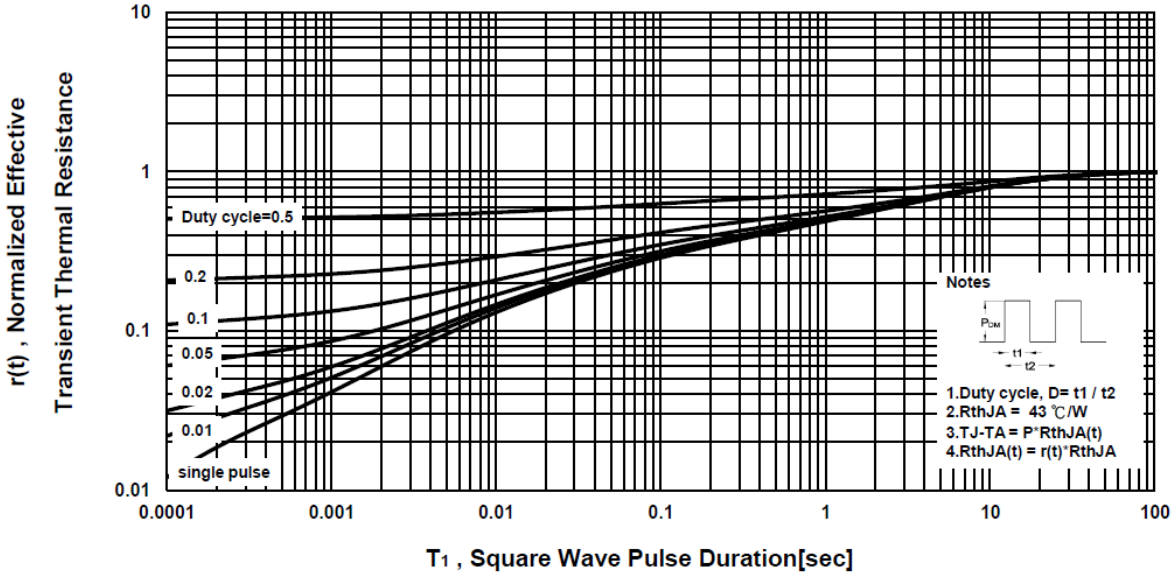
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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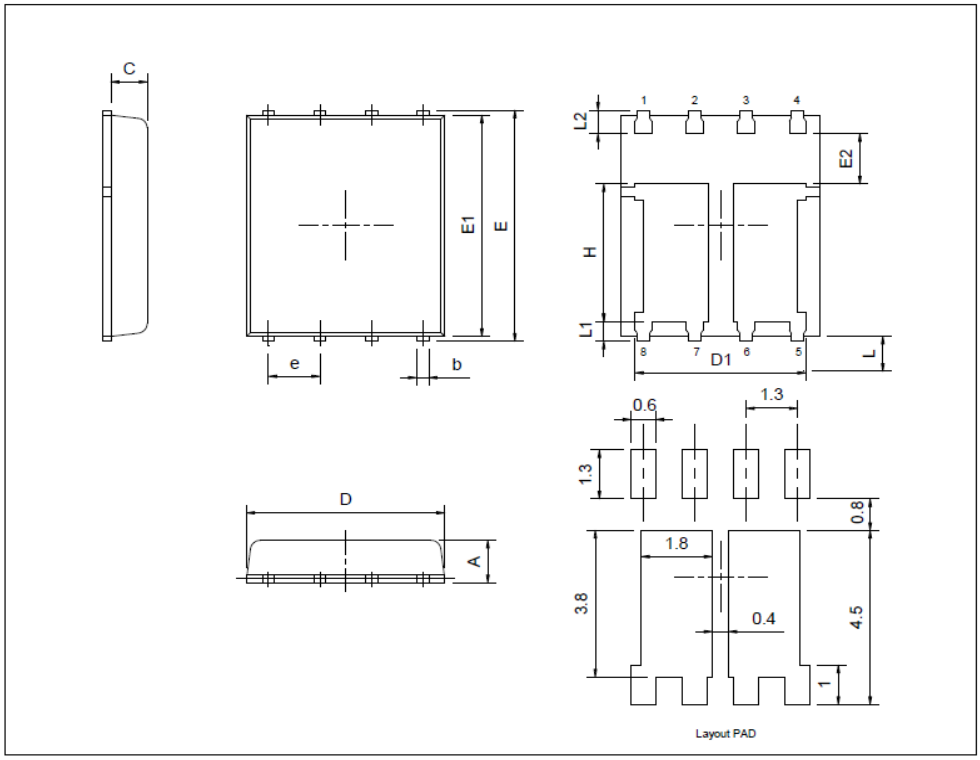
Package Dimension

PDFN 5x6P(左右 Dual) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.9		1.17	L	0.05		0.25
b	0.33		0.51	L1	0.38		0.61
C	0.7		0.97	L2	0.38		0.71
D	4.8		5.0	H	3.38		3.78
D1	3.61		4.31				
E	5.9		6.15				
E1	5.65		5.85				
E2	1.1						
e		1.27					



*散热片形状会因为封装厂框架不同而有所差异。