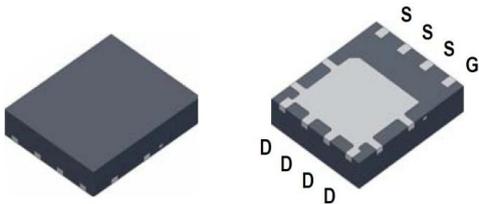


# PK555BA

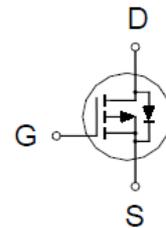
## P-Channel Logic Level Enhancement Mode MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
-30V	28m $\Omega$ @ $V_{GS} = -10V$	-19A



PDFN 5x6P



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		$V_{DS}$	-30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	-19	A
	$T_C = 100\text{ }^\circ\text{C}$		-12	
	$T_A = 25\text{ }^\circ\text{C}$		-7.8	
	$T_A = 70\text{ }^\circ\text{C}$		-6.2	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	-50	
Avalanche Current		$I_{AS}$	-19.3	
Avalanche Energy	L = 0.1mH	$E_{AS}$	18.6	mJ
Power Dissipation <sup>3</sup>	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	19	W
	$T_C = 100\text{ }^\circ\text{C}$		7.9	
	$T_A = 25\text{ }^\circ\text{C}$		3.1	
	$T_A = 70\text{ }^\circ\text{C}$		2	
Operating Junction & Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

# PK555BA

## P-Channel Logic Level Enhancement Mode MOSFET

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient <sup>2</sup>	t ≤ 10s	R <sub>θJA</sub>		40	°C / W
	Steady-State	R <sub>θJA</sub>		63	
Junction-to-Case	Steady-State	R <sub>θJC</sub>		6.3	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> = 25°C. The value in any given application depends on the user's specific board design.

<sup>3</sup>The Power dissipation is based on R<sub>θJA</sub> t ≤ 10s value.

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-0.8	-1.5	-2.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V			-1	uA
		V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			-10	
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -6A		16	28	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -6A		26	45	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -6A		22		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -15V, f = 1MHz		963		pF
Output Capacitance	C <sub>oss</sub>			134		
Reverse Transfer Capacitance	C <sub>rss</sub>			118		
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1MHz		10		Ω
Total Gate Charge <sup>2</sup>	Q <sub>g(VGS=-10V)</sub>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -6A		22		nC
	Q <sub>g(VGS=-4.5V)</sub>			10.8		
Gate-Source Charge <sup>2</sup>	Q <sub>gs</sub>			2.4		
Gate-Drain Charge <sup>2</sup>	Q <sub>gd</sub>			5.4		
Turn-On Delay Time <sup>2</sup>	t <sub>d(on)</sub>		V <sub>DS</sub> = -15V, I <sub>D</sub> ≅ -6A, V <sub>GS</sub> = -10V, R <sub>GS</sub> = 6Ω		16	
Rise Time <sup>2</sup>	t <sub>r</sub>			18		
Turn-Off Delay Time <sup>2</sup>	t <sub>d(off)</sub>			40		
Fall Time <sup>2</sup>	t <sub>f</sub>			26		

## **PK555BA**

### **P-Channel Logic Level Enhancement Mode MOSFET**

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>J</sub> = 25 °C)**

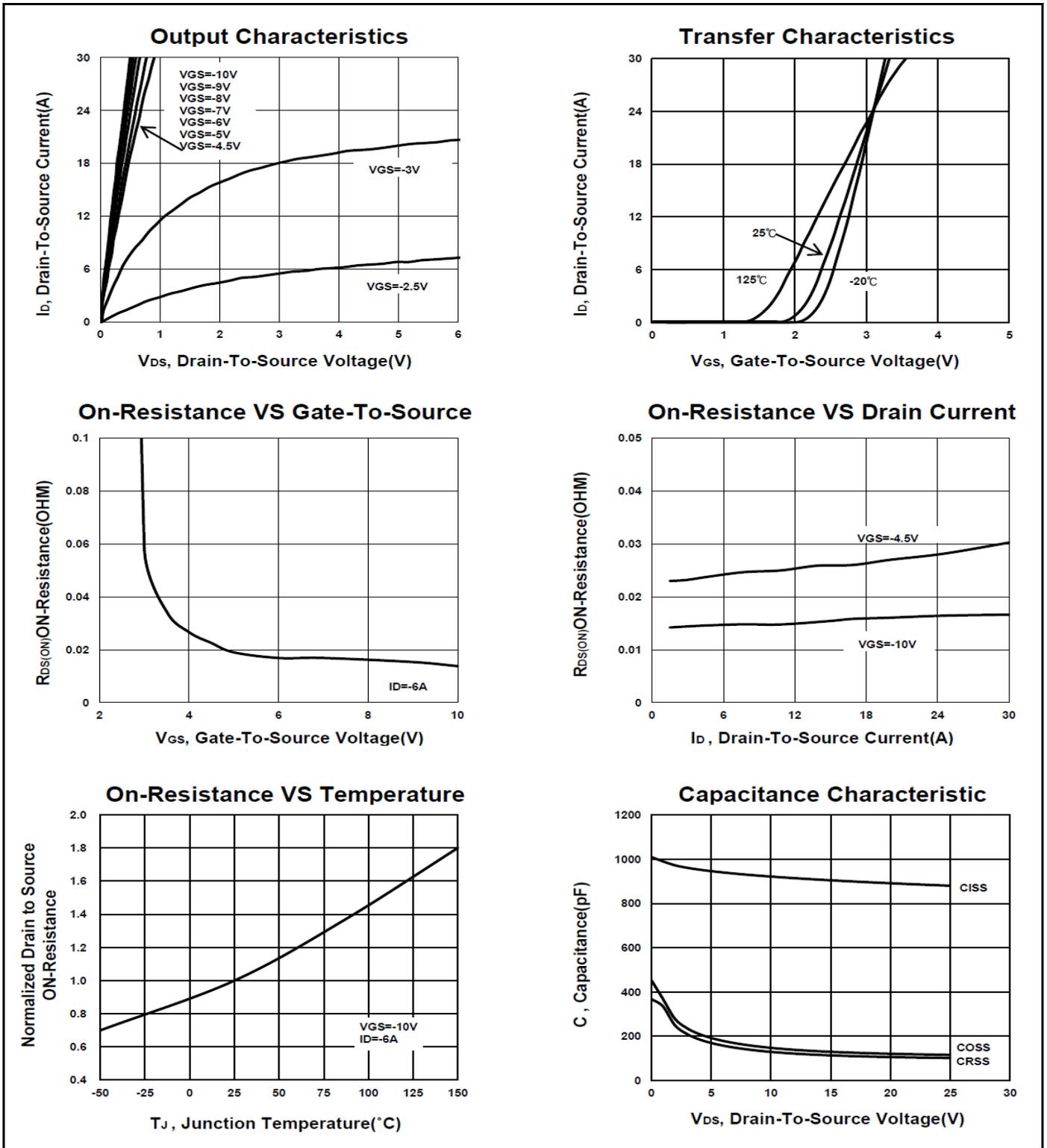
Continuous Current	I <sub>S</sub>				-20	A
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = -6A, V <sub>GS</sub> = 0V			-1	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -6A, dI <sub>F</sub> /dt = 100A / μS		11		nS
Reverse Recovery Charge	Q <sub>rr</sub>			3.3		nC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

# PK555BA

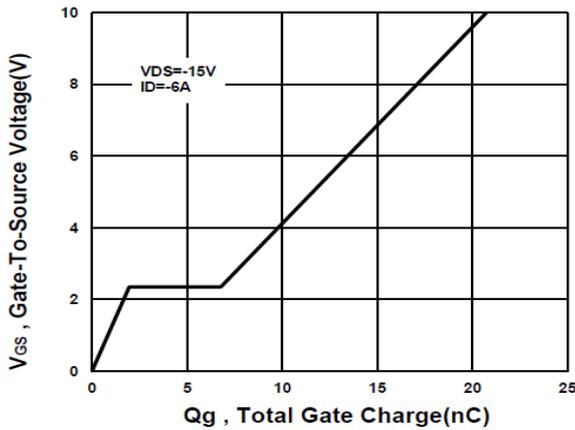
## P-Channel Logic Level Enhancement Mode MOSFET



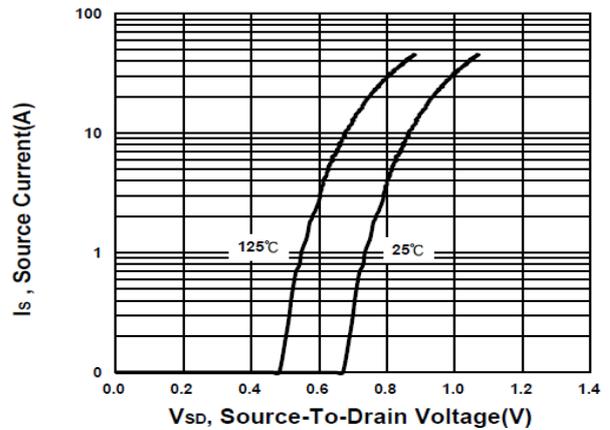
# PK555BA

## P-Channel Logic Level Enhancement Mode MOSFET

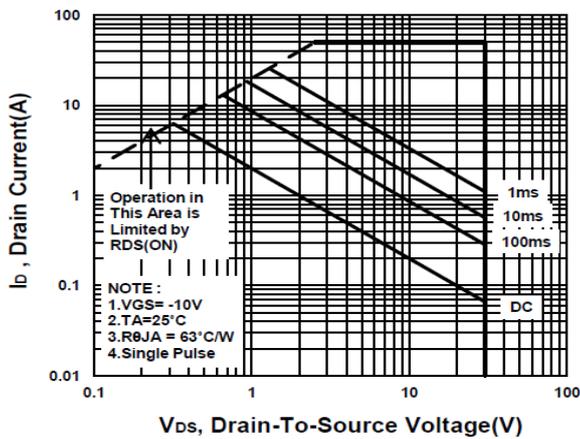
**Gate charge Characteristics**



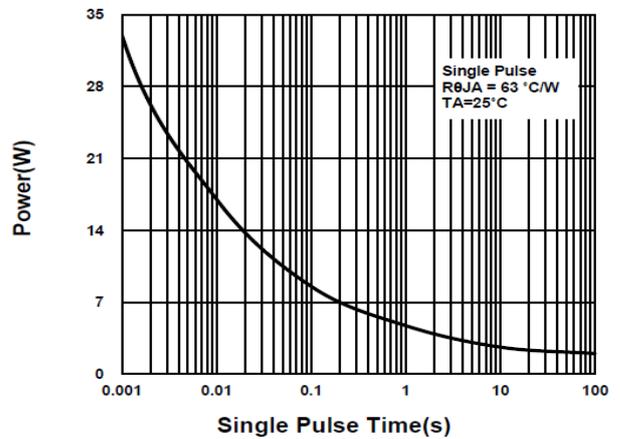
**Source-Drain Diode Forward Voltage**



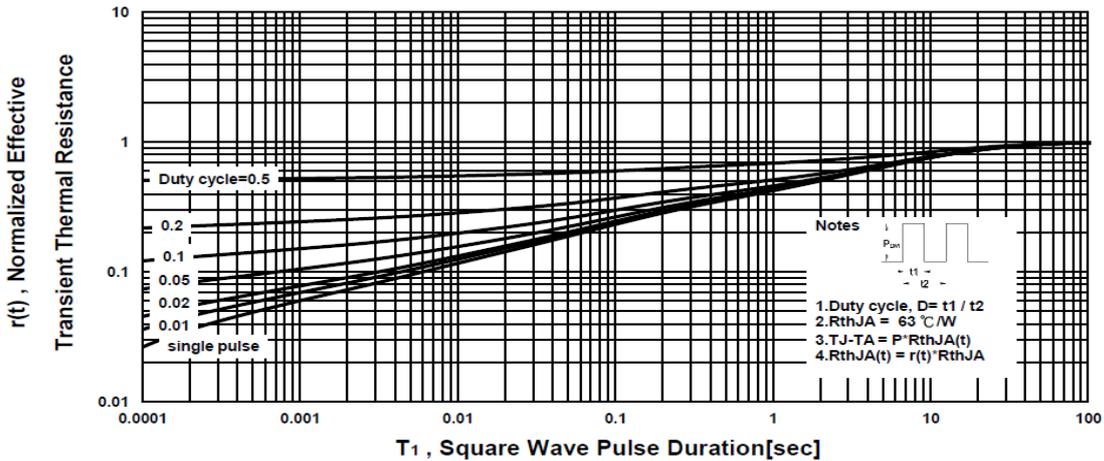
**Safe Operating Area**



**Single Pulse Maximum Power Dissipation**



**Transient Thermal Response Curve**



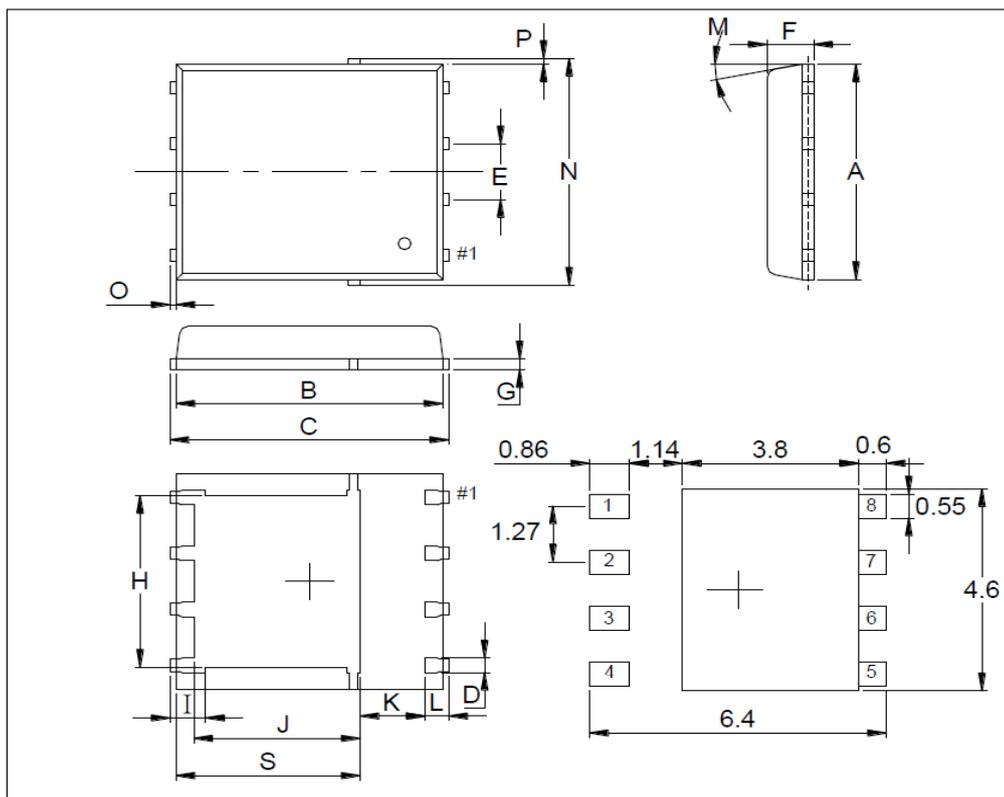
# PK555BA

## P-Channel Logic Level Enhancement Mode MOSFET

### Package Dimension

### PDFN 5x6P MECHANICAL DATA

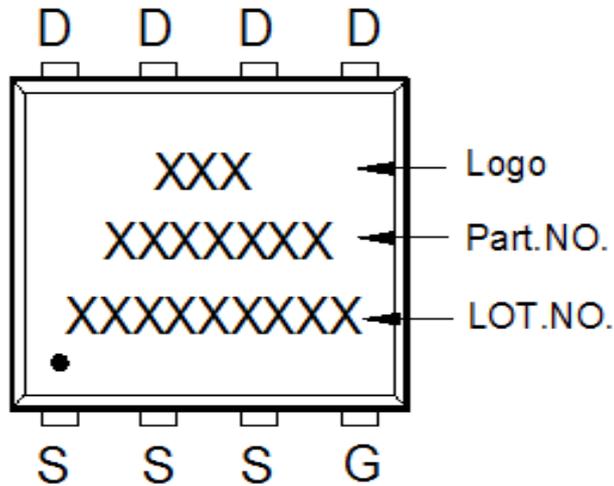
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8		5.15	J	3.34		3.9
B	5.42		5.9	K	0.9		
C	5.9		6.35	L	0.38		0.711
D	0.3		0.51	M	0°		12°
E	1.17	1.27	1.37	N	4.8		5.4
F	0.8	1	1.2	O	0.05		0.36
G	0.15		0.35	P	0.05		0.25
H	3.67		4.31	S	3.73		4.19
I	0.38		0.71				



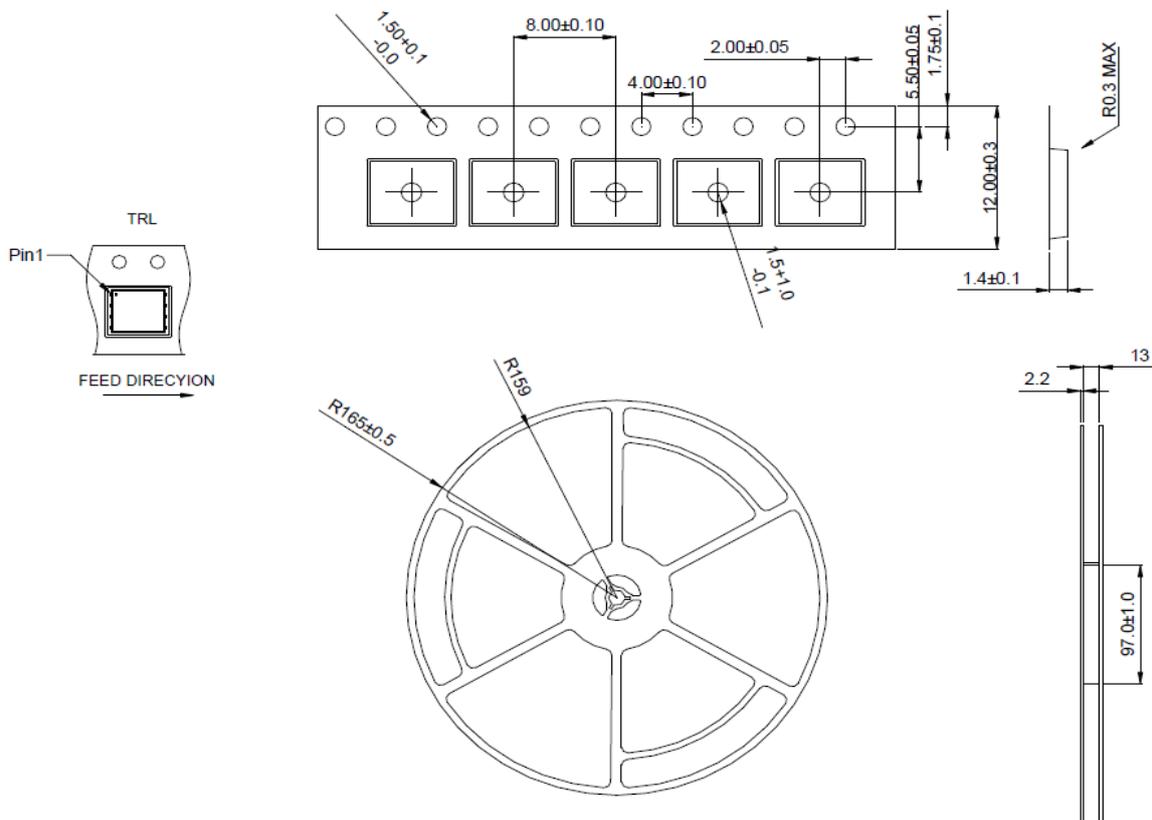
# PK555BA

## P-Channel Logic Level Enhancement Mode MOSFET

### A. Marking Information



### B. Tape & Reel Information: 3000pcs/Reel

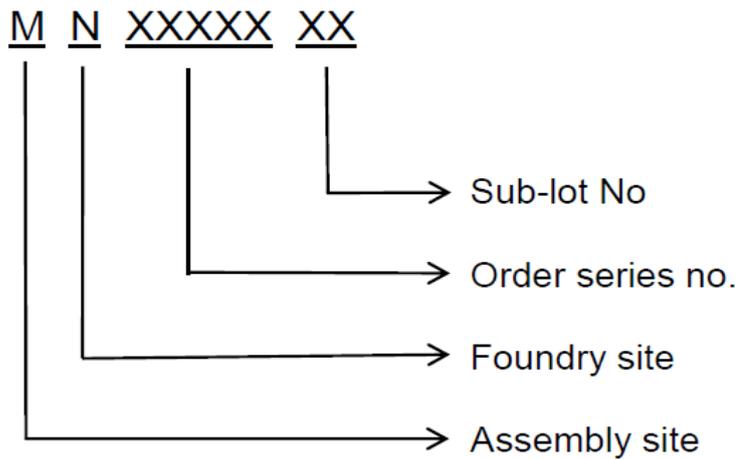


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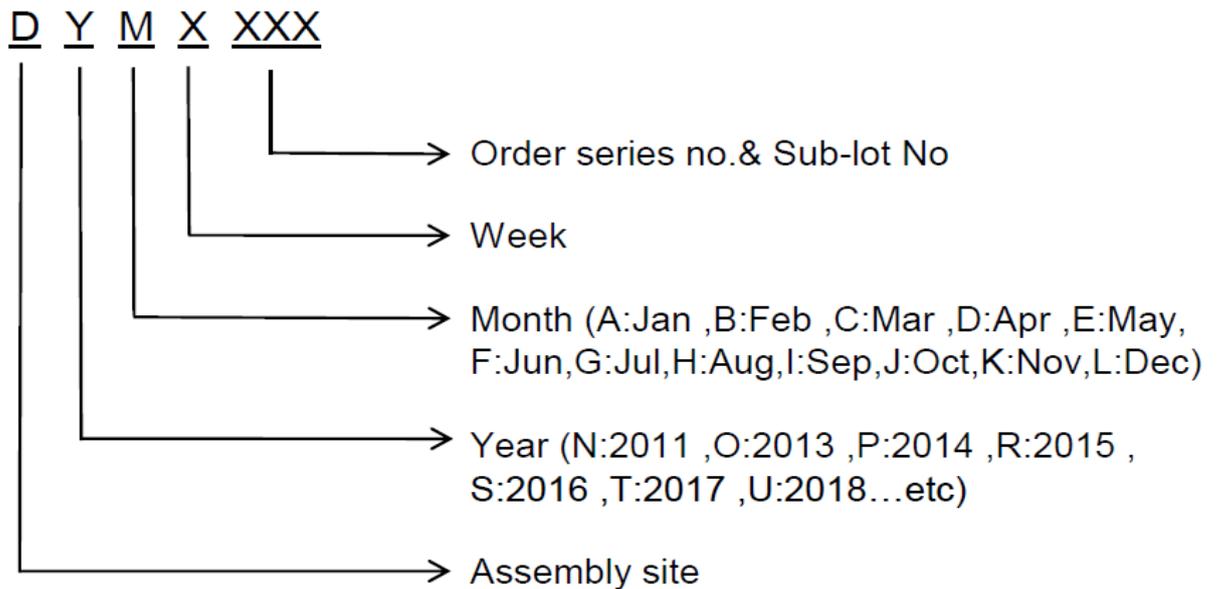
## P-Channel Logic Level Enhancement Mode MOSFET

### C. Lot No.&Date Code rule

#### 1.Lot No.



#### 2.Date Code



# PK555BA

## P-Channel Logic Level Enhancement Mode MOSFET

### D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文"0"和数字"0", "G"和"Q"的字型即可)
3	U-NIKC	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	RoHS label	 long axis: 12 mm minor axis: 6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert "/" between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least