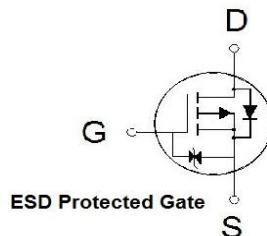


**NIKO-SEM****P-Channel Logic Level Enhancement Mode  
Field Effect Transistor****PK5G3EA  
PDFN 5x6P  
Halogen-Free & Lead-Free****PRODUCT SUMMARY**

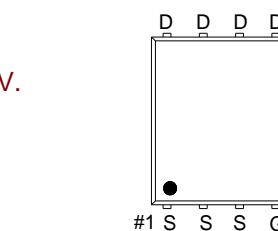
$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$
-30V	6.1mΩ	-68A

**Features**

- Pb-Free, Halogen Free and RoHS compliant.
- Low  $R_{DS(on)}$  to Minimize Conduction Losses.
- Ohmic Region Good  $R_{DS(on)}$  Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- Products Integrated ESD diode with ESD Protected up to 4KV.

**Applications**

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.



G. GATE  
D. DRAIN  
S. SOURCE

100% UIS Tested  
100% Rg Tested

**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$  Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$I_D$	-68	A
		-43	
		-15	
		-12	
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	-150	
Avalanche Current	$I_{AS}$	-68	
Avalanche Energy	$E_{AS}$	231	mJ
Power Dissipation	$P_D$	48	W
		19	
		2.3	
		1.5	
Operating Junction & Storage Temperature Range	$T_j, T_{stg}$	-55 to 150	°C

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient <sup>2</sup>	$R_{\theta JA}$	55	°C / W	
Junction-to-Case	$R_{\theta JC}$			

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ C$ . The value in any given application depends on the user's specific board design.

**NIKO-SEM****P-Channel Logic Level Enhancement Mode  
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PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-30			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1.3	-1.7	-2.3	
Gate-Body Leakage	$I_{\text{GSS}}$	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$			$\pm 10$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = -24\text{V}, V_{\text{GS}} = 0\text{V}$			-1	
		$V_{\text{DS}} = -20\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			-10	$\mu\text{A}$
Drain-Source On-State Resistance <sup>1</sup>	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = -4.5\text{V}, I_D = -20\text{A}$		6.5	10.5	
		$V_{\text{GS}} = -10\text{V}, I_D = -20\text{A}$		4.1	6.1	$\text{m}\Omega$
Forward Transconductance <sup>1</sup>	$g_{\text{fs}}$	$V_{\text{DS}} = -5\text{V}, I_D = -20\text{A}$		55		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -15\text{V}, f = 1\text{MHz}$		4924		pF
Output Capacitance	$C_{\text{oss}}$			795		
Reverse Transfer Capacitance	$C_{\text{rss}}$			715		
Gate Resistance	$R_g$	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		1.9		$\Omega$
Total Gate Charge <sup>2</sup>	$Q_{\text{g}(\text{VGS}=-10\text{V})}$	$V_{\text{DS}} = -15\text{V}, I_D = -20\text{A}$		120		nC
	$Q_{\text{g}(\text{VGS}=-4.5\text{V})}$			60		
Gate-Source Charge <sup>2</sup>	$Q_{\text{gs}}$			13		
Gate-Drain Charge <sup>2</sup>	$Q_{\text{gd}}$			28		
Turn-On Delay Time <sup>2</sup>	$t_{\text{d}(\text{on})}$	$V_{\text{DS}} = -15\text{V}, I_D \approx -20\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GS}} = 6\Omega$		18		nS
Rise Time <sup>2</sup>	$t_r$			96		
Turn-Off Delay Time <sup>2</sup>	$t_{\text{d}(\text{off})}$			162		
Fall Time <sup>2</sup>	$t_f$			126		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_J = 25^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				-37	A
Forward Voltage <sup>1</sup>	$V_{\text{SD}}$	$I_F = -20\text{A}, V_{\text{GS}} = 0\text{V}$			-1.3	V
Reverse Recovery Time	$t_{\text{rr}}$	$I_F = -20\text{A}, dI_F/dt = 100\text{ A / } \mu\text{s}$		17		nS
Reverse Recovery Charge	$Q_{\text{rr}}$			6.8		nC

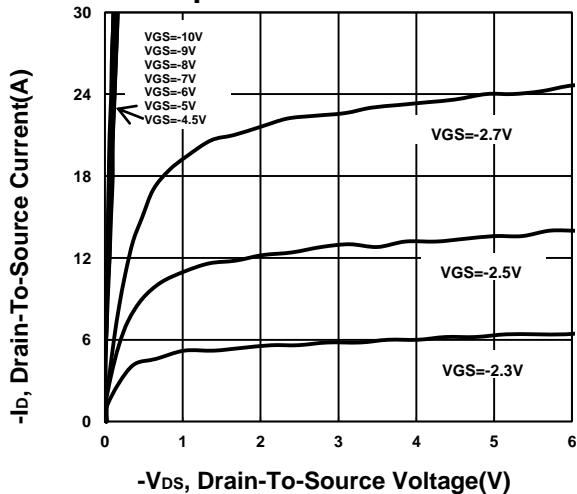
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\text{ }\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .<sup>2</sup>Independent of operating temperature.

**NIKO-SEM**

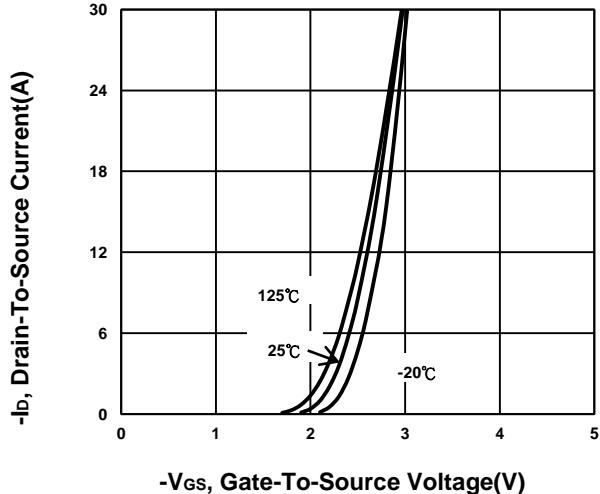
**P-Channel Logic Level Enhancement Mode  
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**PK5G3EA**  
**PDFN 5x6P**  
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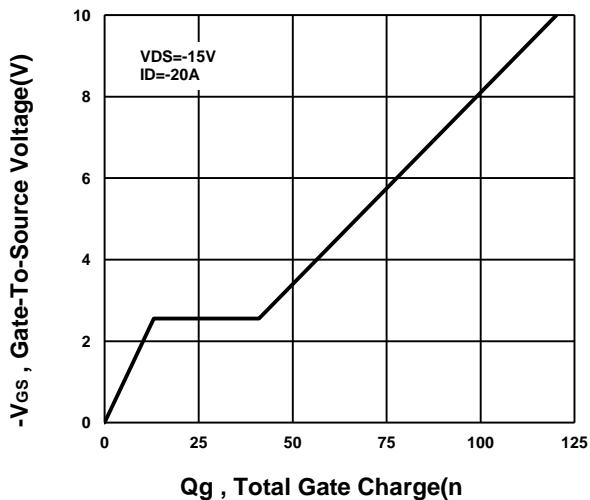
### Output Characteristics



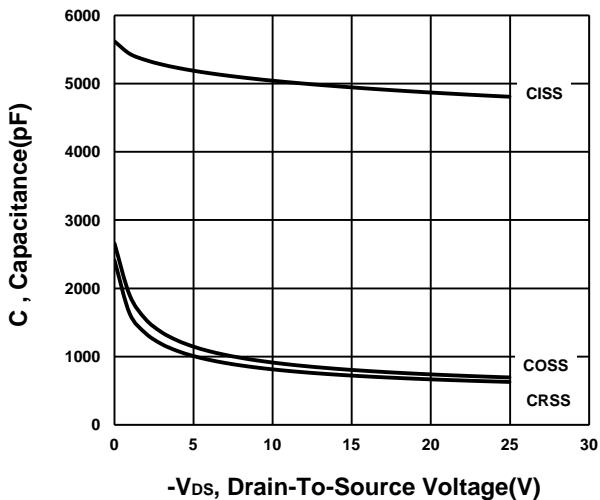
### Transfer Characteristics



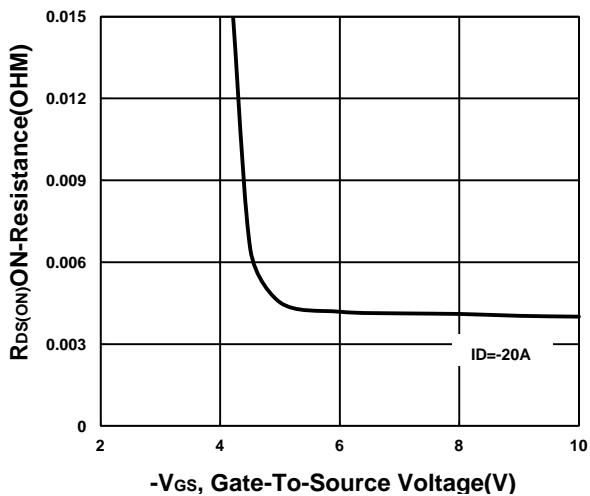
### Gate charge Characteristics



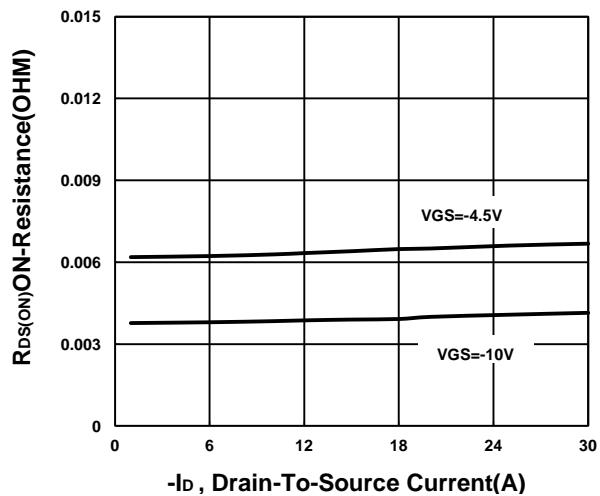
### Capacitance Characteristic

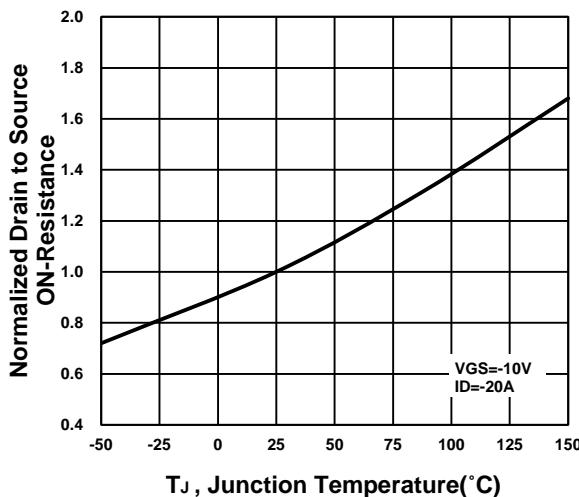
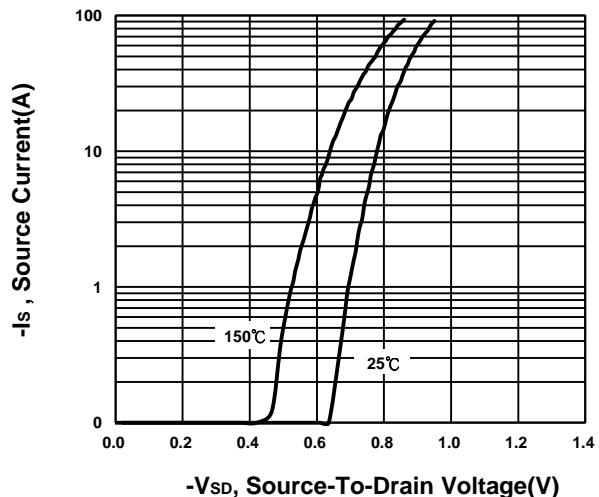
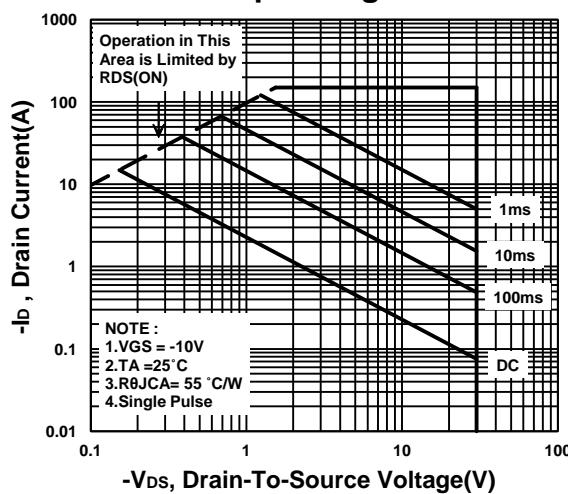
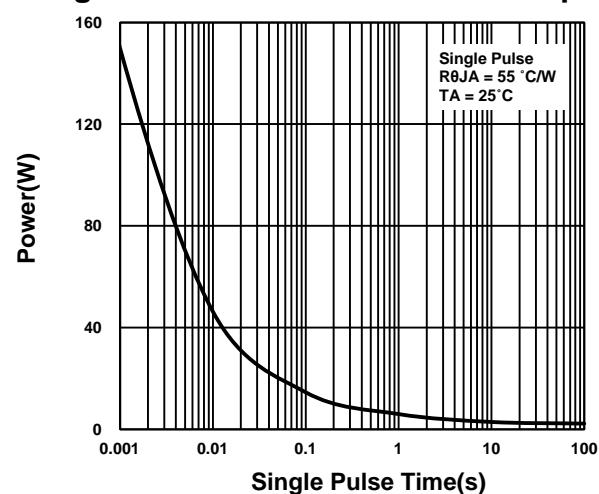
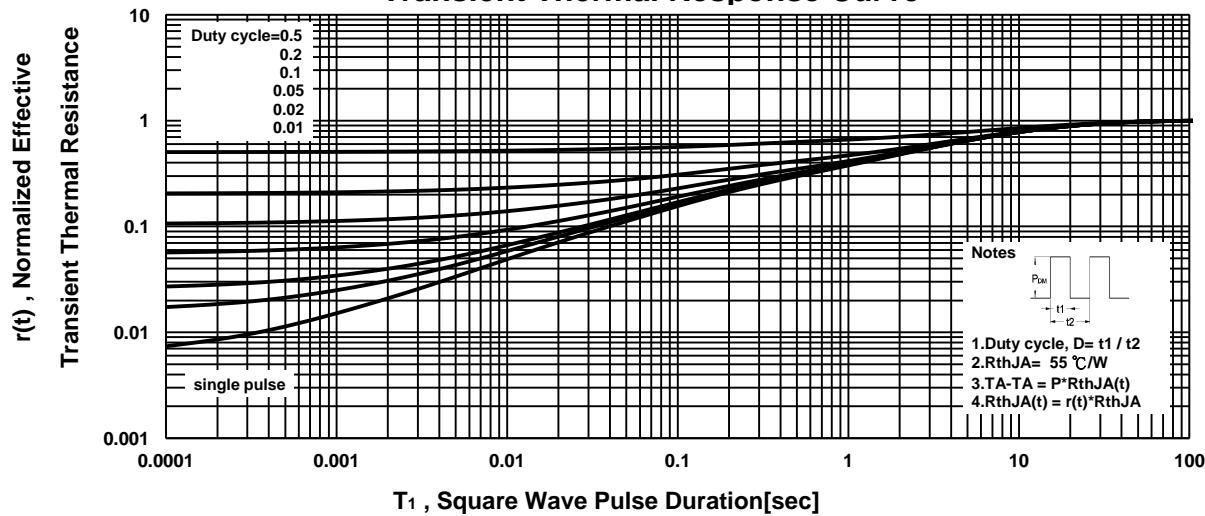


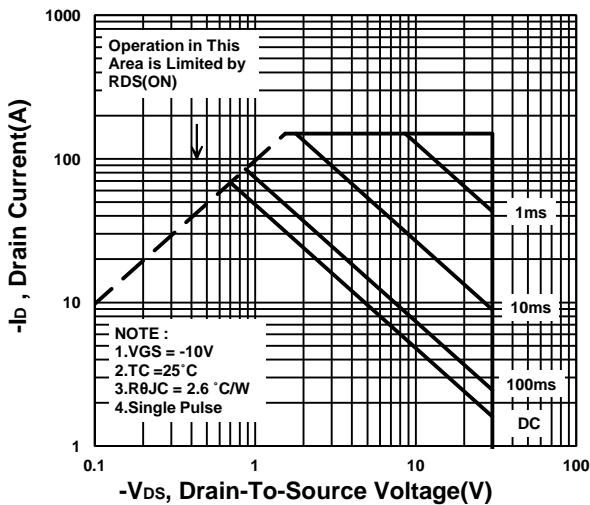
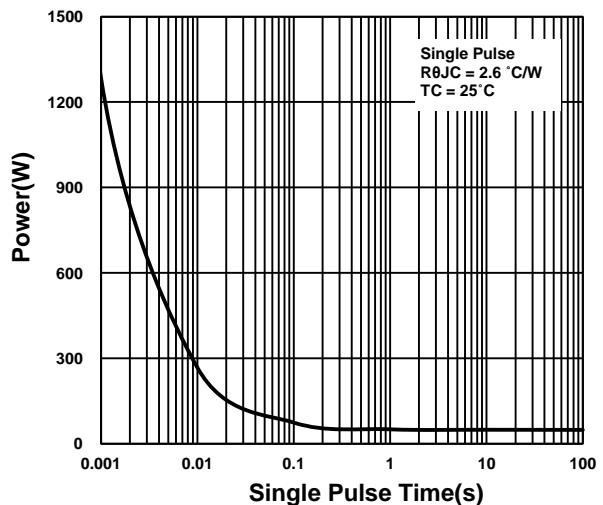
### On-Resistance VS Gate-To-Source



### On-Resistance VS Drain Current



**NIKO-SEM****P-Channel Logic Level Enhancement Mode  
Field Effect Transistor****PK5G3EA  
PDFN 5x6P  
Halogen-Free & Lead-Free****On-Resistance VS Temperature****Source-Drain Diode Forward Voltage****Safe Operating Area****Single Pulse Maximum Power Dissipation****Transient Thermal Response Curve**

**Safe Operating Area****Single Pulse Maximum Power Dissipation****Transient Thermal Response Curve**