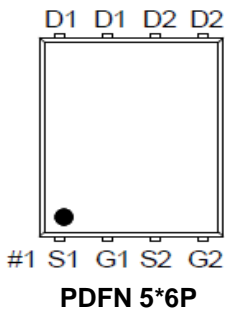


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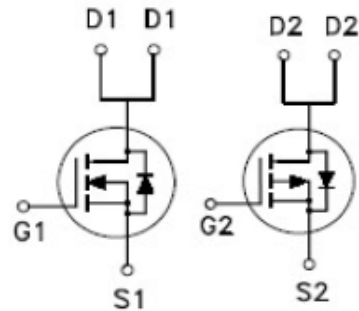
N & P-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D	CH.
-30V	28m Ω @ $V_{GS} = -10V$	-22A	Q2
30V	22m Ω @ $V_{GS} = 10V$	23A	Q1



100% UIS Tested
100% Rg Tested



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	CH.	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	Q2	-30	V
			Q1	30	
Gate-Source Voltage		V_{GS}	Q2	± 20	V
			Q1	± 20	
Continuous Drain Current ³	$T_C = 25\text{ }^\circ\text{C}$	I_D	Q2	-22	A
			Q1	23	
	$T_C = 100\text{ }^\circ\text{C}$		Q2	-14	
			Q1	14	
Pulsed Drain Current ¹		I_{DM}	Q2	-45	A
			Q1	50	
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	I_D	Q2	-7.8	A
			Q1	8.6	
	$T_A = 70\text{ }^\circ\text{C}$		Q2	-6.3	
			Q1	6.9	
Avalanche Current		I_{AS}	Q2	-19	A
			Q1	12	
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	Q2	18	mJ
			Q1	7.3	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	Q2	25	W
			Q1	22	
	$T_C = 100\text{ }^\circ\text{C}$		Q2	10	
			Q1	9	

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Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	Q2	3	W
	$T_A = 70\text{ }^\circ\text{C}$		Q1	3	
			Q2	2	
			Q1	2	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	CH.	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$t \leq 10\text{ s}$	$R_{\theta JA}$	Q2		40	$^\circ\text{C} / \text{W}$
	Steady-State				57	
Junction-to-Ambient ²	$t \leq 10\text{ s}$	$R_{\theta JA}$	Q1		40	
	Steady-State				65	
Junction-to-Case		$R_{\theta JC}$	Q2		5	
			Q1		5.5	

¹Pulse width limited by maximum junction temperature .

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$.

³The Power dissipation is based on $R_{\theta JA}$ $t \leq 10\text{ s}$ value.

³Package limitation current :Q1=10A,Q2=-10A

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	CH.	LIMITS			UNITS
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\mu\text{A}$	Q2	-30			V
		$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	Q1	30			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	Q2	-1	-1.5	-2.5	V
		$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	Q1	1	1.6	2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Q2			± 100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Q1			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	Q2			-1	μA
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	Q1			1	
		$V_{DS} = -20\text{ V}$ $V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Q2			-10	
		$V_{DS} = 20\text{ V}$ $V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Q1			10	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$	Q2		30	45	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}$	Q1		18	32	
		$V_{GS} = -10\text{ V}, I_D = -6\text{ A}$	Q2		20	28	
		$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$	Q1		14	22	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5\text{ V}, I_D = -6\text{ A}$	Q2		18		S
		$V_{DS} = 5\text{ V}, I_D = 7\text{ A}$	Q1		27		

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N & P-Channel Enhancement Mode MOSFET

DYNAMIC							
Input Capacitance	C_{iss}	Q2 $V_{GS} = 0V,$ $V_{DS} = -15V, f = 1MHz$	Q2		929		pF
Output Capacitance	C_{oss}	Q1	Q1		341		
Reverse Transfer Capacitance	C_{rss}	Q2 $V_{GS} = 0V,$ $V_{DS} = 15V, f = 1MHz$	Q2		145		
			Q1		84		
Gate Resistance	R_g	$V_{GS} = 0V,$ $V_{DS} = 0V, f = 1MHz$	Q2		12		Ω
			Q1		3		
Total Gate Charge ²	Q_g	Q2 $V_{DS} = -15V,$ $V_{GS} = -10V, I_D = -6A$	Q2		20.8		nC
			Q1		7.6		
Gate-Source Charge ²	Q_{gs}	Q1 $V_{DS} = 15V,$ $V_{GS} = 10V, I_D = 7A$	Q2		10.8		
			Q1		4.3		
Gate-Drain Charge ²	Q_{gd}		Q2		2		
			Q1		1		
Turn-On Delay Time ²	$t_{d(on)}$	Q2 $V_{DS} = -15V, I_D \cong -6A,$ $V_{GS} = -10V, R_{GEN} = 6\Omega$	Q2		15		nS
			Q1		15		
Rise Time ²	t_r	Q1 $V_{DS} = 15V, I_D \cong 7A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$	Q2		30		
			Q1		30		
Turn-Off Delay Time ²	$t_{d(off)}$		Q2		50		
			Q1		20		
Fall Time ²	t_f		Q2		41		
			Q1		13		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)							
Continuous Current ³	I_S		Q2			-25	A
			Q1			20	
Forward Voltage ¹	V_{SD}	$I_F = -6A, V_{GS} = 0V$	Q2			-1	V
			Q1			1.1	
Reverse Recovery Time	t_{rr}	Q2 $I_F = -6A, di_F/dt = 100A/\mu S$	Q2		12.6		nS
			Q1		7.9		
Reverse Recovery Charge	Q_{rr}	Q1 $I_F = 7A, di_F/dt = 100A/\mu S$	Q2		4.2		nC
			Q1		1.2		

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

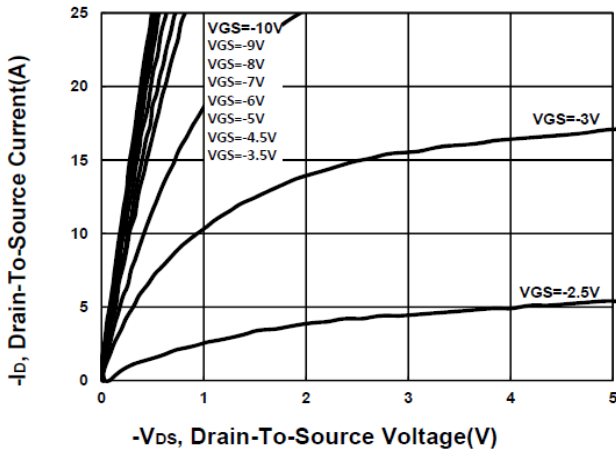
³Package limitation current :Q1=10A,Q2=-10A

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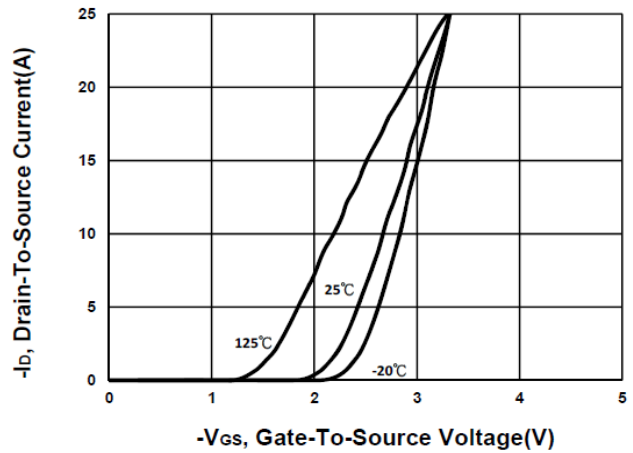
N & P-Channel Enhancement Mode MOSFET

Q2

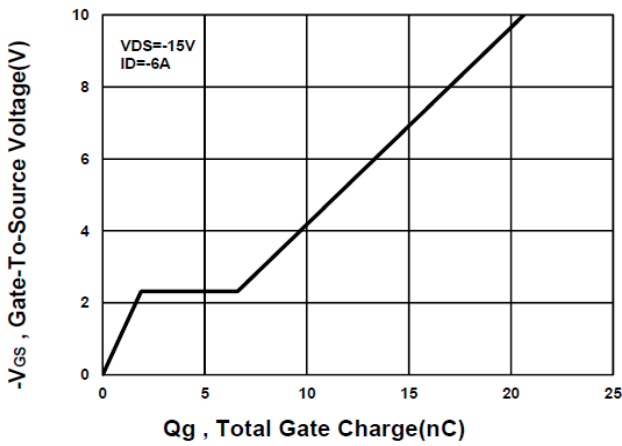
Output Characteristics



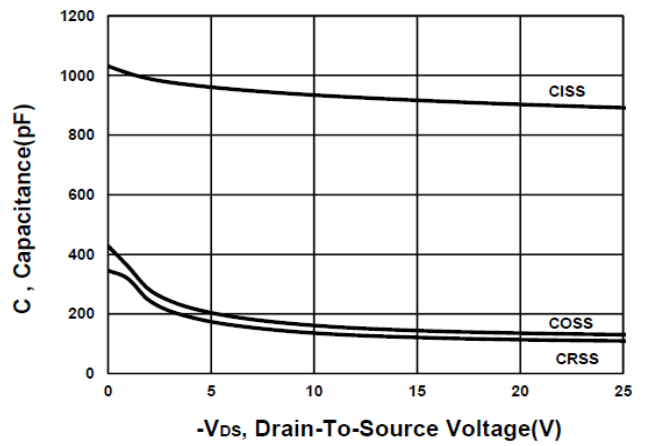
Transfer Characteristics



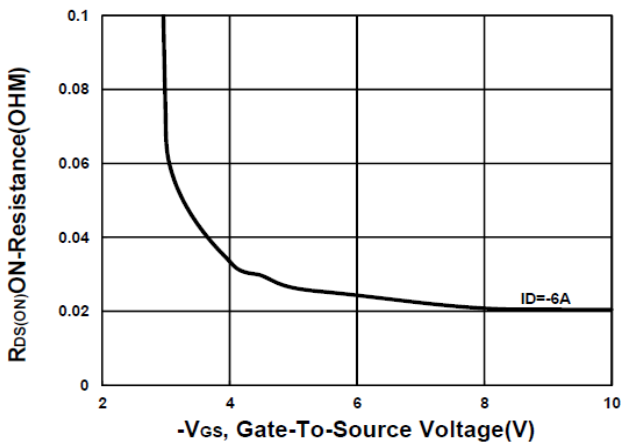
Gate charge Characteristics



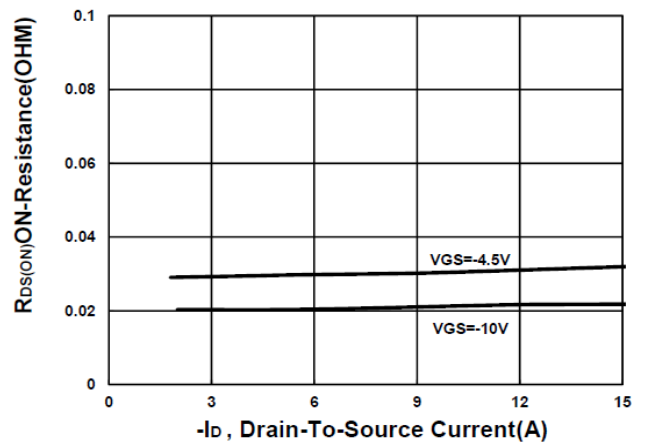
Capacitance Characteristic



On-Resistance VS Gate-To-Source



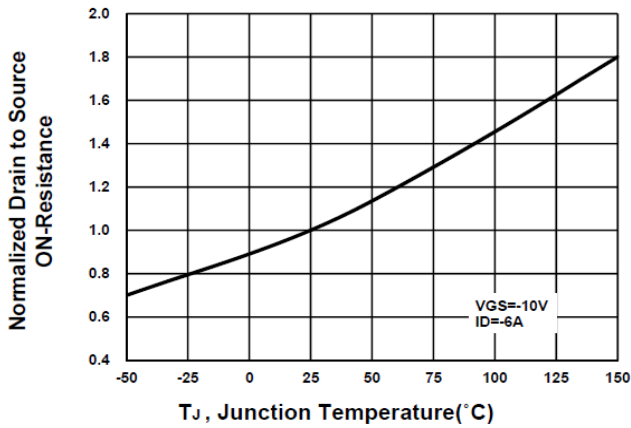
On-Resistance VS Drain Current



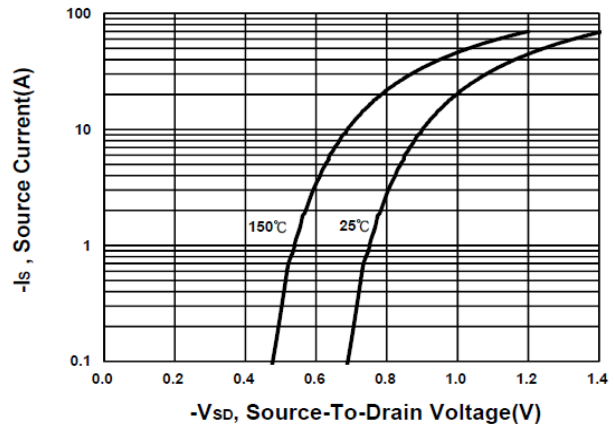
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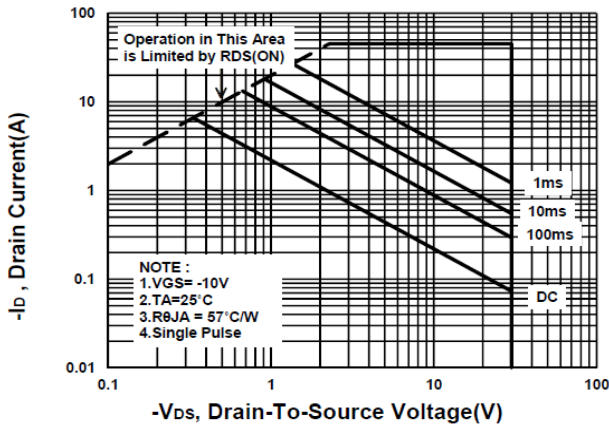
On-Resistance VS Temperature



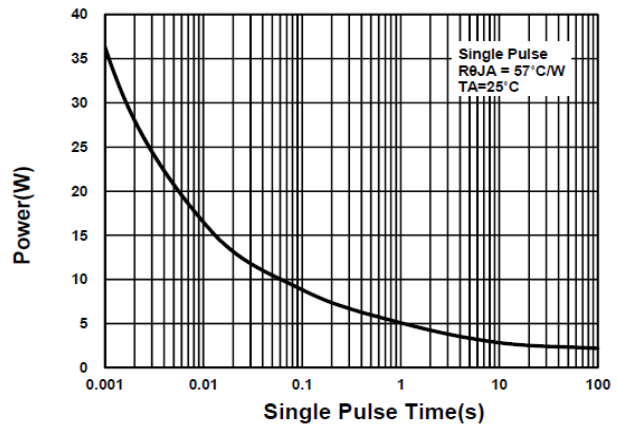
Source-Drain Diode Forward Voltage



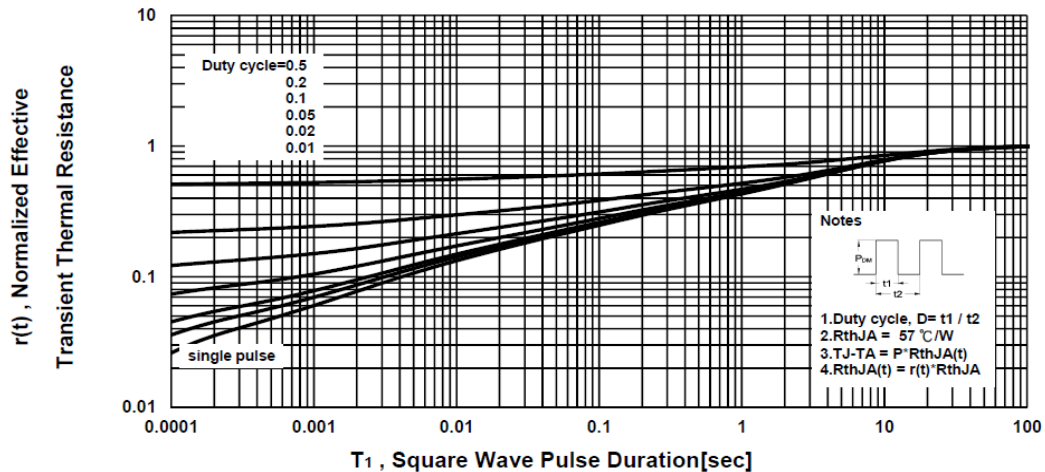
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

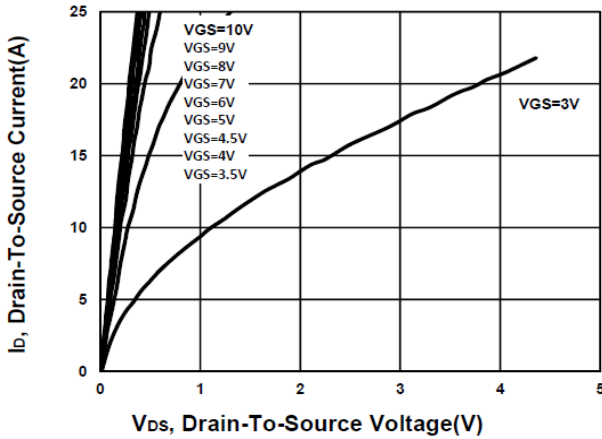


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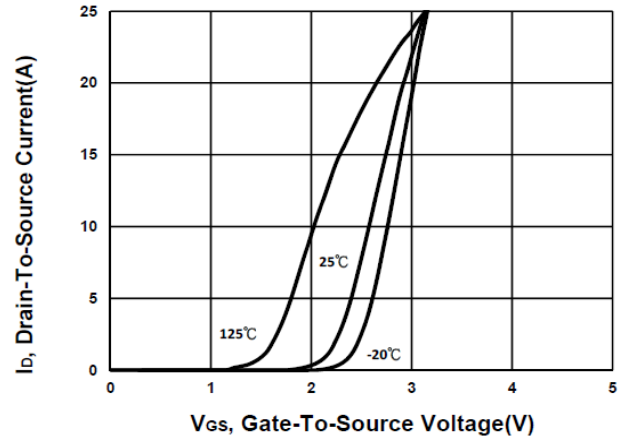
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Q1

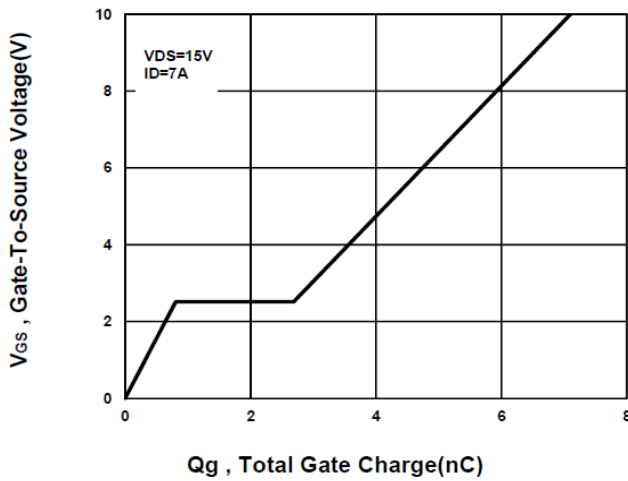
Output Characteristics



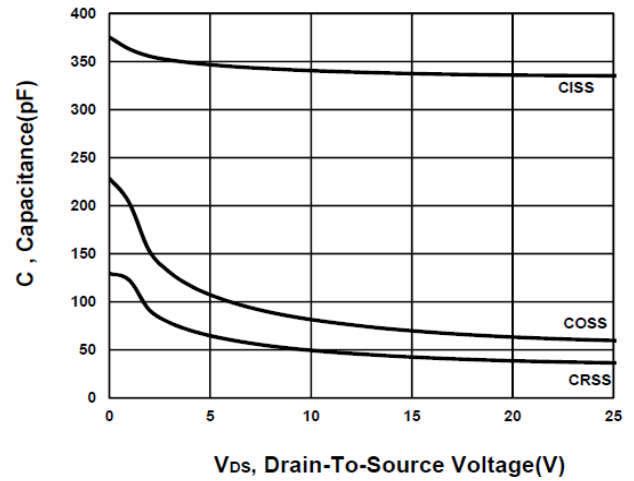
Transfer Characteristics



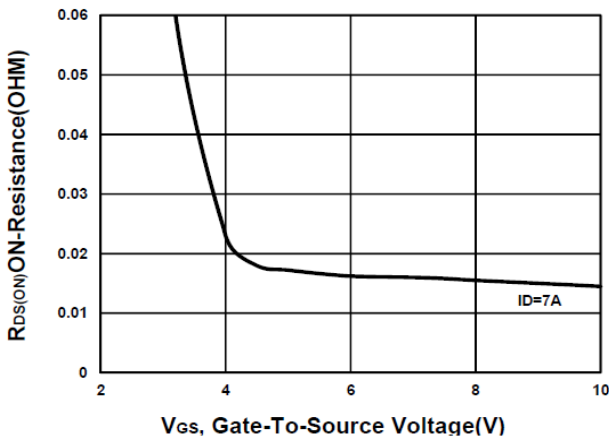
Gate charge Characteristics



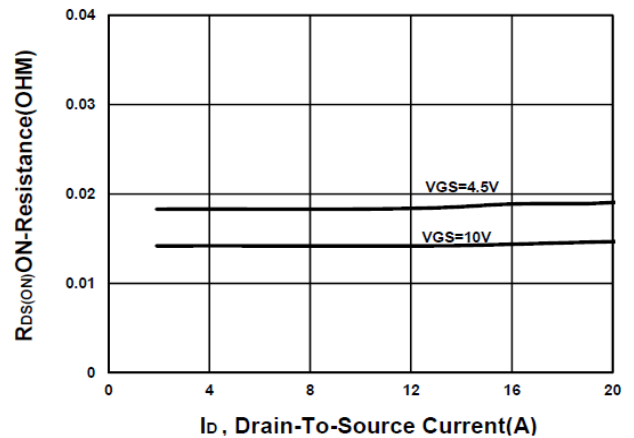
Capacitance Characteristic



On-Resistance VS Gate-To-Source

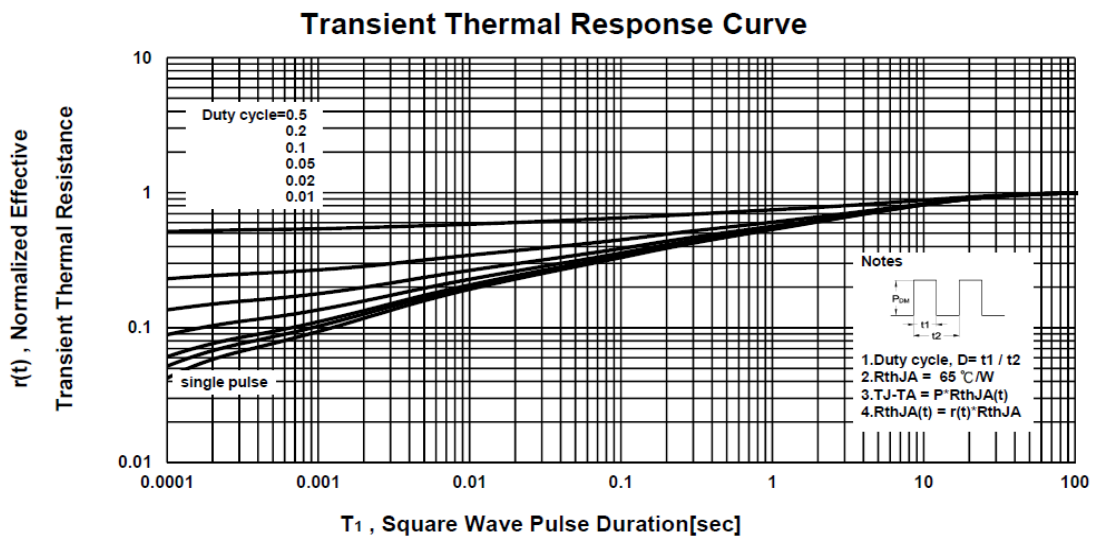
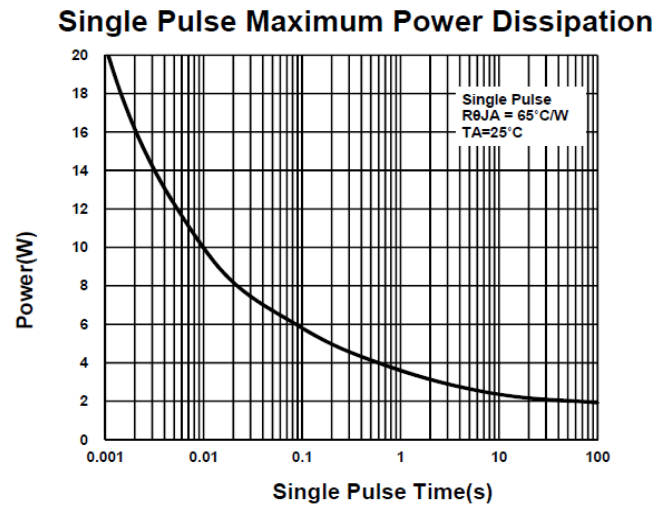
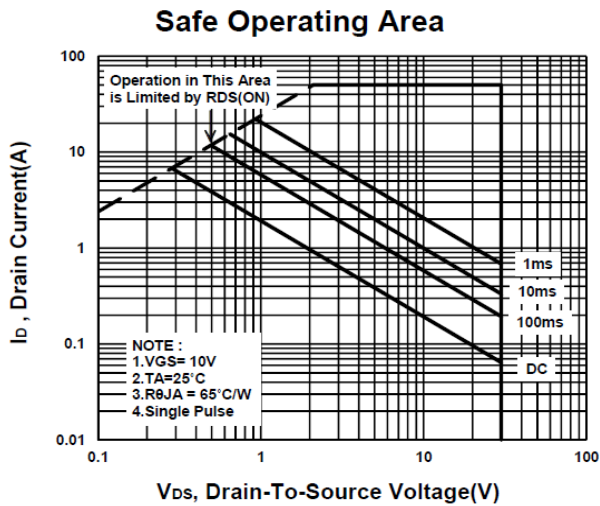
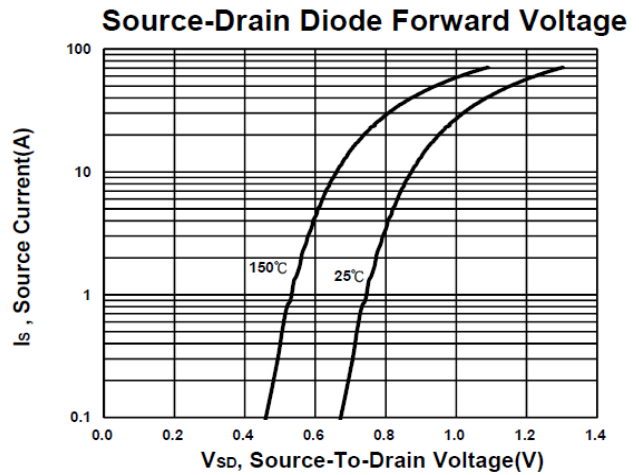
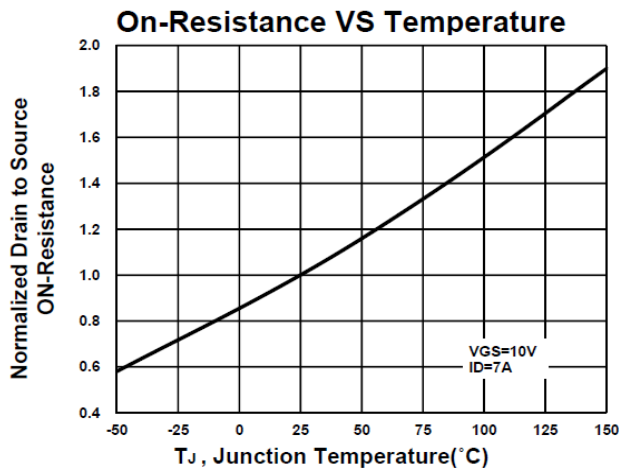


On-Resistance VS Drain Current



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N & P-Channel Enhancement Mode MOSFET



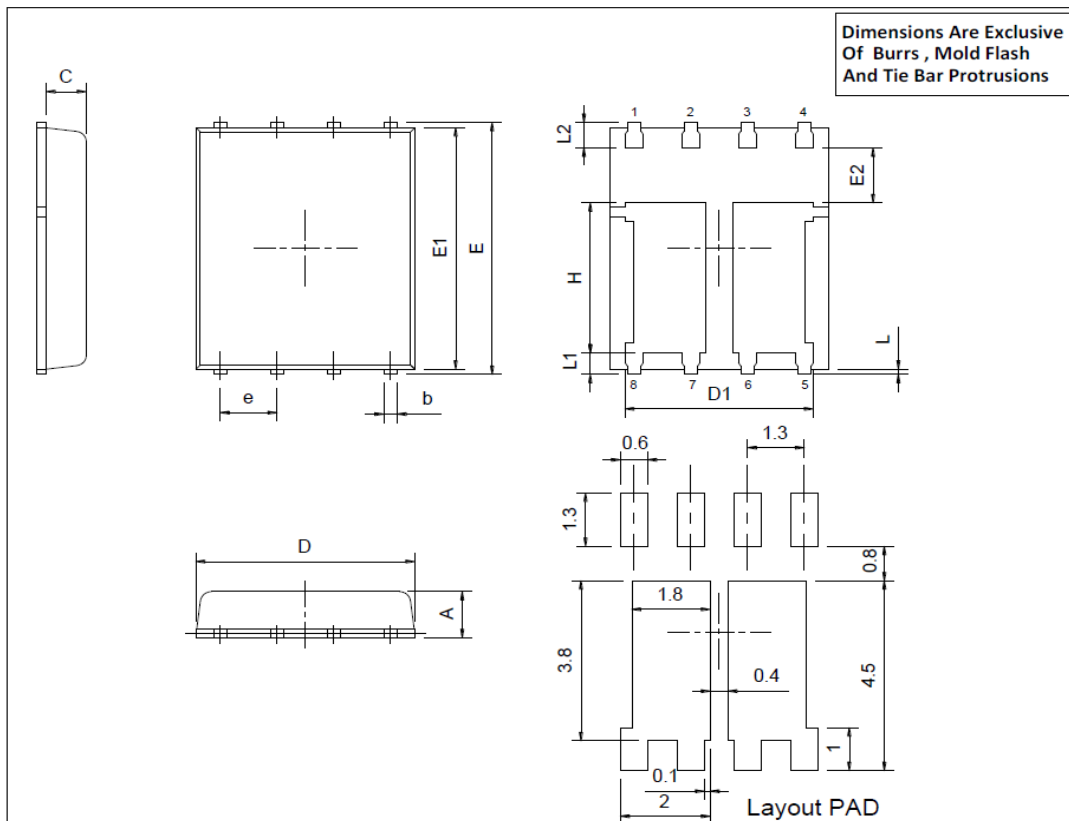
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N & P-Channel Enhancement Mode MOSFET

Package Dimension

PDFN 5x6P(左右 Dual) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.9		1.17	e		1.27	
b	0.33		0.51	L	0.05		0.25
C	0.7		0.97	L1	0.38		0.61
D	4.8		5.0	L2	0.38		0.71
D1	3.61		4.31	H	3.38		3.78
E	5.9		6.15				
E1	5.65		5.85				
E2	1.1						

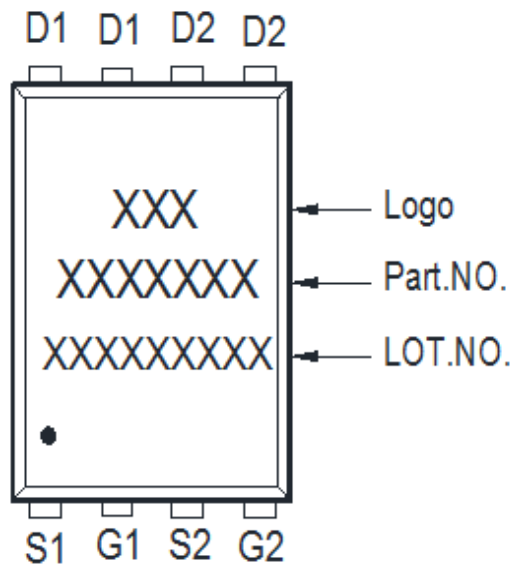


* 散热片形状会因为封装厂框架不同而有所差异。

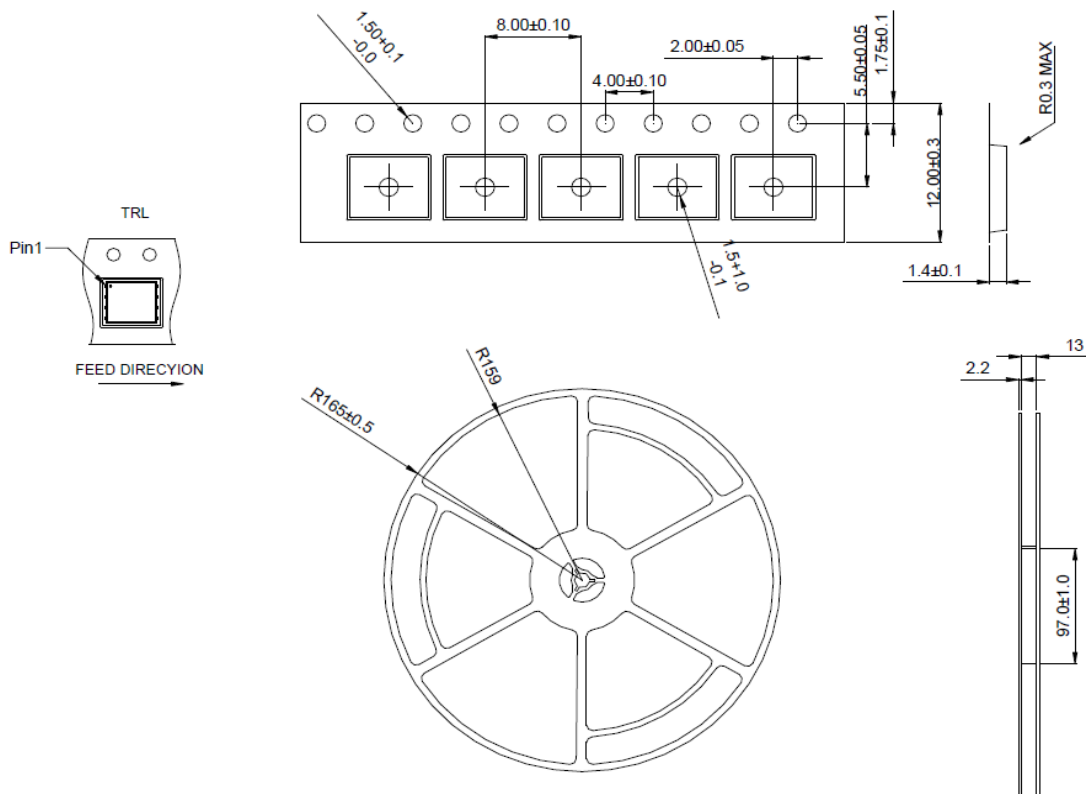
PK601CA

N & P-Channel Enhancement Mode MOSFET

A. Marking Information



B. Tape & Reel Information: 3000pcs/Reel

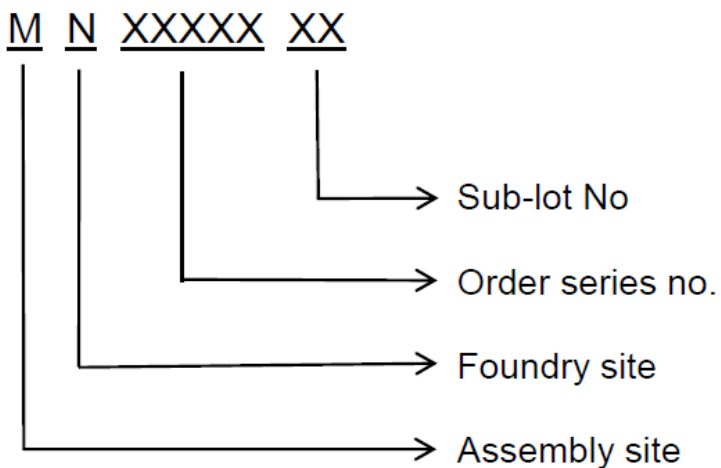


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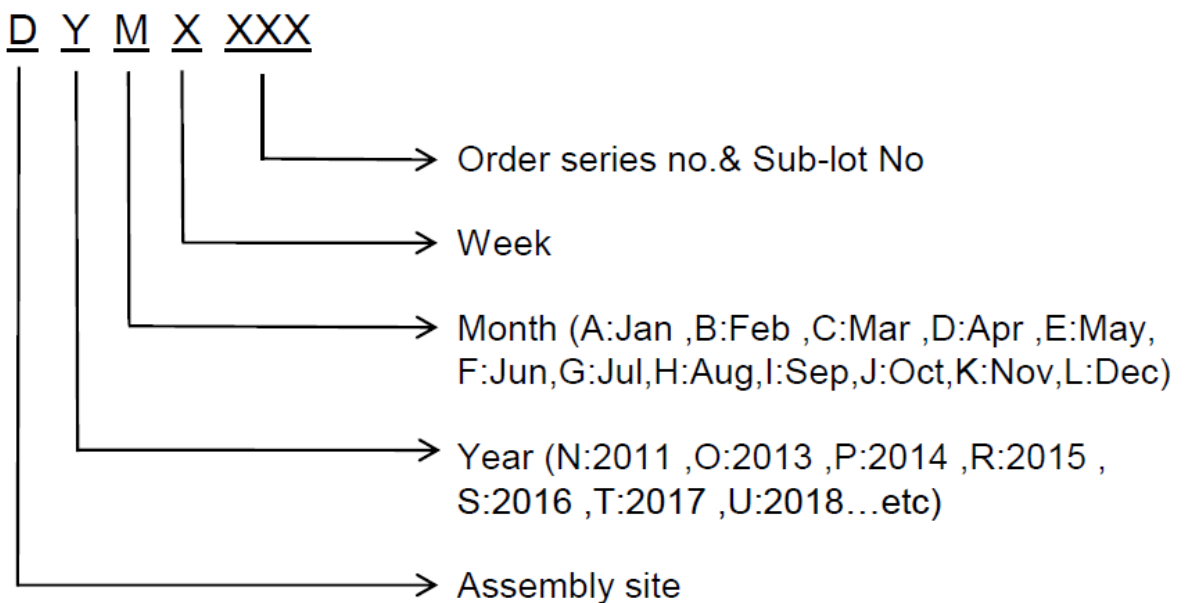
N & P-Channel Enhancement Mode MOSFET

C. Lot No.&Date Code rule

1.Lot No.



2.Date Code





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D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文”0”和数字”0”，”G和”Q”的字型即可)
3	U-NIKC	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	RoHS label	 long axis: 12 mm minor axis:6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert “ / “ between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least