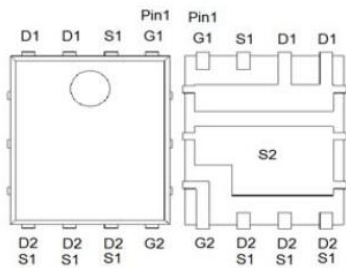


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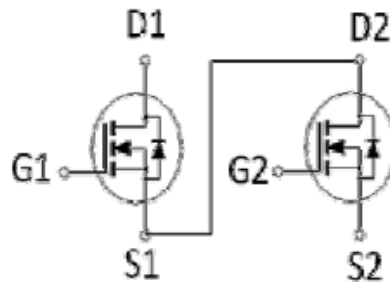
Dual N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D	CH.
30V	1.9m Ω @ $V_{GS} = 10V$	95A	Q2
30V	5.5m Ω @ $V_{GS} = 10V$	48A	Q1



PDFN 5*6P



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	CH.	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	Q2	30	V
			Q1	30	
Gate-Source Voltage		V_{GS}	Q2	± 20	V
			Q1	± 20	
Continuous Drain Current ³	$T_C = 25\text{ }^\circ\text{C}$	I_D	Q2	95	A
			Q1	48	
	$T_C = 100\text{ }^\circ\text{C}$		Q2	60	
			Q1	30	
Pulsed Drain Current ¹		I_{DM}	Q2	150	A
			Q1	120	
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	I_D	Q2	24	A
			Q1	13	
	$T_A = 70\text{ }^\circ\text{C}$		Q2	19	
			Q1	10	
Avalanche Current		I_{AS}	Q2	53	A
			Q1	26	
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	Q2	140	mJ
			Q1	33.8	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	Q2	36	W
			Q1	25	
	$T_C = 100\text{ }^\circ\text{C}$		Q2	14	
			Q1	10	

PK612DZ

Dual N-Channel Enhancement Mode MOSFET

Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	Q2	2.4	W
	$T_A = 70\text{ }^\circ\text{C}$		Q1	1.8	
			Q2	1.5	
	Q1		1.1		
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	CH.	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$	Q2		52	$^\circ\text{C} / \text{W}$
		Q1		69	
Junction-to-Case	$R_{\theta JC}$	Q2		3.4	
		Q1		5	

¹Pulse width limited by maximum junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

³Package limitation current :Q1=35A,Q2=35A.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	CH.	LIMITS			UNITS	
				MIN	TYP	MAX		
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	Q2	30			V	
			Q1	30				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	Q2	1.3	1.7	2.3	V	
			Q1	1.3	1.7	2.3		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q2			± 100	nA	
			Q1			± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$	Q2			1	μA	
			Q1			1		
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 55\text{ }^\circ\text{C}$	Q2			10		
			Q1			10		
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 16A$	Q2		1.8	2.5	m Ω	
			$V_{GS} = 4.5V, I_D = 11A$	Q1		5.2		7.4
			$V_{GS} = 10V, I_D = 20A$	Q2		1.4		1.9
			$V_{GS} = 10V, I_D = 11A$	Q1		3.9		5.5
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 20A$	Q2		70		S	
		$V_{DS} = 5V, I_D = 11A$	Q1		50			

PK612DZ

Dual N-Channel Enhancement Mode MOSFET

DYNAMIC									
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 15V, f = 1MHz$	Q2		2779		pF		
Output Capacitance	C_{oss}		Q1		1041				
			Q2		522				
Reverse Transfer Capacitance	C_{rss}		Q1		198				
			Q2		318				
Gate Resistance	R_g		Q1		123				
		Q2		0.83					
Total Gate Charge ²	Q_g	$V_{GS}=10V$ $V_{GS}=4.5V$ Q2 $V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 20A$ Q1 $V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 11A$	Q2		54		nC		
			Q1		21				
			Q2		29				
			Q1		11				
Gate-Source Charge ²	Q_{gs}	Q2		7.1					
Gate-Drain Charge ²	Q_{gd}	Q1		2.4					
		Q2		13.4					
Turn-On Delay Time ²	$t_{d(on)}$	Q2 $V_{DS} = 15V, I_D \cong 20A,$ $V_{GS}=10V, R_{GEN}= 6\Omega$ Q1 $V_{DS} = 15V, I_D \cong 11A,$ $V_{GS} = 10V, R_{GEN} =6\Omega$	Q2		25			nS	
			Q1		23				
Rise Time ²	t_r		Q2		17				
			Q1		16				
Turn-Off Delay Time ²	$t_{d(off)}$		Q2		54				
			Q1		50				
Fall Time ²	t_f		Q2		17				
			Q1		15				
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)									
Continuous Current ³	I_S			Q2		36			A
				Q1		20			
Forward Voltage ¹	V_{SD}		$I_F = 20A, V_{GS} = 0V$ $I_F = 11A, V_{GS} = 0V$	Q2		1			V
		Q1			1.2				
Reverse Recovery Time	t_{rr}	Q2 $I_F = 20A, di_F/dt = 100A /\mu S$ Q1 $I_F = 11A, di_F/dt = 100A /\mu S$	Q2		21		nS		
			Q1		12.4				
Reverse Recovery Charge	Q_{rr}		Q2		10		nC		
			Q1		4				

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

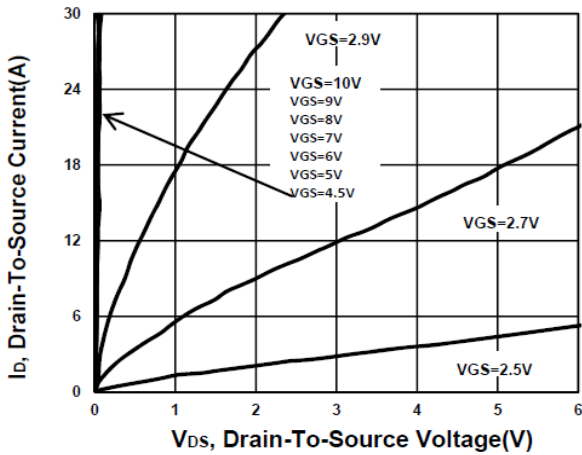
³Package limitation current :Q1=35A,Q2=35A.

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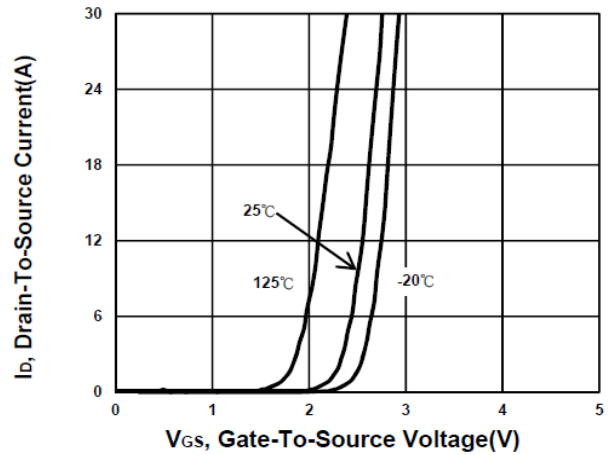
Dual N-Channel Enhancement Mode MOSFET

Q2

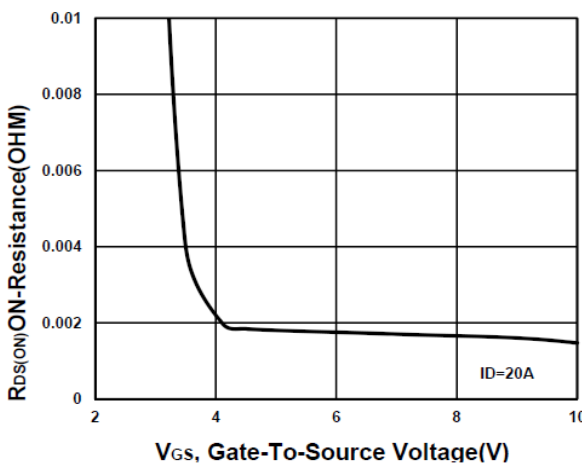
Output Characteristics



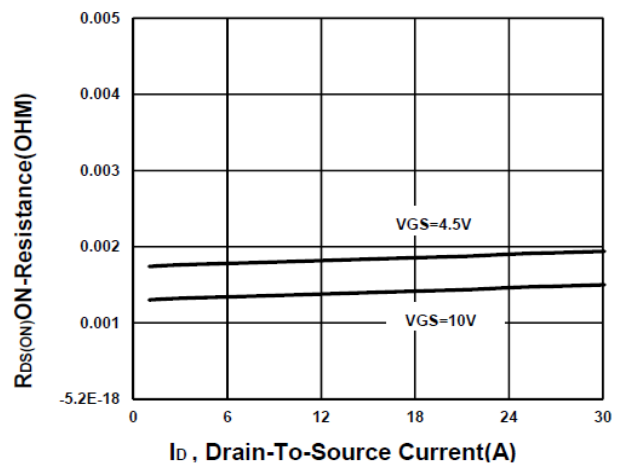
Transfer Characteristics



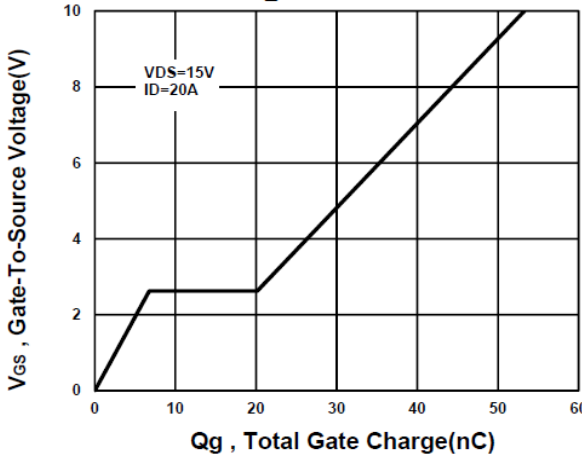
On-Resistance VS Gate-To-Source



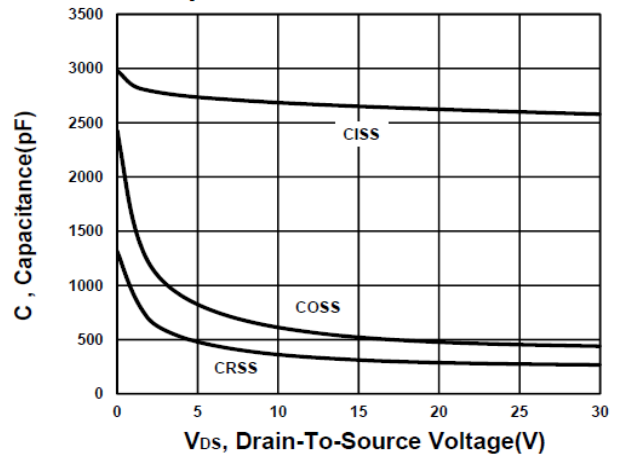
On-Resistance VS Drain Current



Gate charge Characteristics



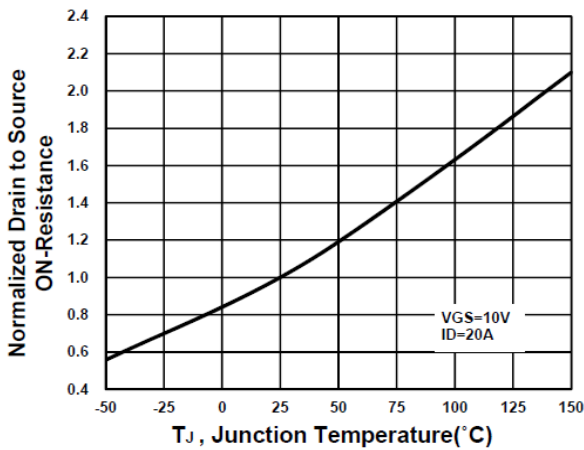
Capacitance Characteristic



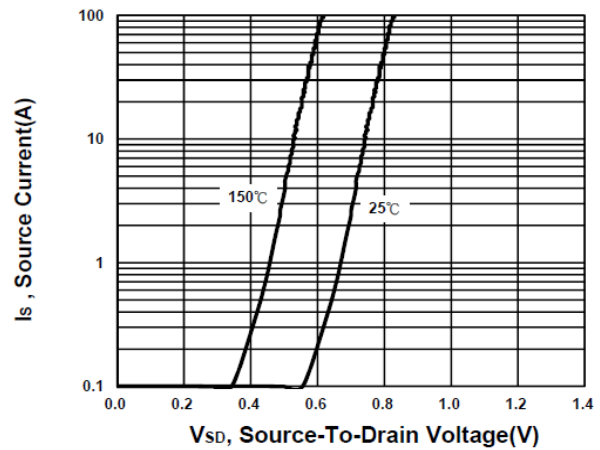
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Dual N-Channel Enhancement Mode MOSFET

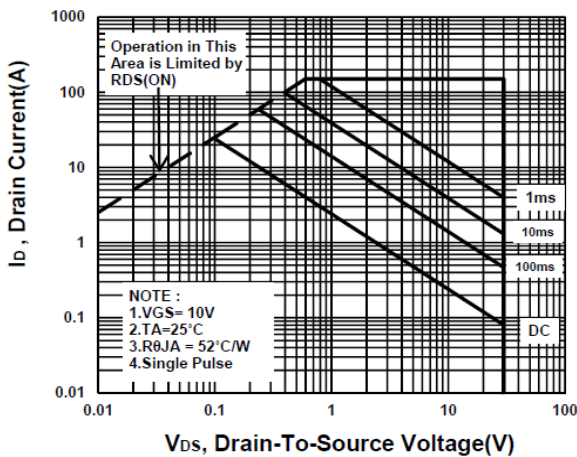
On-Resistance VS Temperature



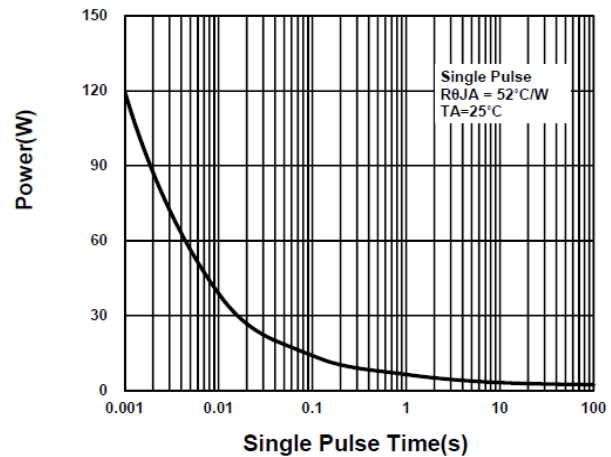
Source-Drain Diode Forward Voltage



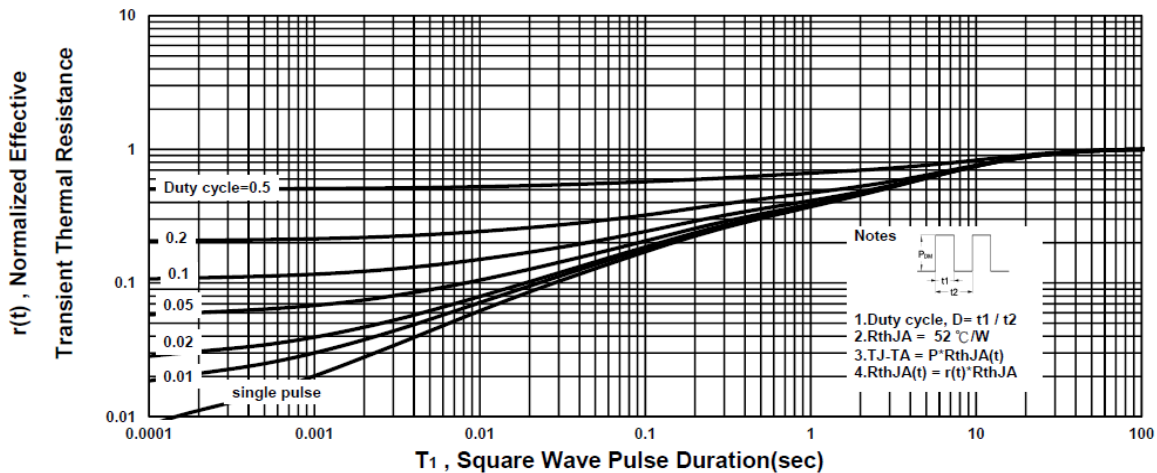
Safe Operating Area



Single Pulse Maximum Power Dissipation

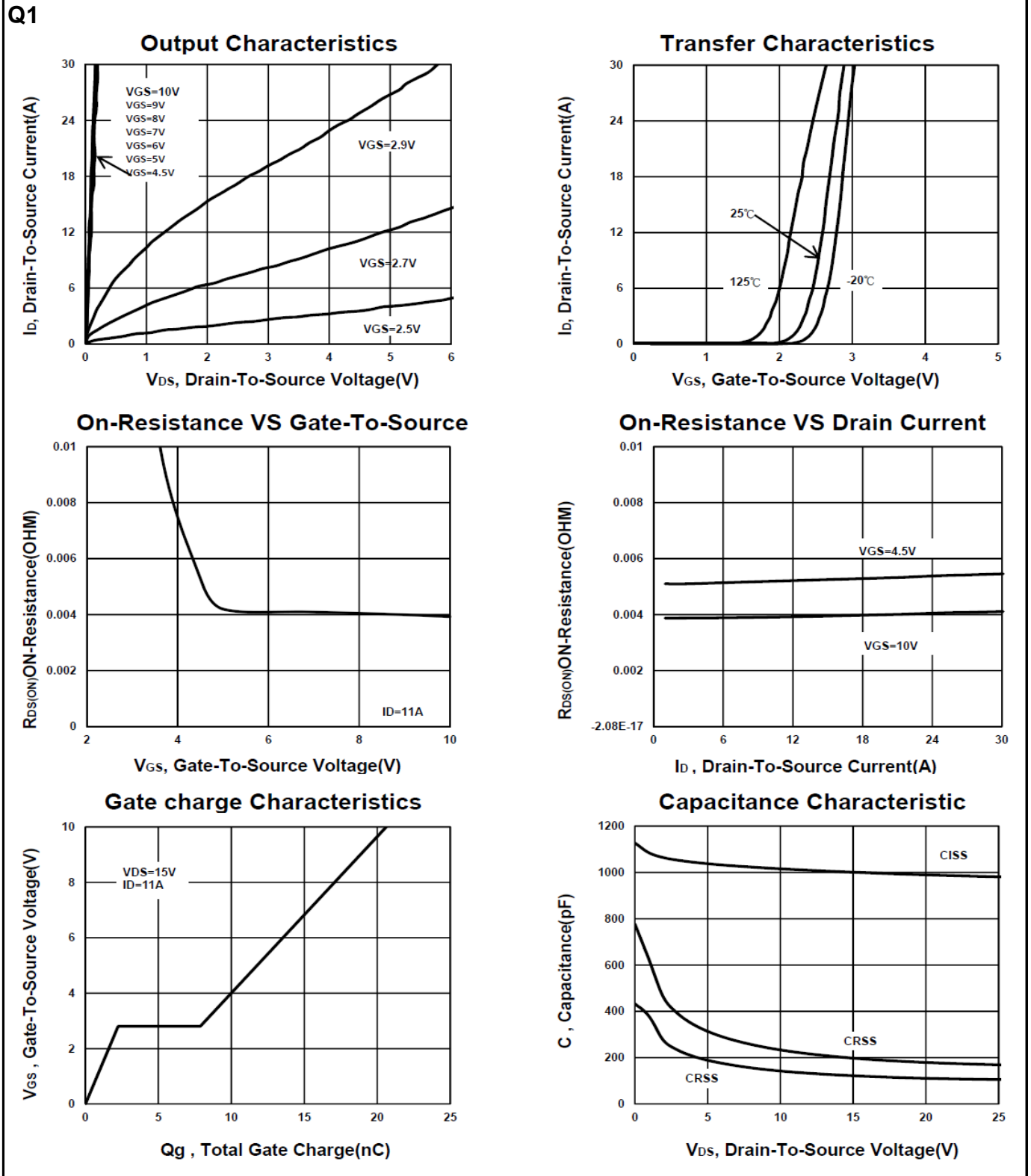


Transient Thermal Response Curve



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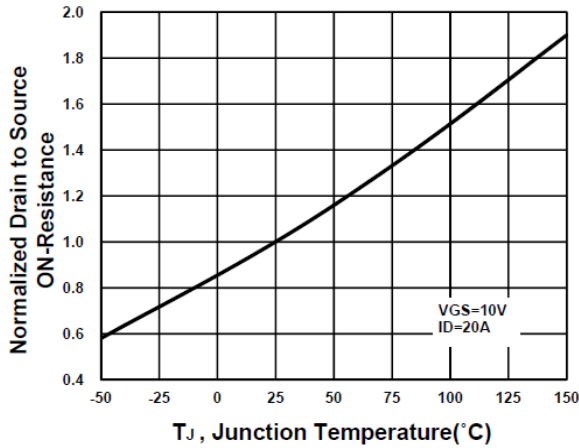
Dual N-Channel Enhancement Mode MOSFET



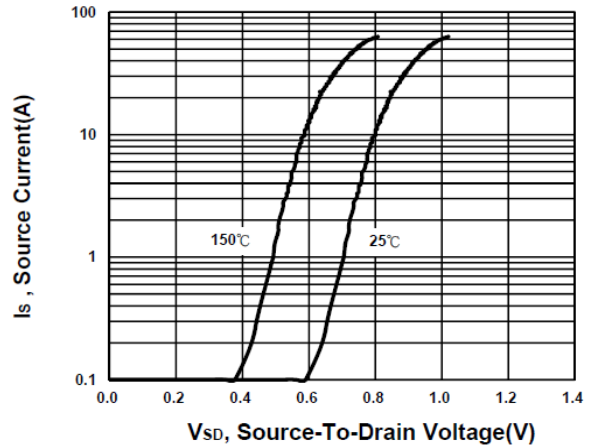
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Dual N-Channel Enhancement Mode MOSFET

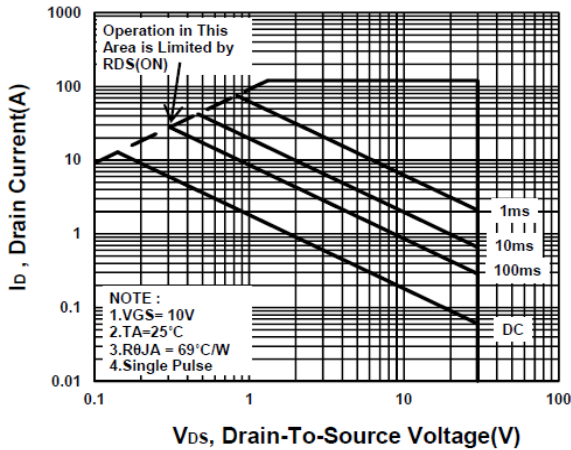
On-Resistance VS Temperature



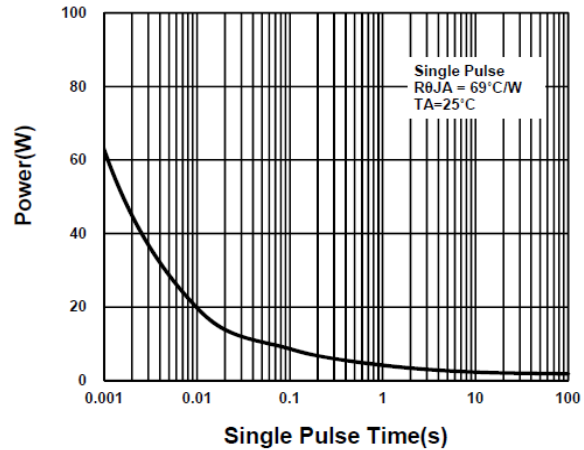
Source-Drain Diode Forward Voltage



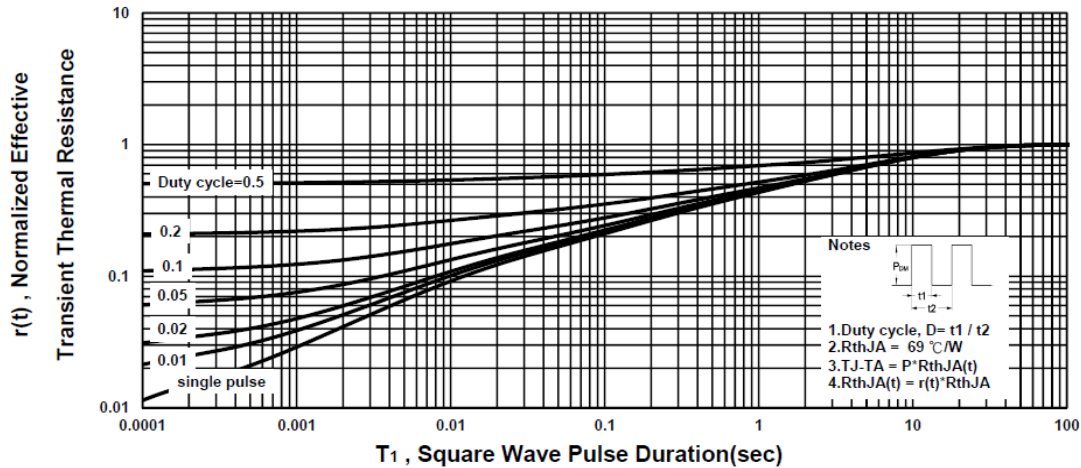
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



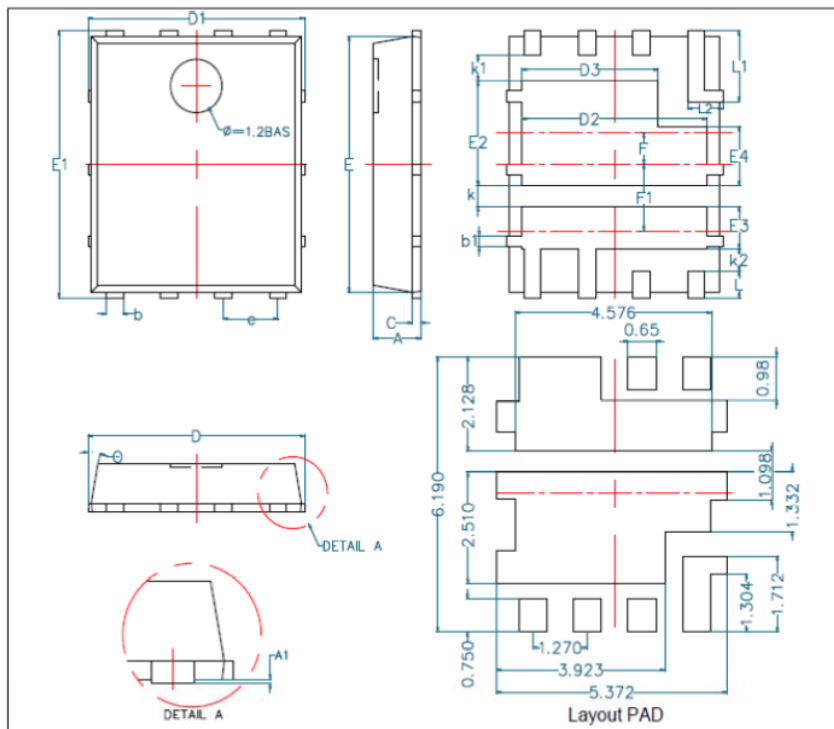
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Dual N-Channel Enhancement Mode MOSFET

Package Dimension

PDFN 5x6P(Dual flip chip) MECHANICAL DATA

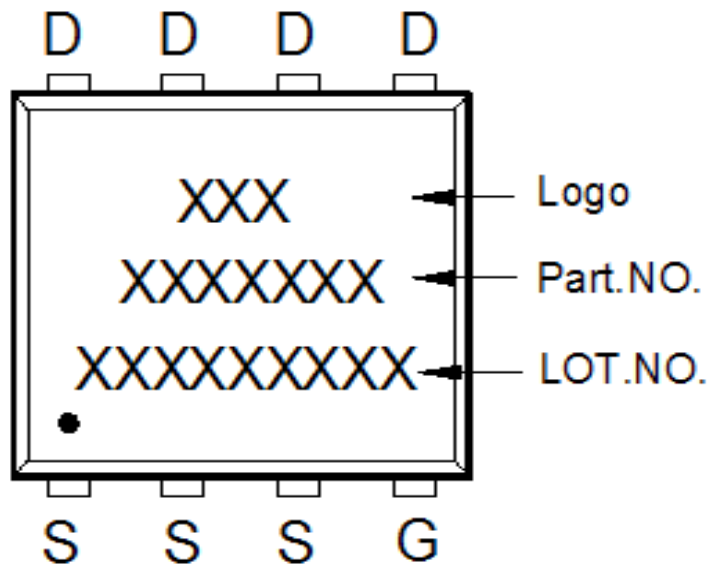
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.00		1.20	E3	0.85		1.15
A1	0.00		0.05	E4	1.23		1.53
b	0.30		0.50	e	1.27 BSC		
b1	0.15		0.35	Θ	10° REF		
c	0.15		0.25	L	0.40		0.60
D1	5.05 BSC			L1	1.50		1.70
D	4.80		5.00	L2	0.72		0.92
D2	4.15		4.45	K	0.47 BSC		
D3	3.02		3.32	K1	0.58 BSC		
E1	6.00 BSC			K2	0.50 BSC		
E	5.65		5.85	F	0.695 REF		
E2	2.30		2.60	F1	1.50REF		



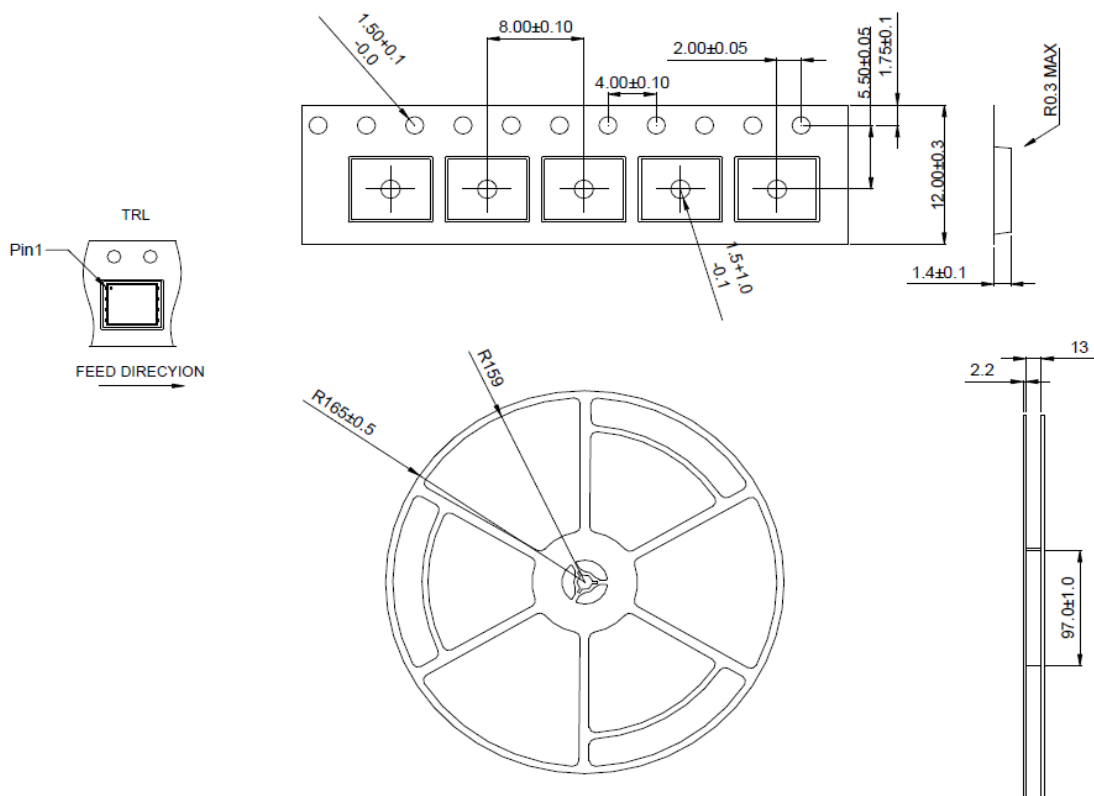
PK612DZ

Dual N-Channel Enhancement Mode MOSFET

A. Marking Information



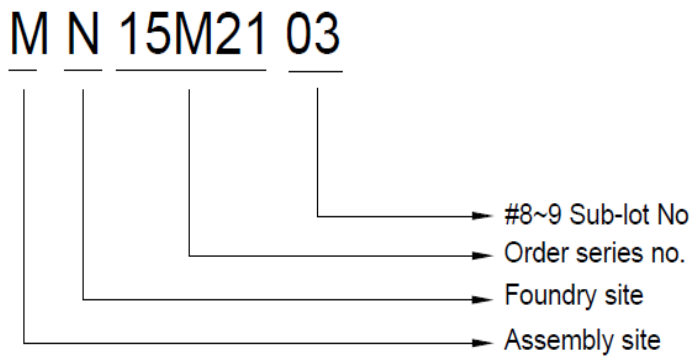
B. Tape & Reel Information: 3000pcs/Reel



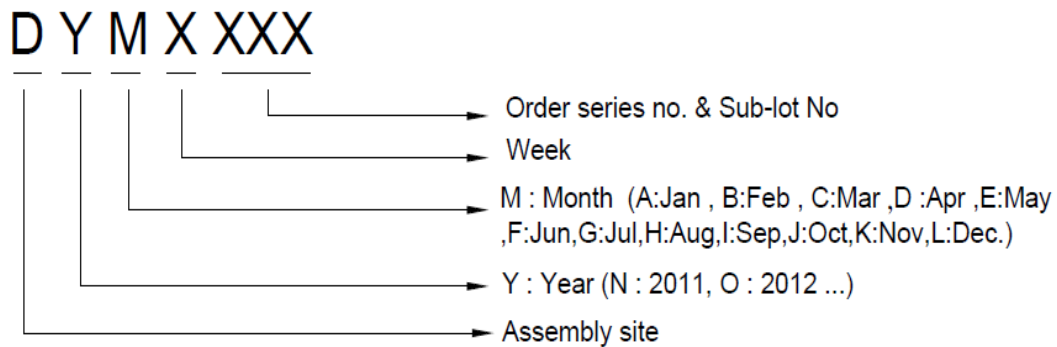
PK612DZ
Dual N-Channel Enhancement Mode MOSFET

C. Lot.No. & Date Code rule

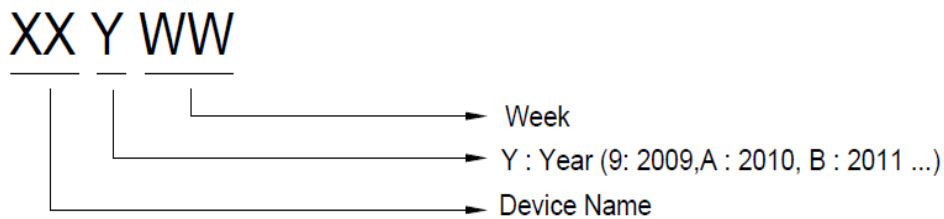
1.LOT.NO.



2.Date Code



3.Date Code (for Small package)





PK612DZ

Dual N-Channel Enhancement Mode MOSFET

D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文”0”和数字”0”，”G和”Q”的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “ / “ between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least