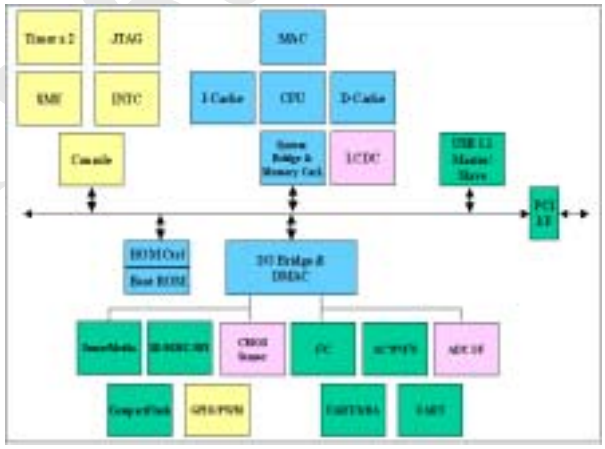
PL-1061
Mobile Computing System

OVERVIEW

The PL-1061 is a low-cost high-performance single chip mobile computing system solution. With a powerful 32-bit RISC CPU core and a wide range of hardware controlled peripheral interfaces, it is capable of handling most mobile computing applications' requirements.

The PL-1061 is designed to cover both low power consumption and high performance applications at the same time. The software could change the system clock rate and CPU clock rate on the run. It gives the applications extra edges on delivering the most computation power when needed and preserve power when the circumstances allowed.

Block Diagram



FEATURE

- MIPS R3000 compatible 32-bit RISC core with MAC Co-Processor running at maximum speed of 100 MHz
- 4K-Byte Direct-Mapped Data Cache, and 4K-Byte 2-way set-associative Instruction Cache
- 16-/32-bit Memory Interface, one chip select supports up to 256MB SDRAM
- 8K-Byte embedded Boot ROM
- Programmable CMOS Sensor Interface
- LCD Controller (STN, TFT, up to 800x600 size and 64k color)
- Support external touch screen controllers, e.g. TI ADS7843, ADI AD7843, etc.
- Support PCI I/F compliant with PCI 2.1 spec.
- SmartMedia Interface
- Support SD/MMC/SPI and SDIO I/F
- CompactFlash Interface
- Support AC `97 / I^2S Interface
- I^2C Master/Slave Interface
- Support USB 1.1 master/slave
- Support one UART/PS2, and one IrDA up to 115.2Kbps
- GPIO and Pulse-Width-Modulation
- Independent Power Domain for RTC and Power Management functions
- JTAG Emulation Interface
- Remote Debugger (GDB) interface
- Support Embedded Linux
- Package type: 388-pin BGA; Footprint: 27mm x 27mm

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