Selectable High Speed Translator Buffer to CMOS, PECL, LVDS

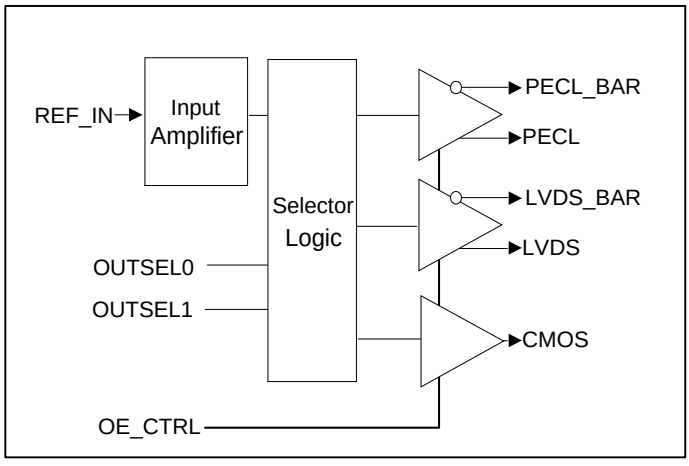
FEATURES

- User selectable output: Differential PECL, Differential LVDS or CMOS/TTL
- Single internally AC coupled input
- Accepts input signal swings as low as 100mV
- Input range from DC to 1.3 GHz.
- 3.3V operation.
- Available in DIE (65 mil x 62 mil).

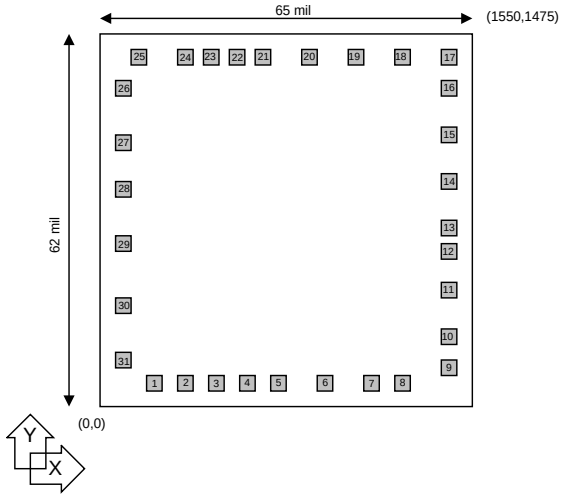
DESCRIPTIONS

The PL130-00 is a low cost, high performance, high speed, buffer that reproduces any input frequency from DC to 1.3GHz. It provides selectable user outputs, between differential PECL, differential LVDS or CMOS/TTL. Any input signal with at least 100mV swing can be used as reference signal. This chip is ideal for conversion from sine wave, TTL, CMOS, or LVDS to PECL, LVDS or CMOS.

BLOCK DIAGRAM



DIE CONFIGURATION



DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

OUTPUT SELECTION AND ENABLE

Pad #18 OUTSEL1	Pad #25 OUTSEL0	Selected Output
0	0	High Drive CMOS
0	1	Standard CMOS
1	0	PECL
1	1	LVDS

OE_SELECT (Pad #9)	OE_CTRL (Pad #30)	State
0	0 (Default)	Output enabled
	1	Tri-state
1 (Default)	0	Tri-state
	1 (Default)	Output enabled

Pad #9: Bond to GND to set to "0", bond to VDD to set to "1"
Pad #30: Logical states defined by PECL levels if OE_SELECT (pad #9) is "0"
Logical states defined by CMOS levels if OE_SELECT is "1"

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.
* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

2. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	PECL/LVDS/CMOS			80/60/20	mA
Operating Voltage	V_{DD}		3.13		3.47	V
Short Circuit Current				±50		mA

3. AC Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		0		1300	MHz
Input signal swing	REF_IN input	100			mV
Output Frequency		0		1300	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns

4. CMOS Output Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Voltage	V_{OH}	I_{OH} = -12mA	2.4			V
Output Low Voltage	V_{OL}	I_{LO} = 12mA			0.4	V
Output High Voltage	V_{OHC}	I_{OH} = -4mA, at CMOS level	V_{DD}– 0.4			V
Output Drive Current		At TTL level	12	17		mA

5. CMOS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Clock Rise/Fall Time		0.8V ~ 2.0V with 10 pF load		1.15		ns
		0.3V ~ 3.0V with 15 pF load		3.7		
Output Clock Duty Cycle		@ 1.4V	45	50	55	%

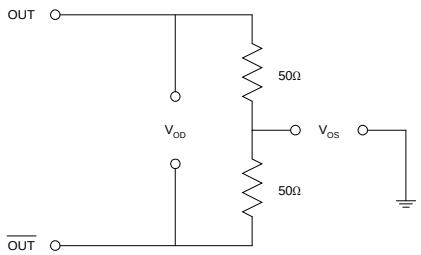
6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

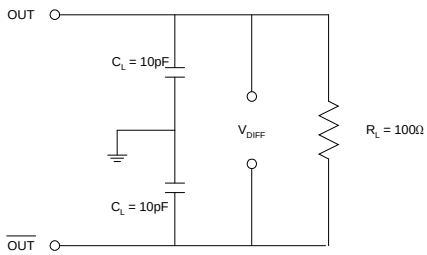
7. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns
Output Clock Duty Cycle		@ 1.25V	45	50	55	%

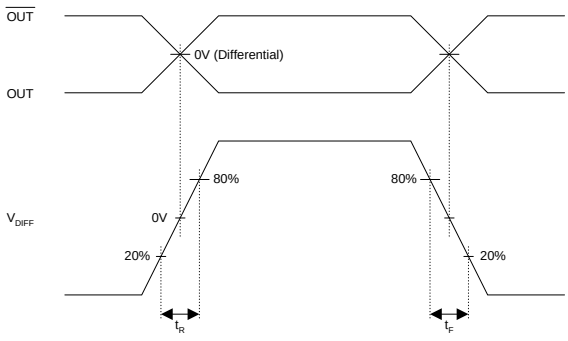
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



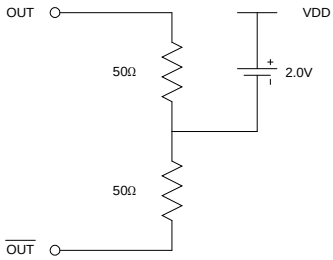
8. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

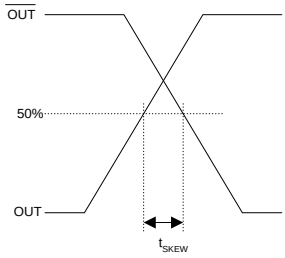
9. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns
Output Clock Duty Cycle		@ Vdd – 1.3V	45	50	55	%

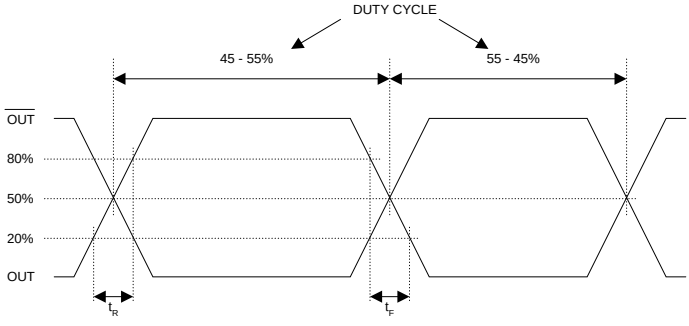
PECL Levels Test Circuit



PECL Output Skew



PECL Transistion Time Waveform



PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)
1	GND	248	109
2	GND	361	109
3	GND	473	109
4	GND	587	109
5	GND	702	109
6	REF_IN	874	109
7	GND	1042	109
8	GNDBUF	1171	109
9	OE_SELECT	1400	125
10	LVDS	1400	259
11	PECL	1400	476
12	VDDBUF	1400	616
13	VDDBUF	1400	716
14	PECLB	1400	871
15	LVDSB	1400	1089
16	CMOS	1400	1227
17	GNDBUF	1389	1365
18	OUTSEL1	1232	1365
19	GND	1042	1365
20	VDD (Optional)	854	1365
21	VDD	659	1365
22	VDD	559	1365
23	VDD	459	1365
24	VDD	358	1365
25	OUTSEL0	194	1365
26	GND (Optional)	109	1223
27	N/C	109	1017
28	GND	109	858
29	VDD (Optional)	109	646
30	OE_CTRL	109	397
31	N/C	109	181

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ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2880 Zanker Road, San Jose, CA 95134
Tel (408) 571-1668 Fax (408) 571-1688

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range