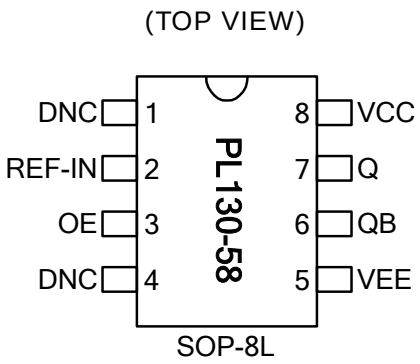
PL130-58

High Speed Translator Buffer to PECL

FEATURES

- Input clock frequency ≤266 MHz
- JEDEC standard Differential LVPECL output
- 70mA typical power supply current
- 300ps Max. Rise/Fall time
- 740ps input propagation delay
- LVCMOS and LVTTL Input compatible
- Single 2.5V ±5% or 3.3V ±10% power supply with V_{EE}=0V
- Available in 8 pin SOP Green/RoHS compliant Package

PIN CONFIGURATION

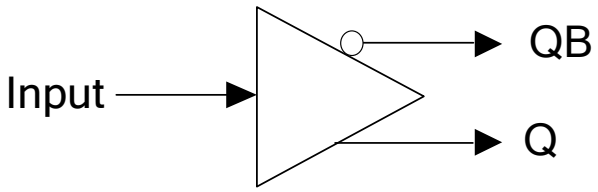


DESCRIPTION

The PL130-58 is a low cost, high performance, high speed, translator buffer that produces a pair of differential LVPECL outputs from CMOS input. Outputs are JEDEC standard LVPECL signals.

The device is targeted for Backplane buffering, data distribution, Fibre Channel and many other applications.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	SOP-8L	Type	Description
DNC	1, 4	-	Do Not Connect
REF-IN	2	Input	Reference input signal. The frequency of this signal will be re-produced at the output (after translation to PECL level).
OE	3	Input	Output enable ('1' for enable). Internal pull-up (default is '1').
VEE	5	Power	Power Ground.
QB	6	Output	PECL Complementary output.
Q	7	Output	PECL True output.
VCC	8	Power	Positive Power Supply.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		110	°C
Lead Temperature (soldering, 10s)			260	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the dev ice at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

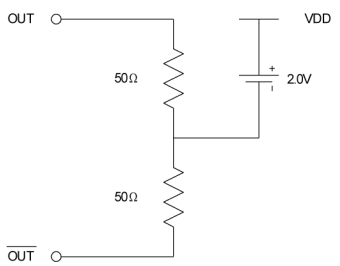
2. AC Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency				266	MHz
Output Frequency				266	MHz

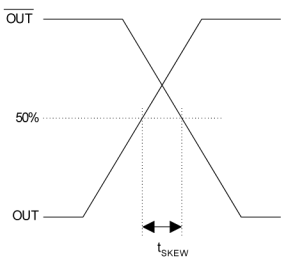
6. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% of output waveform			300	ps
Clock Fall Time	t_f	@80/20% of output waveform			300	ps

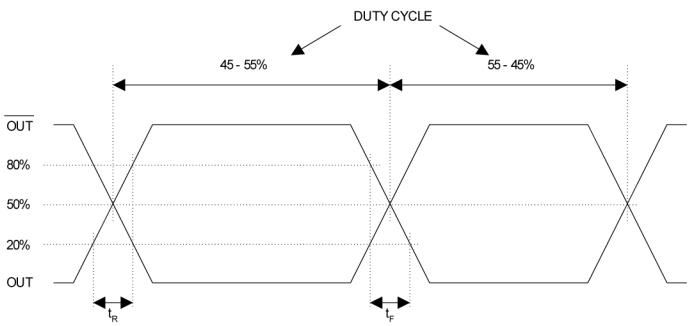
PECL Levels Test Circuit



PECL Output Skew



PECL Transistion Time Waveform

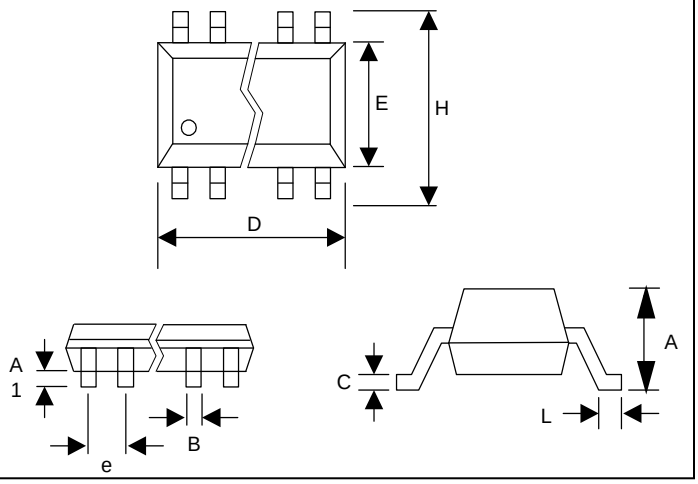


High Speed Translator Buffer to PECL

PACKAGE INFORMATION (GREEN PACKAGE COMPLIANT)

8 PIN (dimensions in mm)

	SOP–8L	
Symbol	Min.	Max.
A	1.47	1.73
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	4.95
E	3.80	4.00
H	5.80	6.20
L	0.38	1.27
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL130-58 X X - R

Part Number

R=Tape and Reel
None: Tube

Package Type
S=SOP

Temperature Range
C= Commercial (0°C to +70°C)
I= Industrial (-40°C to +85°C)

Order Number	Marking	Package Option
PL130-58SC-R	P130-58 SC LLLLL	SOP-8L - Tape and Reel
PL130-58SC		SOP-8L - Tube

***Note: LLLLL designates lot number**