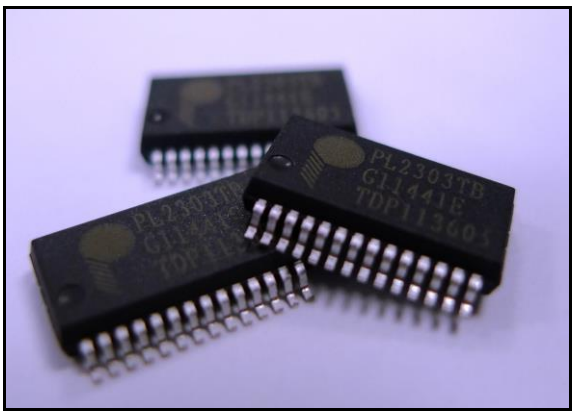
# PL2303TB
# USB to Serial Bridge Controller
# Product Datasheet

Document Revision: 1.1.0
Document Release: March 27, 2018




**Prolific Technology Inc.**

7F, No. 48, Sec. 3, Nan Kang Rd.
Nan Kang, Taipei 115, Taiwan, R.O.C.
Telephone: +886-2-2654-6363
Fax: +886-2-2654-6161
E-mail: sales@prolific.com.tw
Website: http://www.prolific.com.tw

## Disclaimer

All the information in this document is subject to change without prior notice. Prolific Technology Inc. does not make any representations or any warranties (implied or otherwise) regarding the accuracy and completeness of this document and shall in no event be liable for any loss of profit or any other commercial damage, including but not limited to special, incidental, consequential, or other damages.

## Trademarks

The Prolific logo is a registered trademark of Prolific Technology Inc. All brand names and product names used in this document are trademarks or registered trademarks of their respective holders.

## Copyrights

# Revision History

| Revision | Description | Date |
|---|---|---|
| 1.1.0 | ➢ Remove Distributors Contact Information. | March 27, 2018 |
| 1.0.1 | ➢ Modify Ordering Information | May 4, 2012 |
| 1.0.0 | ➢ PL2303TB Product Datasheet – Formal Release | April 12, 2012 |

# Table of Contents

# List of Figures



# List of Tables

# 1.0 Features

- Full Compliant with USB Specification v2.0 (Full-Speed)
- USB-IF Logo Compliant with TID 40001308
- UHCI/OHCI (USB1.1), EHCI (USB 2.0), xHCI (USB 3.0) Host Controller Compatible
- On Chip USB 1.1 Transceiver, 5V→3.3V regulator, and 12 MHz crystal oscillator
- Single Chip USB to RS232 Serial UART Interface:
  - Full-duplex transmitter and receiver (TXD and RXD)
  - Six MODEM control pins (RTS, CTS, DTR, DSR, DCD, and RI)
  - 5, 6, 7 or 8 data bits
  - Odd, Even, Mark, Space, or None parity mode
  - One, one and a half, or two stop bits
  - Parity error, frame error, and serial break detection
  - Programmable baud rate from 75 bps to 12 Mbps
  - External RS232 driver power down control
  - Independent power source for serial interface
  - Works with existing PC COM Port software applications
- Supports RS422/RS485 serial interface (TXD, DTR_N, and RTS_N pins should be externally pulled-up to 5V when 5V interface is applied).
- Extensive Flow Control Mechanism:
  - Adjustable high/low watermark level
  - Automatic hardware flow control with CTS/RTS
  - Automatic software flow control with XON/XOFF
  - Inbound data buffer overflow detection
- Configurable 512-byte bi-directional data buffer:
  - 256-byte outbound buffer and 256-byte inbound buffer; or
  - 128-byte outbound buffer and 384-byte inbound buffer
- Optional external serial EEPROM for startup device configurations
- Supports Remote Wake-up from RS232 input pin signals (RI_N, RXD, DSR_N, DCD_N, CTS_N) and configurable using external EEPROM. Default pin is RI_N.
- Supports Twelve (12) General Purpose I/O (GPIO) pins configuration:
  - Four (4) General Purpose I/O (GP0, GP1, PI_0, & PI_1) standard pins
  - Eight (8) Auxiliary General Purpose I/O (RI_N, DCD_N, DSR_N, CTS_N, DTR_N, RTS_N, RXD, & TXD) pins.
  - Each GPIO pin has output enable value control and input value accessible by driver
- Supports 48/24/12/6/3/1.5 MHz clock output using GP0/GP1 pins
- Supports TXD-RXD Access LED display control using PI_0/P1_1 pins
- Supports USB Selective Suspend (Run-Time Power Management)

- Supports Pulse-Width Modulation (PWM) output on DTR_N, DCD_N, DSR_N, & CTS_N pins with frequency around 370Hz to 47KHz and duty cycle from 1/256 to 255/256.
- Supports Chip Suspend on Powered State (USB-IF Compliance Logo Test Requirement) with configured external EEPROM.
- Provides royalty-free Virtual COM Port (VCP) driver support for:
  - Windows 2000, XP, Vista, and 7 (Microsoft Certified Logo Drivers)
  - Windows Server 2003, 2008, 2008 R2
  - Windows 8
  - Windows XP Embedded (XPe), Point-of-Service (WEPOS), and POSReady
  - Mac OS 8/9, OS X
  - Linux/Android OS (kernel does not include PL2303TB driver)
  - Provides Driver Customization for:
    - Windows CE 4.2, 5.0, 6.0, and Windows Embedded Compact 7 (SDK)
    - Customer VID/PID and special baud rates
- Low Operating Power Consumption and Suspend Current
- -40°C to 85°C Operating Temperature
- Small footprint 28-pin SSOP IC package (RoHS compliant and Pb-free Green Compound)

## 1.1 Prolific USB to Serial Product Comparison

Prolific provides a series of related USB-to-Serial products to meet different design and requirements:

| Part Number | Baud Rate | Crystal | RS232 Interface | Memory | GPIO | RS422/ RS485 | PWM | Multiple Clock Output | TX-RX Access LED |
|---|---|---|---|---|---|---|---|---|---|
| PL2303TA | 6Mbps | 12MHz | ✓ | 24c02 | 2 | | | | |
| PL2303HXD | 12Mbps | Internal | ✓ | OTP | 8 | ✓ | | | |
| PL2303TB | 12Mbps | 12MHz | ✓ | 24c02 | 12 | ✓ | ✓ | ✓ | ✓ |

Check Prolific Sales for a more complete offering on USB to Serial bridge controllers.

## 1.2 Product Applications

- Applications include:
  - Single-chip upgrade solution for Legacy RS232 devices to USB interface
  - USB to RS232/RS422/RS485 converters/cables/dongles
  - Healthcare/Medical USB Interface Data Transfer Cable
  - Personal Infotainment/Media Player Docking USB Interface
  - Cellular/PDA USB Interface Data Transfer Cable
  - Serial-over-IP Wireless Solution
  - USB Barcode/Smart Card Readers
  - GPS/Navigation USB Interface
  - Point-of-Sale (POS) Terminals/Printers
  - PC Docking Station/Port Replicators
  - Industrial/Instrumentation/Automation Control USB Interface
  - USB Modem/Wireless/Zigbee USB Interface
  - Set-Top Box (STB) / Home Gateway USB Interface
  - Battery Charger Application
  - MCU-based devices to USB interface

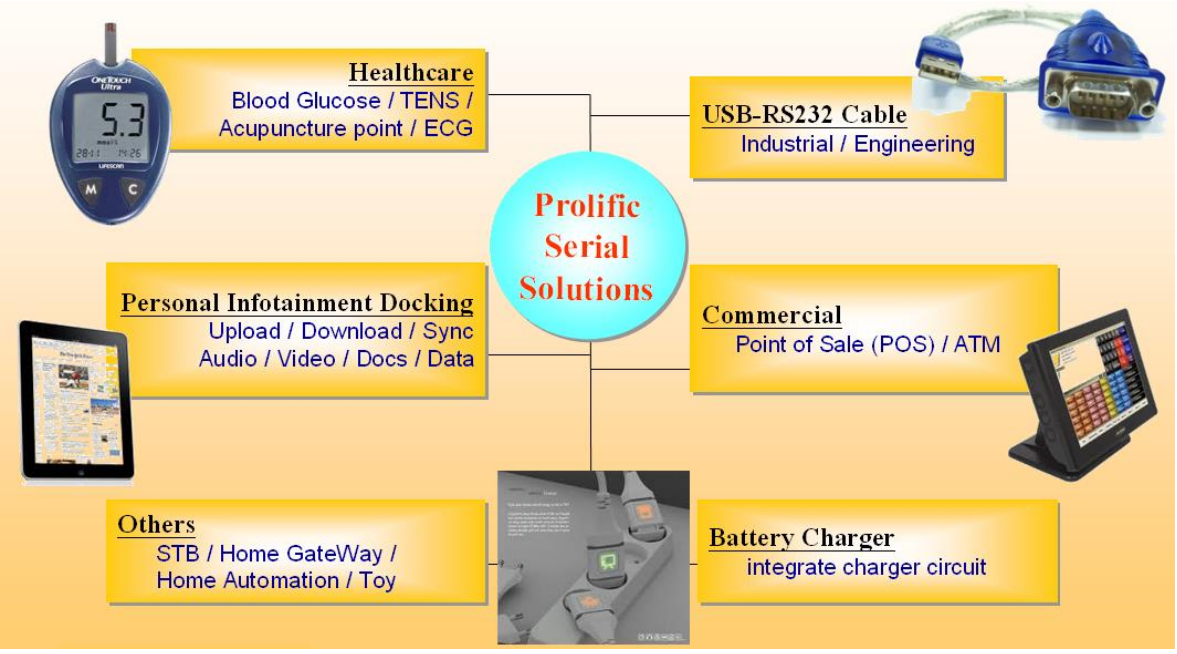



**Figure 1-1 PL2303TB Product Application Areas**

# 2.0 Functional Block Diagram

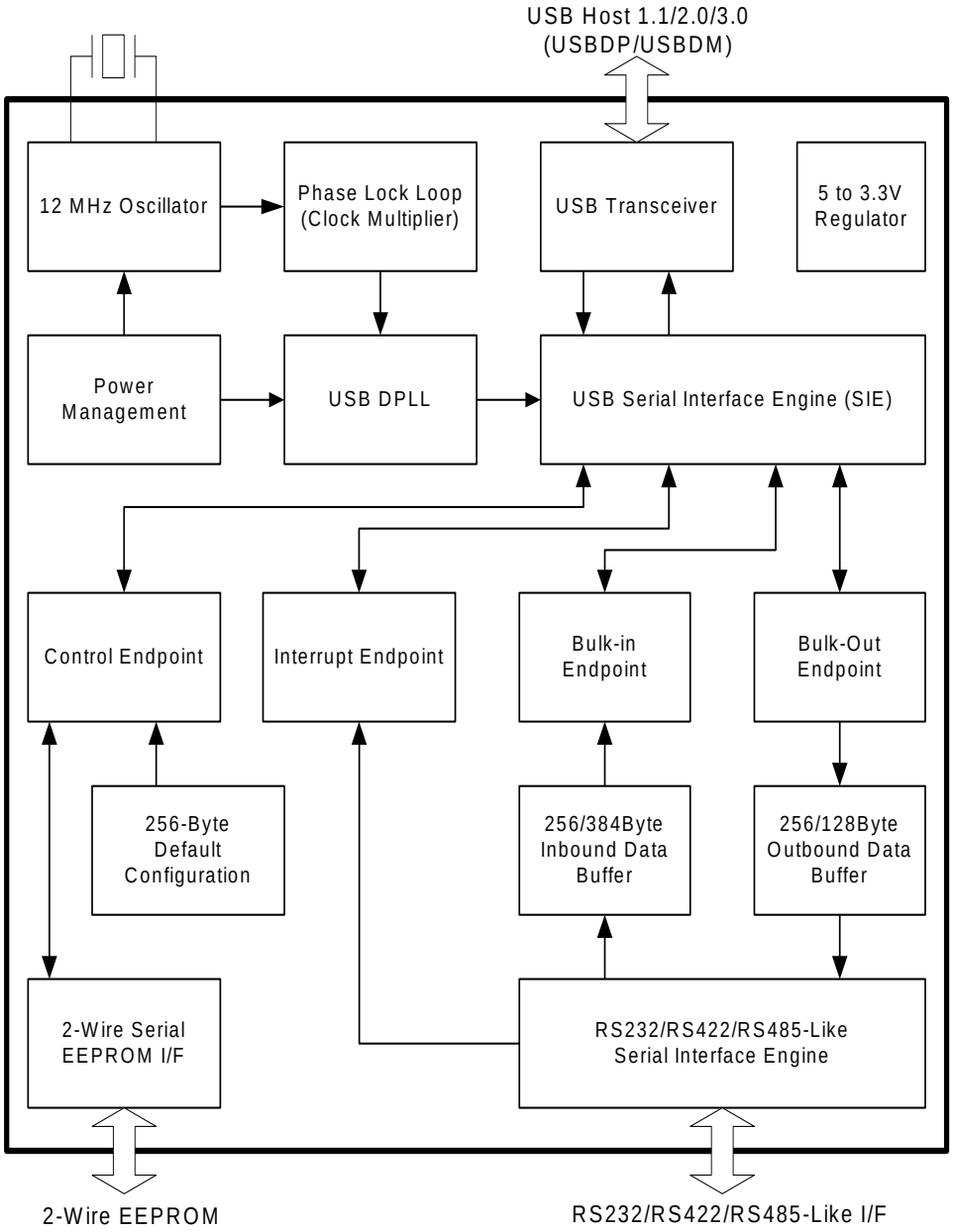



**Figure 2-1 Block Diagram of PL2303TB**

# 3.0 Introduction

PL2303TB provides a convenient solution for connecting an RS232-like full-duplex asynchronous serial device to any Universal Serial Bus (USB) capable host. PL2303TB highly compatible drivers could simulate the traditional COM port on most operating systems allowing the existing applications based on COM port to easily migrate and be made USB ready without having to rewrite the COM port software application.

By taking advantage of USB bulk transfer mode, large data buffers, and automatic flow control, PL2303TB is capable of achieving higher throughput compared to traditional UART (Universal Asynchronous Receiver Transmitter) ports. When real RS232 signaling is not required, baud rate higher than 115200 bps could be used for even higher performance. The flexible baud rate generator of PL2303TB could be programmed to generate any rate between 75 bps and 12M bps.

PL2303TB is exclusively designed for mobile and embedded solutions in mind, providing a small footprint that could easily fit in to any connectors and handheld devices. With very small power consumption in either operating or suspend mode, PL2303TB is perfect for bus powered operation with plenty of power left for the attached devices. Flexible signal level requirement on the RS232-like serial port side also allows PL2303TB to connect directly to any 3.3V~1.8V range devices.

# 4.0 Pin Assignment Outline

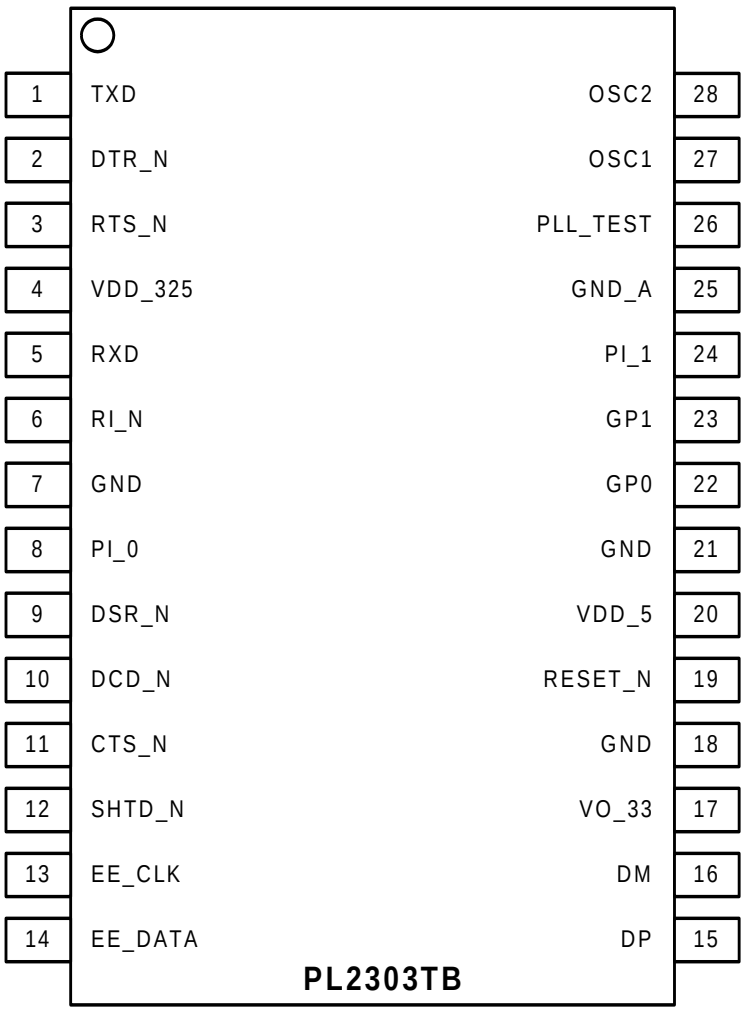



**Figure 4-1 Pin Assignment Outline of PL2303TB**

# 5.0 Pin Assignment & Description

**Pin Type Abbreviation:**

| I: Input | O: Output | I/O: Bidirectional | P: Power/Ground |
|---|---|---|---|

**Table 5-1 Pin Assignment & Description**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | TXD | I/O (1) | Serial port (Transmitted Data).<br>This pin can also be configured a GPIO pin. Refer to GPIO Configuration Pin Section 6.0. |
| 2 | DTR_N | I/O (1) | Serial port (Data Terminal Ready).<br>This pin can also be configured a GPIO pin. Refer to GPIO Configuration Pin Section 6.0. |
| 3 | RTS_N | I/O (1) | Serial port (Request To Send).<br>This pin can also be configured a GPIO pin. Refer to GPIO Configuration Pin Section 6.0. |
| 4 | VDD_325 | P | RS232 VDD. The power pins for the serial port signals. When the serial port is 3.3V, this should be 3.3V. When the serial port is 2.5V, this should be 2.5V. |
| 5 | RXD | I/O (1) | Serial port (Received Data).<br>This pin can also be configured a GPIO pin. Refer to GPIO Configuration Pin Section 6.0. |
| 6 | RI_N | I/O (1) | Serial port (Ring Indicator). For Remote Wakeup use.<br>This pin can also be configured a GPIO pin. Refer to GPIO Configuration Pin Section 6.0. |
| 7 | GND | P | Ground |
| 8 | PI_0 | I/O (1) | General Purpose I/O Pin.<br>This pin can also be configured in EEPROM as a TXD and/or RXD Access LED drive (LED flashes while transmitting or receiving data via USB). Refer to GPIO Pin Configuration Section 6.0. |
| 9 | DSR_N | I/O (1) | Serial port (Data Set Ready).<br>This pin can also be configured as a GPIO pin; or PWM pin in EEPROM. Refer to GPIO Pin Configuration Section 6.0. |
| 10 | DCD_N | I/O (1) | Serial port (Data Carrier Detect).<br>This pin can also be configured in EEPROM as a GPIO pin; or PWM pin in EEPROM. Refer to GPIO Pin Configuration Section 6.0. |
| 11 | CTS_N | I/O (1) | Serial port (Clear To Send).<br>This pin can also be configured in EEPROM as a GPIO pin; or PWM pin in EEPROM. Refer to GPIO Pin Configuration Section 6.0. |
| 12 | SHTD_N | O (2) | RS232 Transceiver Shut Down Control |
| 13 | EE_CLK | I/O (3) | 2-Wire Serial EEPROM Clock |
| 14 | EE_DATA | I/O (3) | 2-Wire Serial EEPROM Data |
| 15 | DP | I/O | USB port D+ signal |
| 16 | DM | I/O | USB port D- signal |
| 17 | VO_33 | P | Regulator Power Output, 3.3V |
| 18 | GND | P | Ground |
| 19 | RESET_N | I (4) | External System Reset (Active Low) |

| | | | |
|---|---|---|---|
| 20 | VDD_5 | P | USB port $V_{BUS}$, 5V Power. |
| 21 | GND | P | Ground |
| 22 | GP0 | I/O (5) | General Purpose I/O Pin.<br>This pin can also be configured in EEPROM as Clock Output Select (48/24/12/6/3/1.5 MHz). Refer to GPIO Pin Configuration Section 6.0. |
| 23 | GP1 | I/O (5) | General Purpose I/O Pin.<br>This pin can also be configured in EEPROM as Clock Output Select (48/24/12/6/3/1.5 MHz). Refer to GPIO Pin Configuration Section 6.0. |
| 24 | PI_1 | I/O (5) | General Purpose I/O Pin.<br>This pin can also be configured in EEPROM as a TXD or RXD Access LED drive (LED flashes while transmitting or receiving data via USB). Refer to GPIO Pin Configuration Section 6.0. |
| 25 | GND_A | P | Analog Ground for PLL |
| 26 | PLL_TEST | I (4) | PLL test mode control |
| 27 | OSC1 | I | Crystal oscillator input |
| 28 | OSC2 | O | Crystal oscillator output |

**Notes:**

**(1)** – SCHMITT In/CMOS Out, 5V Tolerant, Bi-directional Pad. Level and Driving Capability decided by VDD_325, 4mA Output Driving Capability

**(2)** – CMOS Out, 3.3V, Output Pad, 4mA Output Driving Capability.

**(3)** – SCHMITT In/CMOS Out, 5V Tolerant, Bi-directional Pad with internal resistor pulling-up to 3.3V, 4mA Output Driving Capability.

**(4)** – LVTTL In, 3.3V, Input Pad.

**(5)** – SCHMITT In/CMOS Out, 5V Tolerant, Bi-directional Pad, 4mA Output Driving Capability.

# 6.0 GPIO Pin Configuration

The table below shows which PL2303TB pins can be configured as a General Purpose I/O (GPIO) pin. Using external EEPROM, some pins can also be configured as special function pins like clock output, access LED, and PWM output pin. All in all, PL2303TB can allow up to 12 GPIO pins to be configured.

**Table 6-1 GPIO Pin Configuration Options**

| Pin Name | Pin Number | General Purpose IO (GPIO) | Clock Output Select(1) | TXD/RXD Access LED(2) | PWM(3) |
|---|---|---|---|---|---|
| TXD | 1 | GPIO [9] | | | |
| DTR_N | 2 | GPIO [6] (4) | | | PWM_0(4) |
| RTS_N | 3 | GPIO [7] (4) | | | |
| RXD | 5 | GPIO [8] | | | |
| RI_N | 6 | GPIO [0] | | | |
| DSR_N | 9 | GPIO [2] | | | PWM_2 |
| DCD_N | 10 | GPIO [1] | | | PWM_1 |
| CTS_N | 11 | GPIO [3] | | | PWM_3 |
| GP0 | 22 | GPIO [4] | Clock Out 0 | | |
| GP1 | 23 | GPIO [5] | Clock Out 1 | | |
| PI_0 | 8 | GPIO [10] | | LED Out 0 | |
| PI_1 | 24 | GPIO [11] | | LED Out 1 | |

**Notes:**

**(1)** – Clock Output Select with choice of 48MHz, 24MHz, 12MHz, 6MHz, 3MHz, 1.5MHz clock output.

**(2)** – TXD, RXD, or both TXD/RXD access LED control (LED flashes during USB transmit/receive data).

**(3)** – Frequency range is from 366.3Hz to 46.5KHz, and pulse high duty range is from 1/256 to 255/256 in each frequency.

**(1)/(2)/(3)** – These options needs EEPROM to be configured using PL2303TB EEPROM Writer program. See next section.

**(4)** – If TXD and RXD pin is used, DTR_N and RTS_N pins cannot be used as GPIO or PWN pins.

Prolific provides a sample GPIO Test program (Figure 6-1) and program source code for customers to write their own GPIO application. Please contact Prolific FAE or Sales for support.

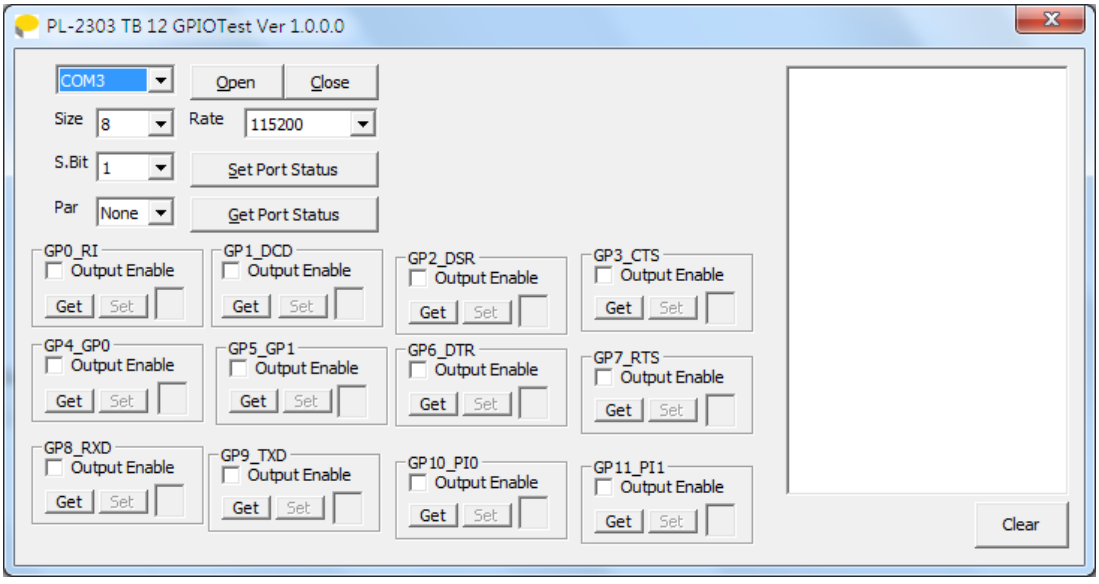



**Figure 6-1 PL2303TB GPIO Test Program**

# 7.0 EEPROM Configuration

The PL2303TB default configuration descriptors are stored in the chip internally which are loaded during power-on reset or USB bus reset when there is no external EEPROM detected or external EEPROM is empty. Some of the descriptors like USB Vendor ID (VID), Product ID (PID), serial number, and other configuration descriptors could be modified using Prolific EEPROM Writer program, and programmed/stored to an external 2-wire serial EEPROM (24C02). The PL2303TB EEPROM Writer also provides the programming controls for setting RS485 function support, Clock Output (for GP0 and GP1 pins), TXD/RXD Access LED (for PI_0, PI_1 pins), and PWM (using DTR_N, DCD_N, DSR_N, and CTS_N pins). When detected, the configuration descriptors stored on the EEPROM will be loaded instead of the default values stored on the chip internally.

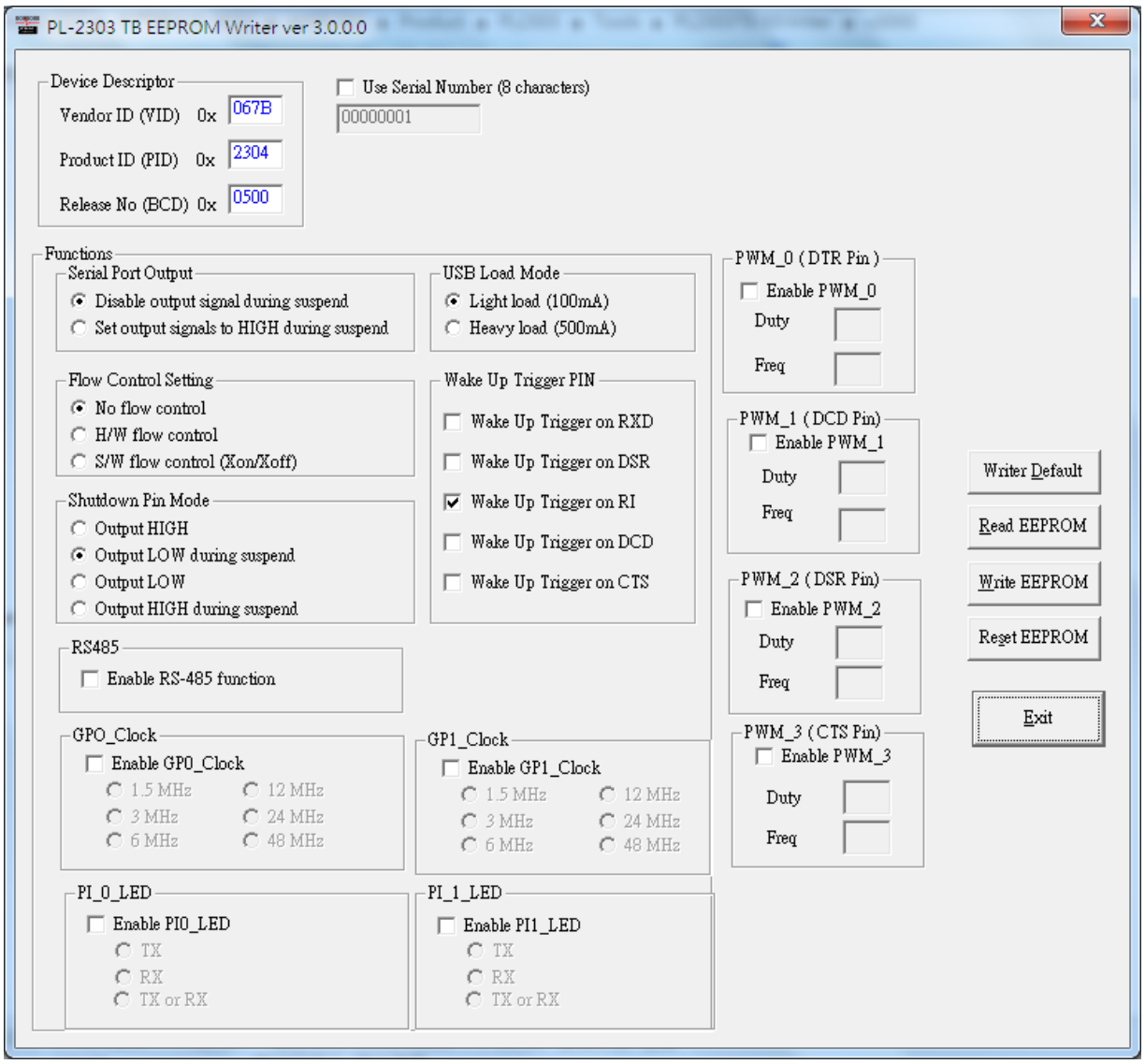



**Figure 7-1 PL2303TB EEPROM Writer Program**

**Table 7-1 EEPROM Configuration Options**

| Device Descriptor | Default Value | Description |
|---|---|---|
| Vendor ID (VID) | 067B (hex) | USB unique Vendor ID of Company or Manufacturer. This ID is applied and registered from USB-IF.<br><br>Refer to this website for applying VID:<br>http://www.usb.org/developers/vendor/ |
| Product ID (PID) | 2304 (hex) | USB Product ID assigned by Company or Manufacturer. |
| Rel. No. (BCD) | 0500 | This field reports the release number of the USB device. This item is fixed and cannot be modified. |
| Serial No. (8 hex characters) | Disabled | This field sets the product USB serial number. Entering a unique serial number allows the device to be assigned the same COM Port number even when plug to other USB ports of the same PC. |
| Serial Port Output | Disable | This option allows setting the serial port output pin signals (TXD, RTS, DTR) to HIGH during suspend mode. |
| USB Load Mode | Light Load (100mA) | This option sets the USB device maximum power if 100mA (low-power) or 500mA (high power). |
| Flow Control Setting | No Flow Control | This option allows to set the flow control initial setting to none, H/W, or S/W control.<br>Note: H/W and S/W flow control can also be set and configured on customer/user serial communication software. |
| Wakeup Trigger Pin | Wakeup trigger on RI | This option allows setting the trigger pin for remote wakeup function. When in suspend mode, changes on the enabled serial port input signals could trigger a wakeup event. |
| Shutdown Pin Mode | Output LOW during suspend | This option allows setting the Shutdown pin (Pin 12) mode to Output HIGH or LOW on normal mode or Suspend mode. |
| RS485 | Disable | Enable this option for RS-485 application. |
| GPO_Clock | Disable | This option allows configuring the GPO pin as a Clock Output enable pin with choice of 1.5/3/6/12/24/48MHz frequency. |
| GP1_Clock | Disable | This option allows configuring the GP1 pin as a Clock Output enable pin with choice of 1.5/3/6/12/24/48MHz frequency. |

| | | |
|---|---|---|
| PI0_LED | Disable | This option allows configuring and enabling the PI_0 pin as Access LED for active TXD, RXD, or both. LED connected to this pin will flash (period is 0.3s) during USB transmission. |
| PI1_LED | Disable | This option allows configuring and enabling the PI_1 pin as Access LED for active TXD, RXD, or both. LED connected to this pin will flash (period is 0.3s) during USB transmission. |
| PWM_0 (DTR_N) | Disable | This option allows configuring the DTR_N pin as PWM control output pin. Frequency range is from 366.3Hz to 46.5KHz, and pulse high duty range is from 1/256 to 255/256 in each frequency. |
| PWM_1 (DCD_N) | Disable | This option allows configuring the DCD_N pin as PWM control output pin. Frequency range is from 366.3Hz to 46.5KHz, and pulse high duty range is from 1/256 to 255/256 in each frequency. |
| PWM_2 (DSR_N) | Disable | This option allows configuring the DSR_N pin as PWM control output pin. Frequency range is from 366.3Hz to 46.5KHz, and pulse high duty range is from 1/256 to 255/256 in each frequency. |
| PWM_3 (CTS_N) | Disable | This option allows configuring the CTS_N pin as PWM control output pin. Frequency range is from 366.3Hz to 46.5KHz, and pulse high duty range is from 1/256 to 255/256 in each frequency. |

# 8.0 Data Formats & Programmable Baud Rate Generator

The PL2303TB supports versatile data formats and has a programmable baud rate generator. The supported data formats are shown on Table 8-1. The programmable baud rate generator supports baud rates up to 12Mbps. Windows driver already supports several baud rate settings shown in Table 8-2.

**Table 8-1 Supported Data Formats**

| | Description |
|---|---|
| Stop bits | 1<br>1.5<br>2 |
| Parity type | None<br>Odd<br>Even<br>Mark<br>Space |
| Data bits | 5, 6, 7, 8 |

**Table 8-2 Baud Rate Settings (Supported by Standard Driver)**

| Baud Rates (bps) | Baud Rates (bps) | Baud Rates (bps) | Baud Rates (bps) | Baud Rates (bps) |
|---|---|---|---|---|
| 12000000 | | | | |
| 6000000 | 460800 | 134400 | 19200 | 1800 |
| 3000000 | 403200 | 128000 | 14400 | 1200 |
| 2457600 | 268800 | 115200 | 9600 | 600 |
| 1228800 | 256000 | 57600 | 7200 | 300 |
| 921600 | 230400 | 56000 | 4800 | 150 |
| 806400 | 201600 | 38400 | 3600 | 110 |
| 614400 | 161280 | 28800 | 2400 | 75 |

**Note:** For other special baud rate requirements, please contact Prolific FAE for driver customization support. The baud rates listed on the above table are already supported by the standard driver and only needs to be set by the COM port configuration of the application software on the PC.

# 9.0 DC & Temperature Characteristics

## 9.1 Absolute Maximum Ratings

**Table 9-1 Absolute Maximum Ratings**

| Items | Ratings |
|---|---|
| Power Supply Voltage | -0.3 to 5.5 V |
| Input Voltage of 3.3V I/O | -0.3 to VO_33 + 0.3 V |
| Input Voltage of 3.3V I/O with 5V Tolerance I/O | -0.3 to VDD_5 + 0.3V |
| Output Voltage of 3.3V I/O | -0.3 to VO_33 + 0.3 V |
| Storage Temperature | -40 to 150 $^{o}$C |

## 9.2 DC Characteristics

**Table 9-2 Operating Voltage and Suspend Current**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Voltage Range | VDD_5 | 3.6 | 5 | 5.5 | V |
| Regulator Output Driving Current (VDD_5 = 5V) | $I_{LOAD}$ | - | - | 150 | mA |
| Operating Current(1) (Power Consumption) | $I_{DD}$ | - | 8 | 10 | mA |
| Suspend Current | $I_{SUS}$ | - | 370 | 400 | μA |

**Note:** (1) – No device connected.

### 9.2.1 3.3V I/O Pins

**Table 9-2-1 3.3V I/O Pins**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Driving Capability | $I_{DD}$ | -- | 4 | -- | mA |
| Output Voltage of Regulator | VO_33 | 3.0 | 3.3 | 3.6 | V |
| Input Voltage (CMOS) | | | | | |
| Low | $V_{IL}$ | -- | -- | 0.3* VO_33 | V |
| High | $V_{IH}$ | 0.7* VO_33 | -- | -- | V |
| Input Voltage (LVTTL) | | | | | |
| Low | $V_{IL}$ | -- | -- | 0.8 | V |
| High | $V_{IH}$ | 2.0 | -- | -- | V |
| Schmitt Trigger Threshold Voltage | | | | | |
| Negative going | $V_{t-}$ | 0.9 | 1.2 | -- | V |
| Positive going | $V_{t+}$ | -- | 2.1 | 2.5 | V |
| Output Voltage, 3.3V | | | | | |
| Low | $V_{OL}$ | -- | -- | 0.4 | V |
| High | $V_{OH}$ | 2.4 | -- | -- | V |

### 9.2.2 Serial I/O Pins

**Table 9-2-2a VDD_325@3.3V Serial I/O Pins**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Driving Capability | $I_{DD}$ | -- | 4 | -- | mA |
| Power Supply for Serial I/O Pins | VDD_325 | 3.0 | 3.3 | 3.6 | V |
| Input Voltage | | | | | |
| Low | $V_{IL}$ | -- | -- | 0.8 | V |
| High | $V_{IH}$ | 2.0 | -- | -- | V |
| Schmitt Trigger Threshold Voltage | | | | | |
| Negative going | $V_{t-}$ | 0.8 | 1.1 | -- | V |
| Positive going | $V_{t+}$ | -- | 1.6 | 2.0 | V |
| Output Voltage | | | | | |
| Low | $V_{OL}$ | -- | -- | 0.4 | V |
| High | $V_{OH}$ | 2.4 | -- | -- | V |

**Table 9-2-2b VDD_325@2.5V Serial I/O Pins**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Driving Capability | $I_{DD}$ | -- | 2.6 | -- | mA |
| Power Supply for Serial I/O Pins | VDD_325 | 2.25 | 2.5 | 2.75 | V |
| Input Voltage | | | | | |
| Low | $V_{IL}$ | -- | -- | 0.25* VDD_325 | V |
| High | $V_{IH}$ | 0.7* VDD_325 | -- | -- | V |
| Schmitt Trigger Threshold Voltage | | | | | |
| Negative going | $V_{t-}$ | 0.25* VDD_325 | 0.84 | -- | V |
| Positive going | $V_{t+}$ | -- | 1.31 | 0.7* VDD_325 | V |
| Output Voltage | | | | | |
| Low | $V_{OL}$ | -- | -- | 0.4 | V |
| High | $V_{OH}$ | 1.85 | -- | -- | V |

**Table 9-2-2c VDD_325@1.8V Serial I/O Pins**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Driving Capability | $I_{DD}$ | -- | 1.4 | -- | mA |
| Power Supply for Serial I/O Pins | VDD_325 | 1.65 | 1.8 | 1.95 | V |
| Input Voltage | | | | | |
| Low | $V_{IL}$ | -- | -- | 0.25* VDD_325 | V |
| High | $V_{IH}$ | 0.7* VDD_325 | -- | -- | V |
| Schmitt Trigger Threshold Voltage | | | | | |
| Negative going | $V_{t-}$ | 0.25* VDD_325 | 0.6 | -- | V |
| Positive going | $V_{t+}$ | -- | 1.04 | 0.7* VDD_325 | V |
| Output Voltage | | | | | |
| Low | $V_{OL}$ | -- | -- | 0.4 | V |
| High | $V_{OH}$ | 1.25 | -- | -- | V |

## 9.3 Clock Characteristics

**Table 9-3 Clock Characteristics**

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Frequency of Operation | 11.976 | 12.000 | 12.024 | MHz |
| Clock Period | 83.1 | 83.3 | 83.5 | ns |
| Duty Cycle | 45 | 50 | 55 | % |

## 9.4 Temperature Characteristics

**Table 9-4 Temperature Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Temperature | -- | -40 | -- | 85 | $^{o}$C |
| Junction Operation Temperature | $T_J$ | -40 | 25 | 125 | $^{o}$C |

## 9.5 Leakage Current and Capacitance

**Table 9-5 Leakage Current and Capacitance**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Leakage Current*1 | $I_L$ | -10 | ±1 | 10 | µA |
| Tri-state Leakage Current | $I_{oz}$ | -10 | ±1 | 10 | µA |
| Input Capacitance | $C_{IN}$ | -- | 2.8 | -- | pF |
| Output Capacitance | $C_{OUT}$ | 2.7 | -- | 4.9 | pF |
| Bi-directional Buffer Capacitance | $C_{BID}$ | 2.7 | -- | 4.9 | pF |

**Note:** *1. No pull-up or pull-down resistor.

## 9.6 Power-On Reset

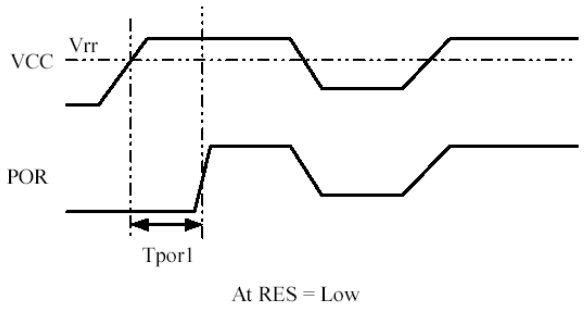



**Figure 9-1 Power-On Reset Diagram**

**Table 9-6 Power-On Reset**

| Description and Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power supply voltage | VCC | 2.8 | 3.3 | 4.0 | V |
| VCC rise relax voltage | $V_{rr}$ | 1.8 | 2.3 | 2.8 | V |
| Power output low duration<br>VCC \| $_{rise}$ @ $V_{rr}$ to POR \| $_{rise}$ @ 1/2*VCC<br>(VCC slew rate = 1V/1us) | $T_{por1}$ | 1.3 | 5 | 264 | µS |

## 10.0 Special GPIO Application Reference Schematic

Figure 10-1 and 10-2 shows the reference schematic for PL2303TB special GPIO application:

- Clock Output (48/24/12/6/3/1.5 MHz) using GP0/GP1 pins
- TXD-RXD Access LED display control using PI_0/P1_1 pins
- Pulse-Width Modulation (PWM) output on DTR_N, DCD_N, DSR_N, & CTS_N pins with frequency around 370Hz to 47KHz and duty cycle from 1/256 to 255/256.

Contact Prolific FAE for more PCB design support.

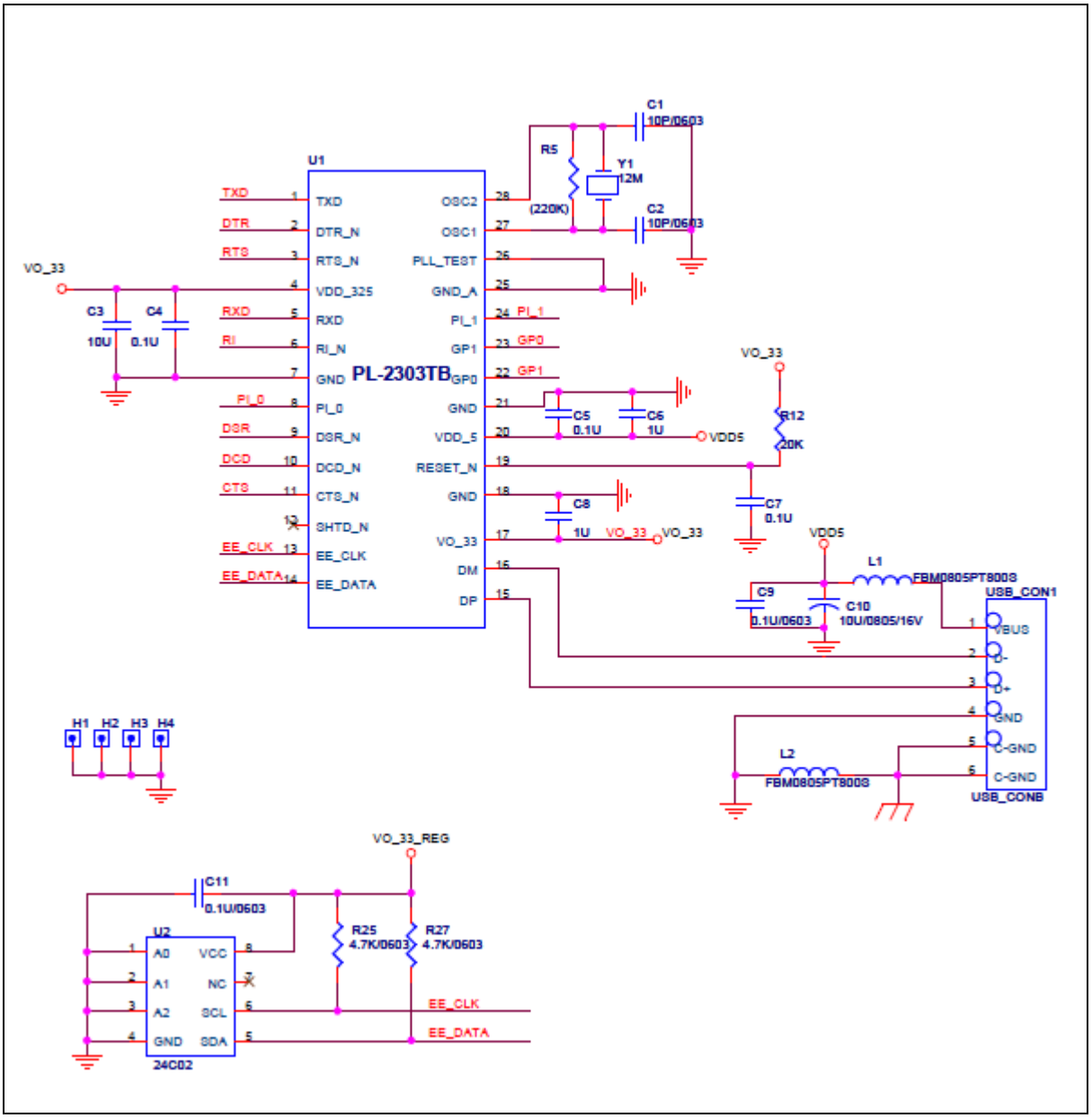



**Figure 10-1 PL2303TB Reference Schematic**

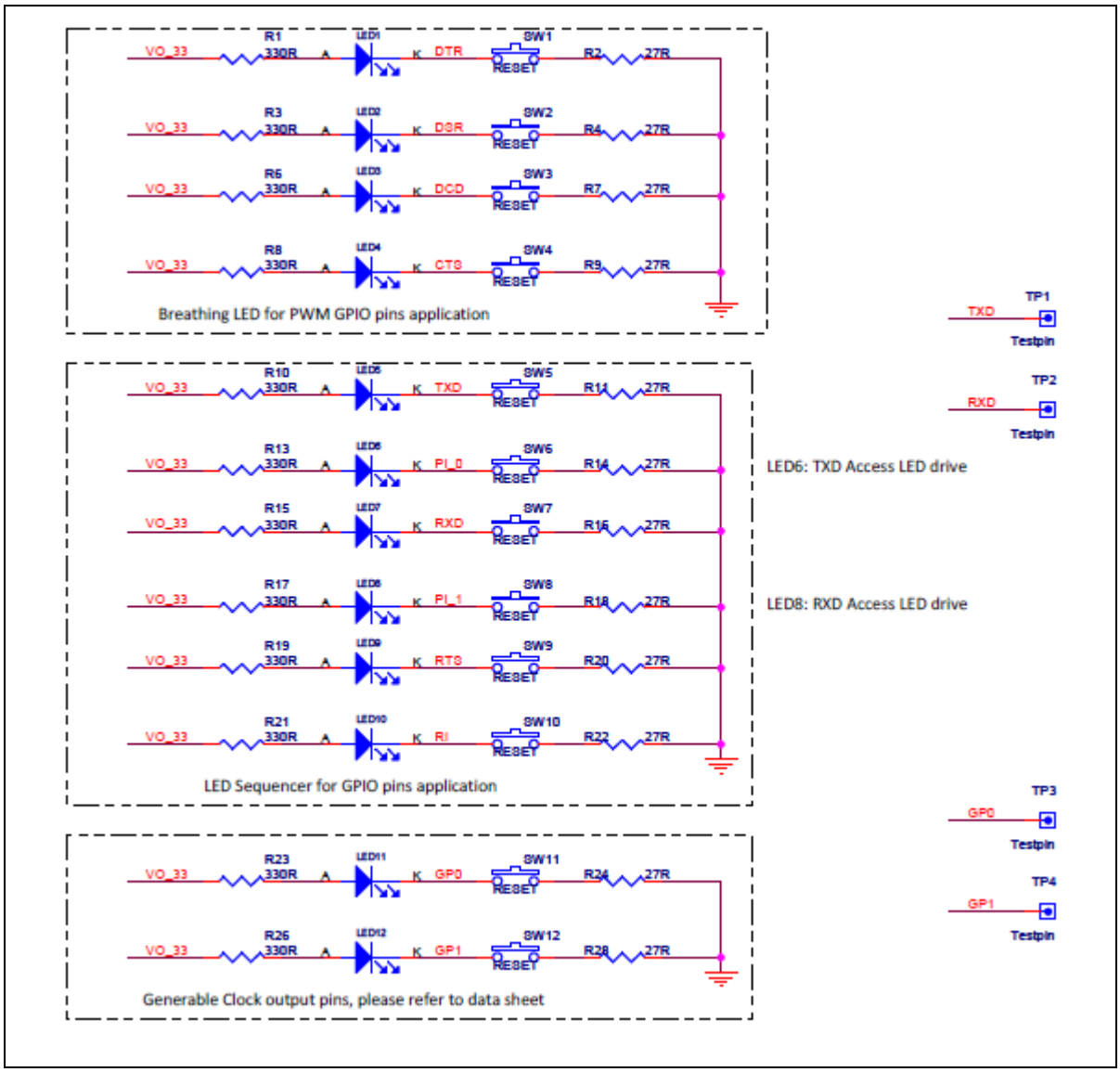



**Figure 10-2 PL2303TB Special GPIO Reference Schematic**

# 11.0 Outline Diagram

## 11.1 SSOP28 Package

**Table 11-1 Package Dimension**

| Symbol | Millimeter | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| b | 0.22 | | 0.38 | 0.009 | | 0.015 |
| E | 7.40 | 7.80 | 8.20 | 0.291 | 0.307 | 0.323 |
| E1 | 5.00 | 5.30 | 5.60 | 0.197 | 0.209 | 0.220 |
| L | 0.55 | 0.75 | 0.95 | 0.021 | 0.030 | 0.037 |
| R1 | 0.09 | | | 0.004 | | |
| D | 9.9 | 10.2 | 10.5 | 0.390 | 0.402 | 0.413 |
| A | | | 2.0 | | | 0.079 |
| e | | 0.65 | | | 0.0256 | |
| L1 | | 1.25 | | | 0.050 | |
| A1 | 0.05 | | | 0.020 | | |
| A2 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |

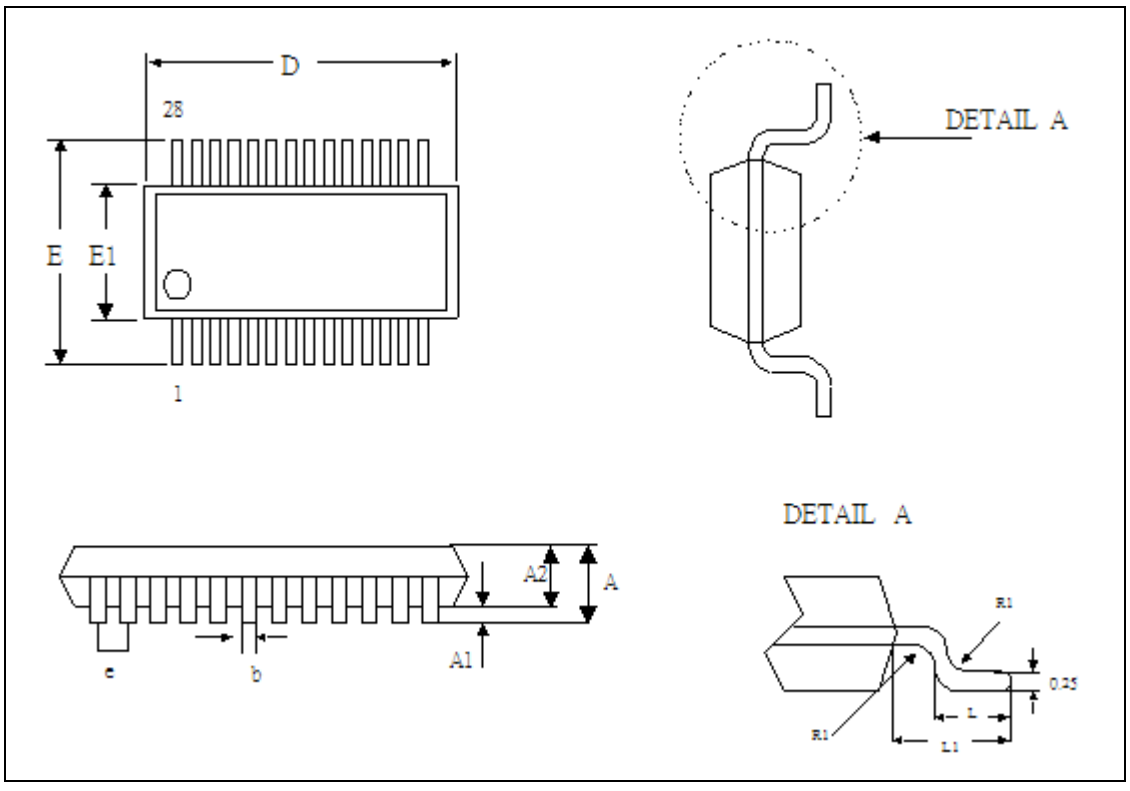



**Figure 11-1 Outline Diagram of PL2303TB SSOP28**

# 12.0 Ordering and Chip Marking Information

This section provides the chip ordering part number information and the chip marking information.

**Table 12-1 Ordering Information**

| Part Number | Package Type |
|---|---|
| PL-2303TB LF | 28-pin SSOP Lead Free |

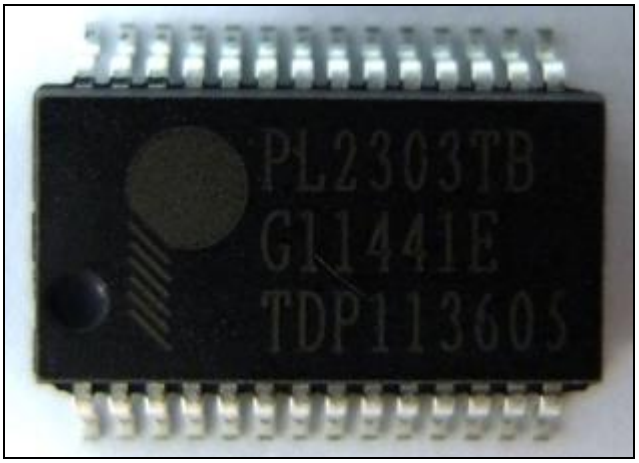



**Figure 12-1 Chip Part Number Information**

**Table 12-2 Chip Marking Information**

| Line | Marking | Description |
|---|---|---|
| First Line | PL2303TB | Chip Product Name |
| Second Line (GYYWWXX) | G | Green compound packing material (Pb-free) |
| | YY | Last two digits of the manufacturing year |
| | WW | Week number of the manufacturing year |
| | XX | Chip Version (1E) |
| Third Line | TXXXXXXXX | Manufacturing LOT code |

Example: "*G11441E*" – means Green packing + Year 2011 + Week no. 44 + 1E chip version.